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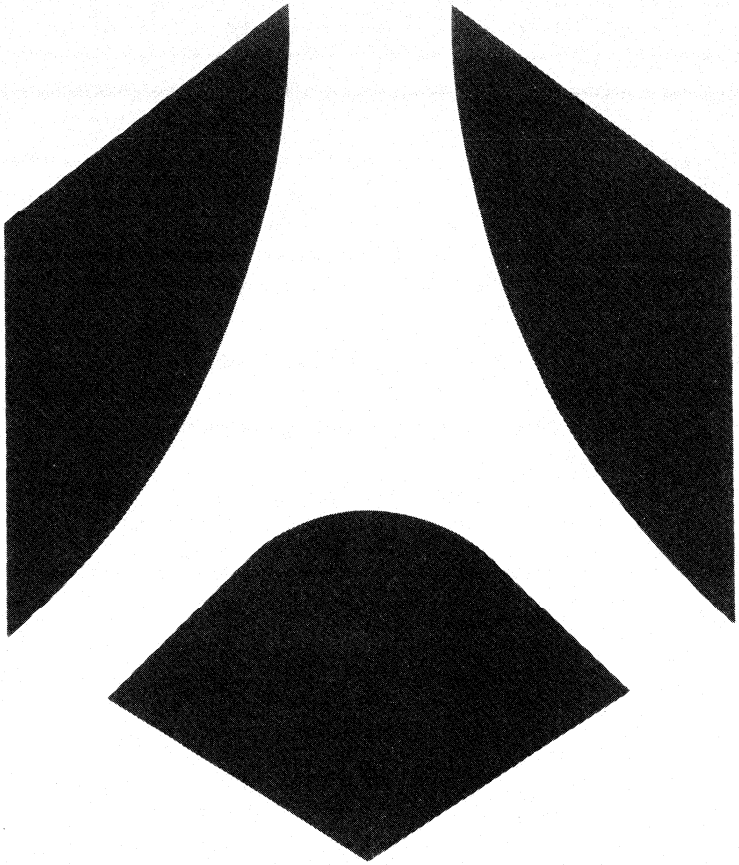
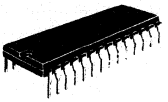
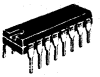
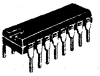


Television and monitor circuits

DEFLECTION CIRCUITS

Function	Part number	Characteristic	Package		Page
Horizontal and vertical	TEA2017	Complete horizontal and vertical deflection circuit for black and white TV sets. Direct drive of frame yoke (maximum output current: ± 1.5 A), direct drive of line darlington, muting output	SIL15		1-9
	TEA2026C	TV scanning and power supply digital processor includes 50-60 Hz identification, security and start-up systems	DIL28		1-19
	TEA2028	TV scanning and power supply digital processor includes 50-60 Hz identification, security and start-up systems. SMPS secondary regulation.			1-29
	TEA2029C	TV scanning and power supply digital processor includes 50-60 Hz identification, security and start-up systems. In conjunction with TEA2162, it provides SMPS secondary regulation.			1-39
	TEA2037A	Low cost horizontal and vertical deflection circuit for black and white TV sets and monochrome displays. Direct drive of frame yoke (maximum output current: ± 1 A), direct drive of line darlington.	DIL16		1-53
Vertical	TEA2115	Vertical power stage with fly-back generator for 110° screen	SIL 7		1-63
Horizontal	TBA920	Line oscillator, sync. separator, phase comparator for monochrome TV sets.	DIL16		1-71
	TBA920S	Line oscillator, sync. separator, phase comparator for monochrome TV sets.			1-71

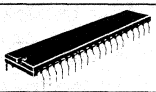
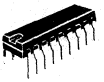
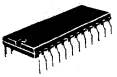
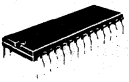
TIME BASE AND SYNCHRO CIRCUIT

Function	Part number	Characteristic	Package		Page
Horizontal	TDA2593	Line oscillator combination, burst, blanking and frame pulse separation for color TV sets.	DIL16		1-77
Parabolic correction	TEA2031A	Ensures the vertical rate, parabolic and keystone correction for 110° screens.	DIL8		1-85

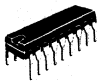
POWER SUPPLIES (SMPS FLY-BACK MODE)

Function	Part number	Characteristic	Package	Page
Switch mode power supply	TEA2018A	Power supply control circuit for fixed frequency fly-back power supplies up to 80 W. Direct drive of the switching transistor. Output current $I_B = KI_C$. Total protection from overload, short-circuit and temperature. Low rest current.	DIL8	1-91
	TEA2019	Power supply control circuit for fixed frequency fly-back power supplies up to 80 W. Direct drive of the switching transistor. Output current $I_B = KI_C$. Total protection from overload, short-circuit and temperature. — Low rest current. — Sync. capability with internal PLL.	DIL14	1-99
	TEA2162	Control IC for fixed frequency fly-back power supplies up to 200 W. In conjunction with TEA2029, this IC provides full secondary regulation for color TV applications (Master/Slave). Optimized power stage drive current. Over-voltage/current protections. Soft-start procedure.	DIL16	1-107
	UAA4006B	Control circuit for fixed frequency fly-back power supplies up to 200 W. Direct drive of switching transistor with self regulated base current. Reduced storage time. Total protection from overload, short circuit and temperature. Very low rest current.	DIL16	1-117

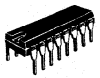
CHROMA CIRCUITS

Function	Part number	Characteristic	Package		Page
High voltage video amplifier	TEA5101	Drives directly R-G-B cathodes and gives measure of cut-off currents.	SIL15		1-125
Video processor	TEA5031D	In conjunction with PAL and/or SECAM decoder, this circuit constitutes a complete and flexible color TV chroma system featuring: on screen display inputs, electronic control of contrast, brightness and saturation, automatic cut-off adjustment, low dissipation, and positive color difference inputs.	DIL28		1-133
	TEA5040	Wide band serial bus controlled video processor with digital control of brightness, saturation and contrast.	DIL40		1-141
PAL decoder	TEA5620	Complete PAL decoding system.	DIL18		1-157
SECAM decoder	TEA5630	Complete SECAM decoding system. Can be combined with PAL decoder for PAL/SECAM applications (automatic PAL/SECAM switching).	DIL24		1-173
PAL/SECAM NTSC1/2 decoder	TEA5640	Automatic PAL/SECAM/NTSC1/NTSC2 decoder. Suppresses all adjustments. No crystal required. Operates with an external frequency reference of 62.5 kHz.	DIL28		1-187

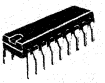
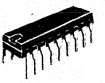
VIDEO AND SOUND IF CIRCUITS

Function	Part number	Characteristic	Package		Page
Video IF	TDA2540	IF amplifier with demodulator and AFC (CCIR standard) for NPN tuner.	DIL16		1-203
	TDA2541	IF amplifier with demodulator and AFC (CCIR standard) for PNP tuner.			1-203
	TDA2542	IF amplifier with demodulator and AFC (French standard).			1-211
	TDA4426	Very stable IF amplifier with demodulator and AFC for PNP tuner.	DIL18		1-217
	TDA4427	Very stable IF amplifier with demodulator and AFC for PNP tuner and inverted AFC.			1-217
	TDA4443	IF amplifier with demodulator for multistandard applications. High input sensitivity. Large AGC capabilities.	DIL16		1-225
Sound IF	TDA4445A	Quasi parallel sound processing with quadrature inter-carrier demodulator. Very high input sensitivity. Good AM suppression.	DIL16		1-233
	TDA4445B	AM/FM sound demodulator. Low AM distortion. Very high input sensitity. No adjustment for the AM demodulator.			1-233

PERITELEVISION INTERFACE CIRCUIT

Function	Part number	Characteristic	Package		Page
Video and AF switch	TEA1014	For monosound TV sets. Follows the SCART specification nº 108.	DIL14		1-241
Video switch	TEA2014	Switched 2 Vpp video output. Not switched 75 Ω, 1 Vpp video output.	DIL8		1-249
R-G-B switch	TEA5114	3-channel high frequency switch (20 MHz), designed for R-G-B and video applications. Low output impedance (75 Ω).	DIL16		1-253
	TEA5115	5-switch (R-G-B, Fast blanking, Sync.) video signal selector. 25 MHz bandwidth for R-G-B signals.	DIL18		1-259
	TEA5116	5-switch (R-G-B, Fast blanking, Sync.) video signal selector. 25 MHz bandwidth for R-G-B signals.			1-267

REMOTE CONTROL AND CHANNEL SELECTOR CIRCUITS

Function	Part number	Characteristic	Package		Page
Transmitter	UAA4000	For ultrasonic or infrared transmission. 32 command capability.	DIL18		1-275
	UAA4000S	Pulse position modulation provides excellent noise immunity.			1-281
Receiver	UAA4009	Complete circuit for PPM demodulation. 12 channel tuning voltage switch (remote and keyboard), one DC voltage output for volume adjustment, standby information.	DIL18		1-287
	TEA5049	Infrared preamplifier working in pulse carrier mode at 400 kHz. Large amplification with AGC. Noise reduction system.	DIL14		1-293

HOMSON COMPONENTS
EMICONDUCTEURS

TEA2017

HORIZONTAL AND VERTICAL DEFLECTION MONITOR

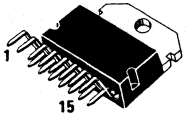
The TEA2017 is an horizontal and vertical deflection circuit. It is particulary intended for black and white TV and display video units but it can also be used in low cost color TV applications. The TEA2017 provides a low cost deflection system.

Mains features

- Direct frame yoke drive ± 1.5 A driving current.
- Line darlington driving capability.
- Built-in frame separator without external components.
- Muting output.
- Integrated flyback generator.
- Frame output protection against short circuits.
- Very few external components.
- High dissipation power package.

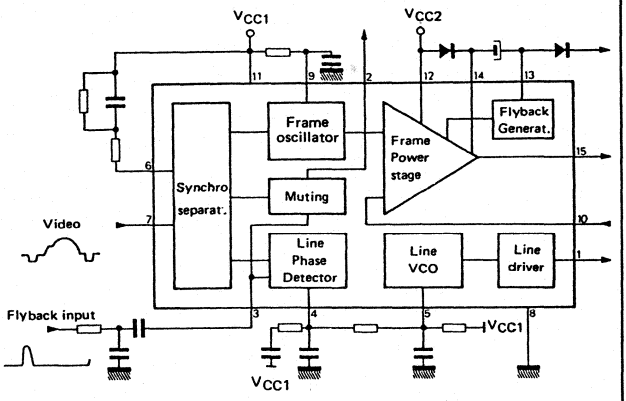
HORIZONTAL AND VERTICAL DEFLECTION MONITOR

CASE CB-501



PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT

1	Line output
2	Muting output
3	Line flyback input
4	Phase detector
5	Line oscillator
6	Synchro separator
7	Video input
8	Ground
9	Frame oscillator
10	Power amplifier negative input
11	V_{CC1}
12	V_{CC2}
13	Flyback generator
14	V_{CC} power stage
15	Frame output

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Direct vertical supply voltage	V_{CC2}	30	V
Flyback vertical peak voltage	V_{FB}	60	V
Vertical output current	I_{OV}	± 1.5	A
Supply voltage	V_{CC1}	20	V
Storage and junction temperature	T_j , T_{stg}	- 40 + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Max junction-case thermal resistance	$R_{th(j-c)}$	3	°C/W
Max junction-ambient thermal resistance	$R_{th(j-a)}$	40	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$; $V_{CC1} = 10$ V ; $V_{CC2} = 24$ V (Unless otherwise specified).

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage (pin 11)	V_{CC1}	8	–	20	V
Supply current (pin 11)	I_{CC1}	–	15	–	mA
Vertical supply voltage (Pin 14)	V_{CC2}	10	–	30	V
Vertical supply current (Pin 14) - V_{CC2} = 30 V without load	I_{CC2}	–	25	–	mA
Video Input (Pin 7)					
Input threshold voltage		–	4	–	V
Video input signal (see figure application No.1)		0.4	–	4	V_{PP}
Flyback input (Pin 3)					
Input impedance		4.5	5.6	7	kΩ
Line output (Pin 1)					
Output current					
Peak value		–	- 500	–	mA
DC value		–	- 180	–	mA
Control pulse width		20	22	24	µs
Output saturation to ground (I = 200 mA)	V_{SAT1}	–	–	2	V
Line oscillator (Pin 5)					
Threshold voltage					
Low level		–	3.2	–	V
High level		–	6.6	–	V
Supply voltage influence on frequency (V_{CC1} = 10 V)	$\frac{\Delta F}{\Delta V}$	–	0.051	0.09	µs/V
Phase comparator (Pin 4)					
Control voltage		–	3 to 7	–	V
Control current		–	± 0.5	–	mA
Control sensibility (see fig. application n° 1)		–	750	–	Hz/µs
Pull in range (see fig. application n° 1)		–	± 800	–	Hz
Frame oscillator (Pin 9)					
Threshold voltage					
Low level		1.8	2	2.2	V
High level		2.6	3.1	3.6	V
Saw tooth voltage with synchronization		–	1	–	V_{PP}
Output power stage (Pin 15)					
Output saturation voltage					
To ground I = 1 A		–	–	0.8	V
To V_{CC} I = 1 A		–	–	2.4	V
Muting (Pin 2)					
Output voltage (muting on : no video signal)		–	8	–	V
Output voltage (muting off)		–	0.7	1.2	V

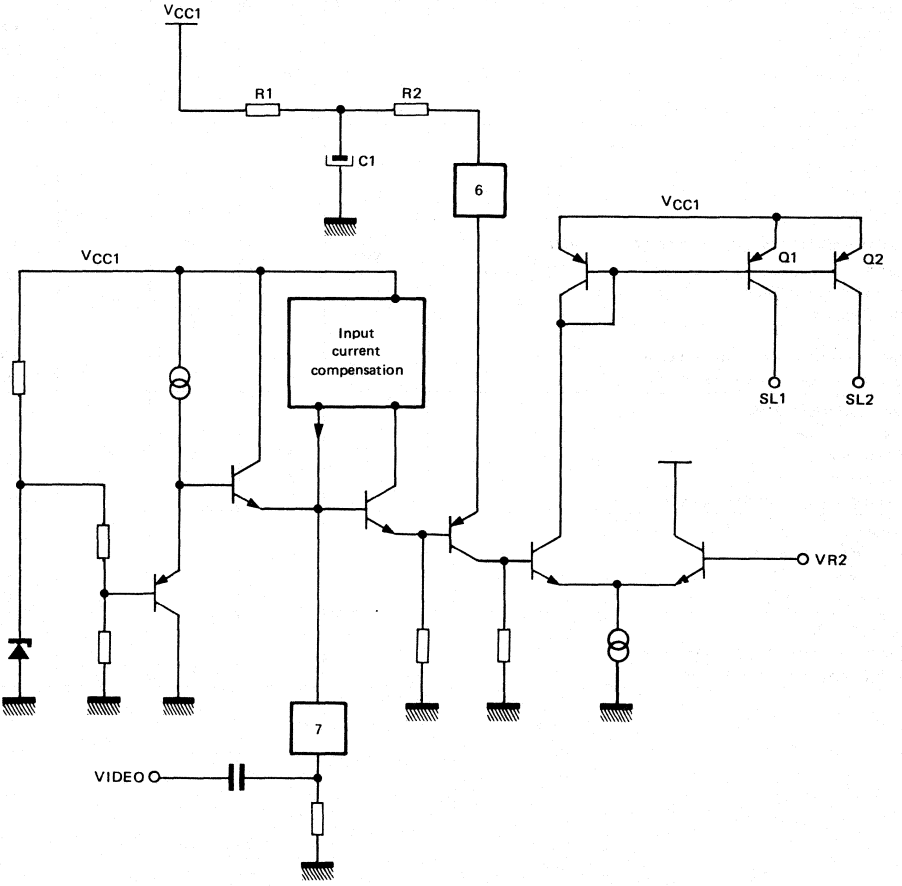
GENERAL DESCRIPTION

The TEA 2017 performs all of the video and power functions required to provide signals for the direct drive of a line darlington and the frame yoke.

It contains :

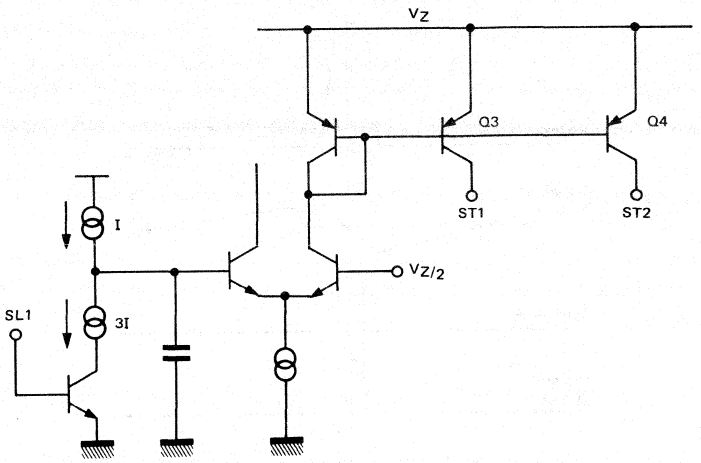
- A synchronizing separator with the slice level of synchro separation determined by the external components.
- An integrated frame synchronizing separator without external components.
- A saw tooth generator for the frame with synchronization allowed during the last fourth of the free run period.
- A power amplifier for direct drive of the frame yoke with overload, short circuit and thermal protections.
- A line phase detector and a voltage control oscillator.
- An open collector output for the direct drive of a line darlington.
- A muting output.

SYNCHRONIZATION SEPARATOR CIRCUIT



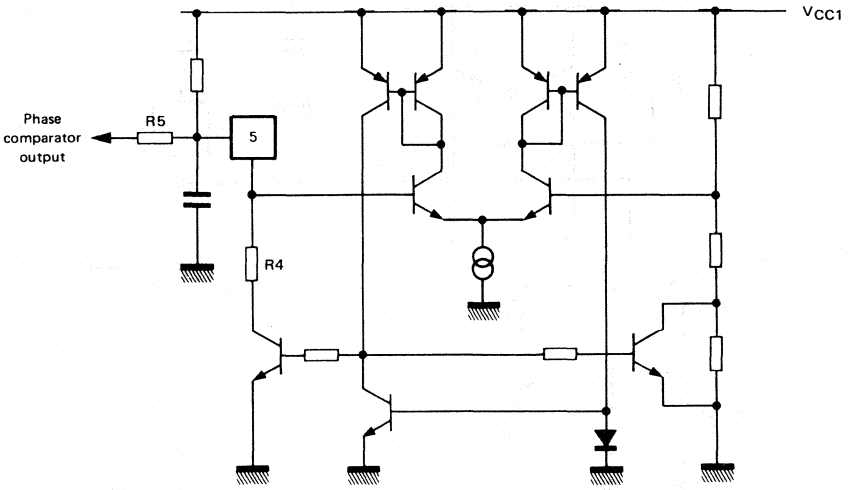
The sync-tip DC level on pin 7 is clamped to 2.5 V. The slice level of sync-separation present on capacitor C1 depends on the value of resistor R1 and R2. When the video signal on pin 7 decreases under the capacitor voltage the transistors Q1 and Q2 provide current for the other parts of the circuit.

FRAME SEPARATOR



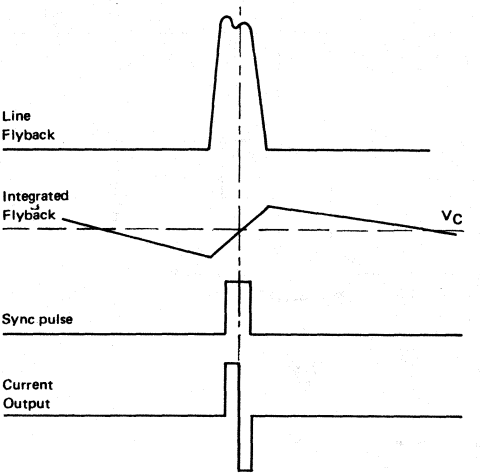
The sync-pulse allows the discharging of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync pulse permits the complete discharging of the capacitor, so during the frame sync-pulse Q3 and Q4 provide current for the other parts of the circuit.

LINE OSCILLATOR

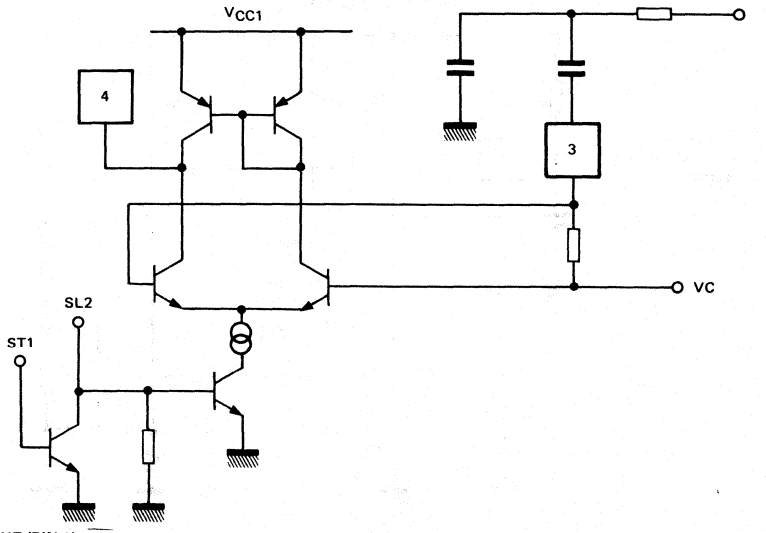


The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The voltage control is applied on resistor R5.

PHASE COMPARATOR



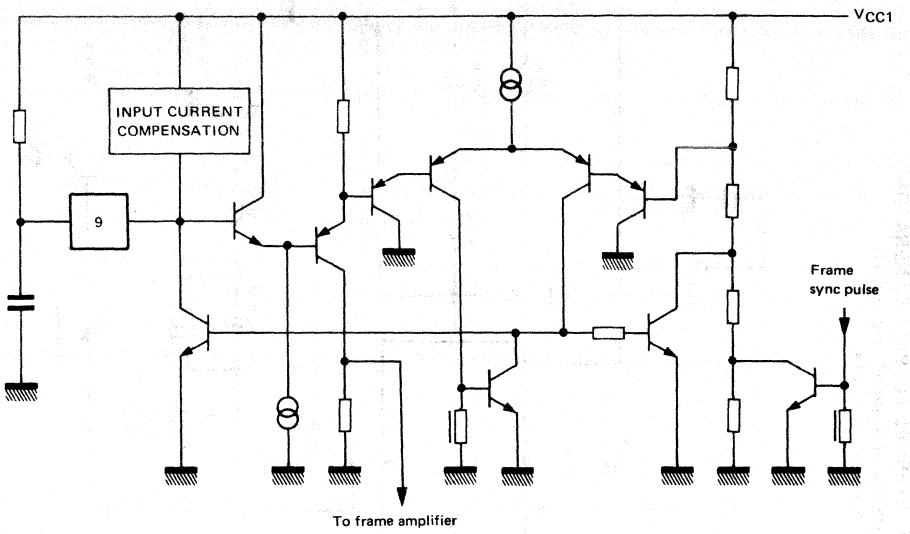
The sync-pulse drives the current in the comparator. The line flyback integrated by the external network gives on pin 3 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 3 superior to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.



LINE OUTPUT (PIN 1)

It is an open collector output which is able to drive pulse current of 500 mA for a rapid discharging of the darlington base. The output pulse time is 22 μs for a 64 μs period.

FRAME OSCILLATOR



The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last fourth of the free run period. The input current during the charge of the capacitor is less than 100 mA.

FRAME OUTPUT AMPLIFIER

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected ; it contains also a thermal protection.

Its positive input is directly connected to the invert of the frame saw tooth.

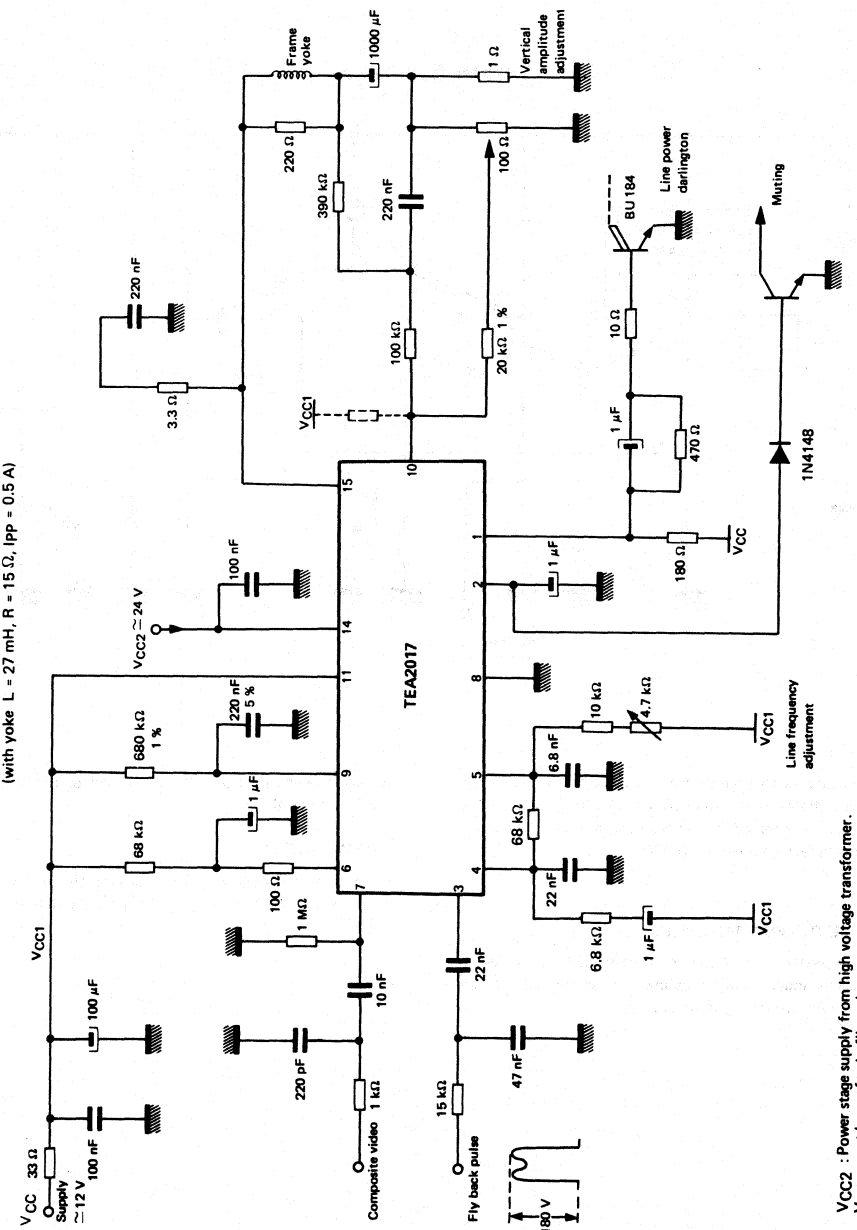
MUTING OUTPUT

It delivers voltage pulse during the line fly-back if there is no video signal on the input. The output impedance is 1 kΩ.

APPLICATION No. 1 (WITHOUT INTERNAL FLYBACK GENERATOR)

TYPICAL BLACK-WHITE TV APPLICATION FOR 14" - 110° SCREEN

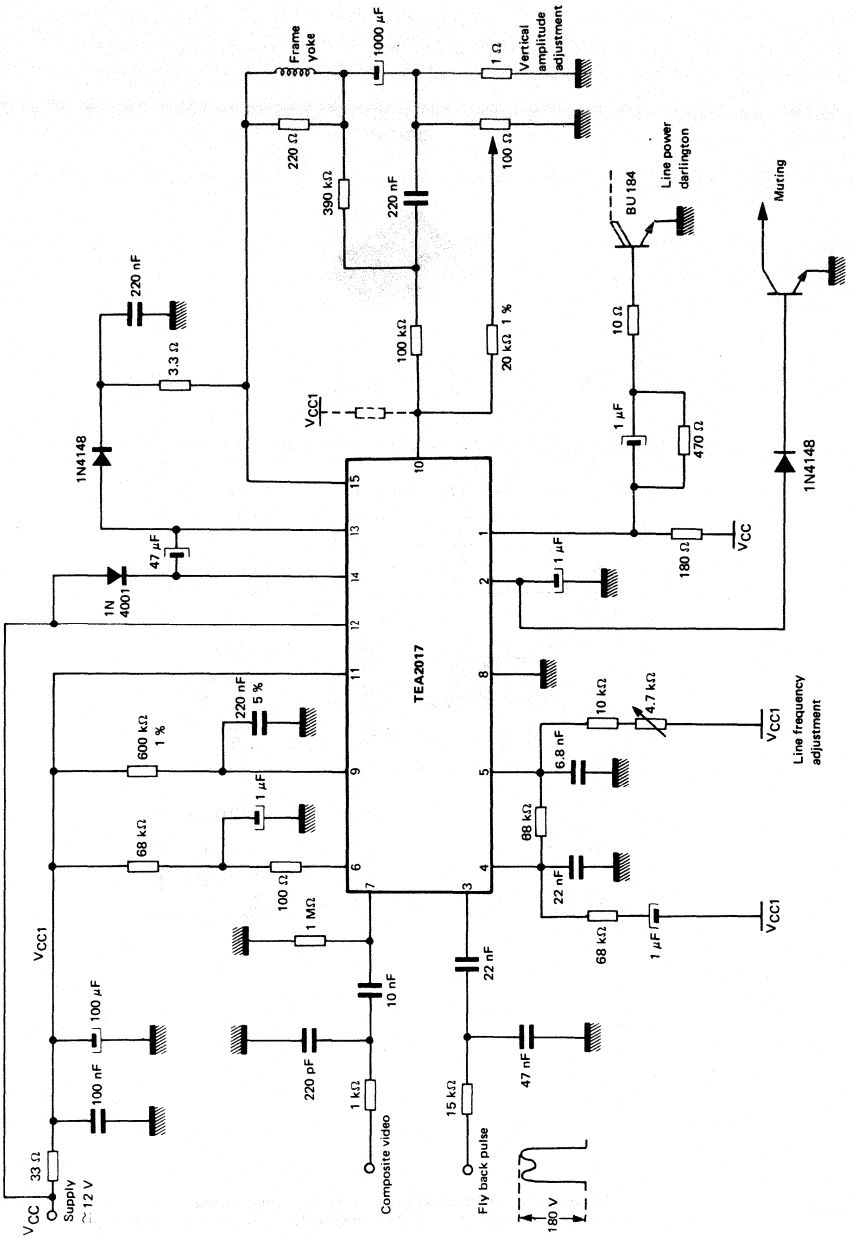
(with yoke L = 27 mH, R = 15 Ω, Ipp = 0.5 A)



VCC2 : Power stage supply from high voltage transformer.
VCC1 must be perfectly filtered.

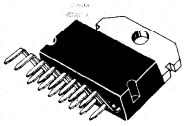
APPLICATION No. 2 (WITH INTERNAL FLYBACK GENERATOR)

TYPICAL BLACK-WHITE TV APPLICATION FOR 14" - 110° SCREEN
(with yoke L = 27 mH, R = 15 Ω, Ipp = 0.5 A)

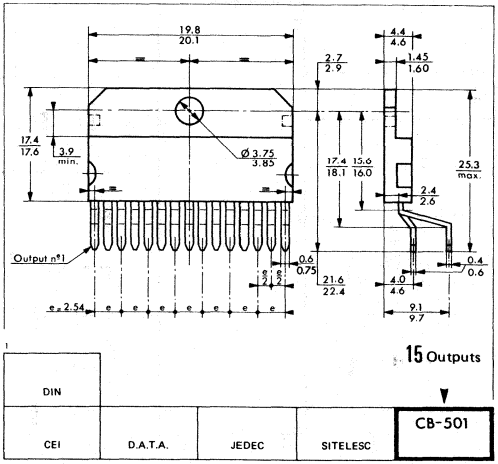


PHYSICAL DIMENSIONS

CB-501



PLASTIC PACKAGE



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HOMSON COMPONENTS
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TEA2026C

COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

The TEA2026C is a complete (horizontal and vertical) deflection processor with secondary step up SMPS control for color TV sets.

Deflection :

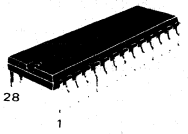
- Ceramic 500 KHz resonator frequency reference.
- No line and frame oscillator adjustment.
- Dual PLL for line deflection.
- High performance synchronization.
- Super sandcastle output.
- Video identification circuit.
- Automatic 50/60 Hz standard identification.
- Excellent interlacing control.
- Special patented frame synchro device for VCR operation.
- Frame saw-tooth generator.
- Frame phase modulator for thyristor.

SMPS Control :

- Error amplifier and phase modulator.
- Synchronization with horizontal deflection.
- Line frequency operation
- Security circuit and start-up processor.
- Switching power transistor is turned off by line fly back signal.

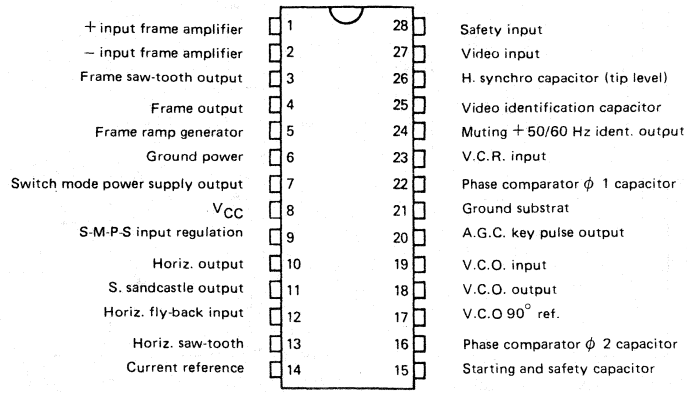
COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

CASE CB-132



PLASTIC PACKAGE

PIN ASSIGNMENT



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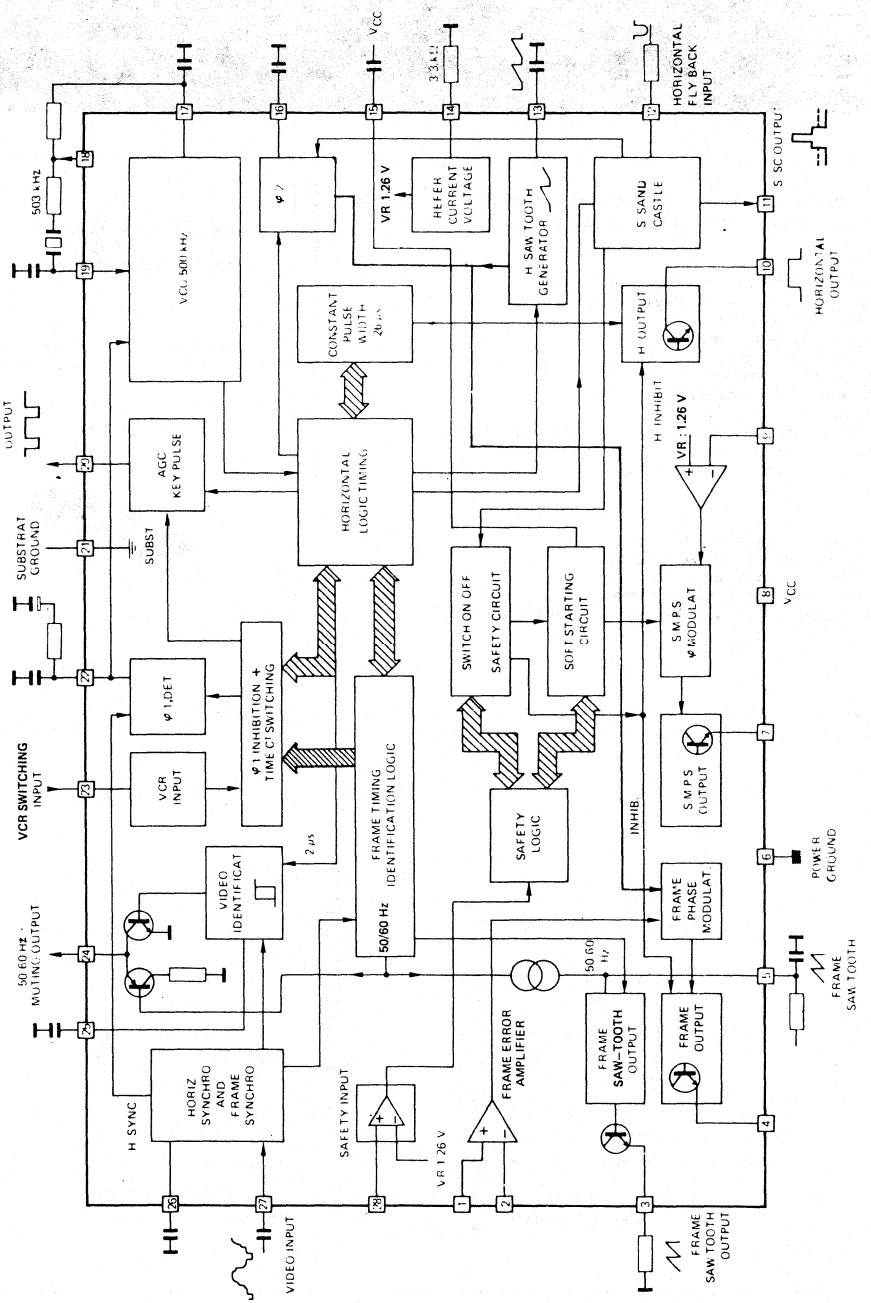
BLOCK DIAGRAM



MAXIMUM RATINGS (Limiting values) - $T_{amb} = 25°C$ (unless otherwise noted)

Rating	Symbol	Min	Max	Unit
Supply voltage (Pin 8)		–	14	V
Operating supply voltage (Pin 8)	V_{CC}	Starting threshold	13.2	V
AGC current (Pin 20)	I_{20}	–	5	mA
Video identification current (Pin 24)	I_{24}	–	10	mA
Negative line retrace voltage (Pin 12)	V_{12}	- 20	–	V
Line retrace current (Pin 12)	I_{12}	–	+ 10	mA
Line output current (Pin 10)	I_{10}	- 10	40	mA
Frame saw-tooth generator (Pin 3)	I_3	–	20	mA
Frame output current (Pin 4)	I_4	–	100	mA
SMPS output current (Pin 7)	I_7	- 40	40	mA
Safety input current (Pin 28)	I_{28}	–	5	mA
Safety input voltage (Pin 28)	V_{28}	–	V_{CC}	–
Common mode range (Pins 1–2)	V_1 / V_2	–	10	V

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction ambiant thermal resistance	$R_{th(j-a)}$	55	°C/W

GENERAL DESCRIPTION

INTRODUCTION

This integrated circuit uses I^2L bipolar technology and combines analog signal processing with digital processing.

Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500 kHz by means of a facheap ceramic resonator. This avoids the frequency adjustment normally required with line and frame oscillators.

A chain of dividers and appropriate logic circuitry produce very accurately defined sampling pulses and the necessary timing signals.

The principal functions implemented are :

- Horizontal scanning processor.
- Frame scanning processor : Two applications are possible :
  - – D Class Power stage using an external thyristor.
  - – B Class Power stage using an external power amplifier with fly-back generator such as the TEA 2116 I.C.
- Line and frame synchronization separation.
- Dual phase-locked loop horizontal scanning.
- High performance frame and line synchronization with interlacing control.
- Video identification circuit.
- Super sandcastle.
- Automatic 50-60 Hz standard identification.
- VCR input for PLL time constant and frame synchro switching.
- AGC key pulse output.
- Frame saw-tooth generator and phase modulator.
- Switching mode regulated power supply comprising error amplifier and phase modulator.
- Security circuit and start-up processor.
- 500 KHz VCO

The circuit is supplied in a 28 pin CB-132 case.

$V_{CC} = 12$ V.

SYNCHRONIZATION SEPARATOR

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.

The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signals in noise conditions.

FRAME SYNCHRONIZATION

Frame synchronization is fully integrated (no external capacitor required).

The frame timing identification logic permits automatic adaptation to 50 - 60 Hz standards or non-interlaced video.

An automatic synchronization window width system provides:

- fast frame capture (6.7 ms wide window),
- good noise immunity (0.4 ms narrow window).

The internal generator starts the discharge of the saw-tooth generator capacitor so that it is not disturbed by line fly-back effects.

Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line fly-back.

A 32 μs timing is automatically applied on standardized transmissions, for perfect interlacing.

In VCR mode, the discharge time is controlled by an internal monostable independant of the line frequency and gives a direct frame synchronization.

HORIZONTAL SCANNING

The horizontal scanning frequency is obtained from the 500 KHz VCO.

The circuit uses **two phase-locked loops (PLL)** :

the first one controls the frequency, the second one controls the relative phase of the synchronization and line fly-back signals.

The frequency PLL has two switched time constants to provide :

- capture with a short time constant,
- good noise immunity after capture with a long time constant.

The output pulse has a constant duration of 26 μs, independent of V_{CC} and any delay in switching off the scanning transistor

VIDEO IDENTIFICATION

The horizontal synchronization signal is sampled by a 2 μs pulse within the synchronization pulse. The signal is integrated by an external capacitor.

The identification function provides three different levels :

- 0 V : no video identification
- 6 V : 60 Hz video identification
- 12 V : 50 Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers, and for audio muting.

SUPER SANDCASTLE with 3 levels : burst, line fly back, frame blanking.

In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.

VCR INPUT

This provides for continuous use of the short time constant of the first phase-locked loop (frequency).

In VCR mode, the frame synchronization window widens out to a search window and there is no delay of frame fly-back (direct synchronization).

FRAME SCANNING

Frame saw-tooth generator :

The current to charge the capacitor is automatically switched to 60 Hz operation to maintain constant amplitude.

Frame phase modulator (with two differentiel inputs)

The output signal is a pulse at the line frequency, pulse width modulated by the voltage at the differential pre-amplifier input.

This signal is used to control a thyristor which provides the scanning current to the yoke. The saw-tooth output is a low impedance and can therefore be used in class B operation with a power amplifier circuit.

SWITCH MODE POWER SUPPLY (SMPS) SECONDARY REGULATION

This power supply uses a differential error amplifier with an internal reference voltage of 1.26 V and a phase modulator operating at the line frequency. The power transistor is turned off by the line fly-back

The «soft start» device imposes a very small conduction angle on starting up, this angle progressively increases to its nominal regulation value.

The maximum conduction angle may be monitored by forcing a voltage on pin 15. This pin may also be used for current limitation.

SECURITY CIRCUIT AND START UP PROCESSOR

When the security input (pin 28) is at a voltage exceeding 1.26 V the three outputs are simultaneously cut off until this voltage drops below the 1.26 V threshold again. In this case the switch mode power supply is restarted by the «soft start» system.

If this cycle is repeated three times, the three outputs are cut off definitively. To reset the safety logic circuits V_{CC} must be zero volt.

This circuit eliminates the risk to switch off the TV receiver in the event of a flash affecting the tube.

On starting up, the horizontal and vertical scanning functions come into operation at $V_{CC} = 6$ V. The power supply then comes into operation progressively, only when $\varphi 2$ is normally locked.

On shutting down, the three functions are interrupted simultaneously after the first line fly-back.

ELECTRICAL OPERATING CHARACTERISTICS - $T_{amb} = 25°C$ - $V_{CC} = 12$ V (unless otherwise noted) - Pulse duration at 50 % of the ampl.

Characteristic	Symbol	Min	Typ	Max	Unit
Supply current (pin 8; frame, line and SMPS output without load)	I_{CC}	–	50	80	mA
Synch. separator (pins 26-27)					
Positive video input AC coupled (output impedance of signal source $< 200\ \Omega$)	–	0.2	1.8	3	Vpp
Negative clamping current (during synch. pulse).	$-I_{27}$	25	40	55	μA
Clamping current	I_{27}	3	6	9	μA
Pin for slicing level 0.2 V $< V_{27pp} <$ 2 V. (50 % of sync. amplitude)					
Positive current	$-I_{26}$	0	750	1000	μA
Negative current	I_{26}	17	25	36	μA
Pulse for keyed AGC (pin 20)					
Negative(function: without video signal: low level, with video signal: key pulses)					
Output current	I_{20}	–	–	5	mA
Output saturation voltage ($I_{20} = 5$ mA)	V_{20}	–	0.25	0.4	V
Pulse width (synchro pulse is always inside the key pulse)	t_k	6.5	8	8.5	μs
VCO (pins 17-18 and 19)					
Frequency control range after line divider (ceramic resonator : 503 kHz)	–	15.30 to 16.10	–	–	kHz
Phase comparator φ1 (pin 22)					
Output current low loop gain high loop gain	– –	± 0.35 ± 1	± 0.50 ± 1.5	± 0.65 ± 2	mA mA
Window pulse width	–	7	10	13	μs
VCR switching (pin 23)					
Threshold voltage VCR operating	–	1.7	2.2	2.7	V
Input current ($V_{23} = 0$, $V_{CC} = 12$ V)	I_{23}	- 0.030	- 0.25	- 1	mA
Video identification (pin 24)					
Output saturation voltage (without video signal, $I_{24} = 3$ mA)	V_{24}	–	0.2	0.6	V
Output voltage (with 60 Hz video signal, $I_{24} = 2.5$ mA)	–	5	6.5	7.5	V
Output voltage (with 50 Hz video signal, $I_{24} = 10\ \mu A$)	–	11.0	11.5	–	V
Video identification (pin 25)					
Output current (charging the capacitor)	I_{25}	0.5	0.75	1	mA
Identification time (charging the capacitor)	t_{25}	1.3	1.7	2.2	μs
Threshold (voltage changing from lower to higher value)	V_{25}	4	4.5	5	V
Hysteresis	L_{HYS}	150	240	400	mV
H-ramp generator (pin 13)					
Charge current	I_{ch13}	185	200	215	μA
Base voltage of saw-tooth	V_{I13}	–	–	0.5	V
Discharge current	I_{dis13}	3.5	7.0	–	mA
Super sandcastle (pin 11)					
Output voltages					
Burst key pulse level ($I_{11} = -5$ mA)	V_{B11}	9	–	–	V
Line blanking pulse level ($I_{11} = -5$ mA)	V_{L11}	4	4.5	5	V
Frame blanking pulse level (and frame out of function)-($I_{11} = -5$ mA)	V_{BT11}	2	2.5	3	V

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

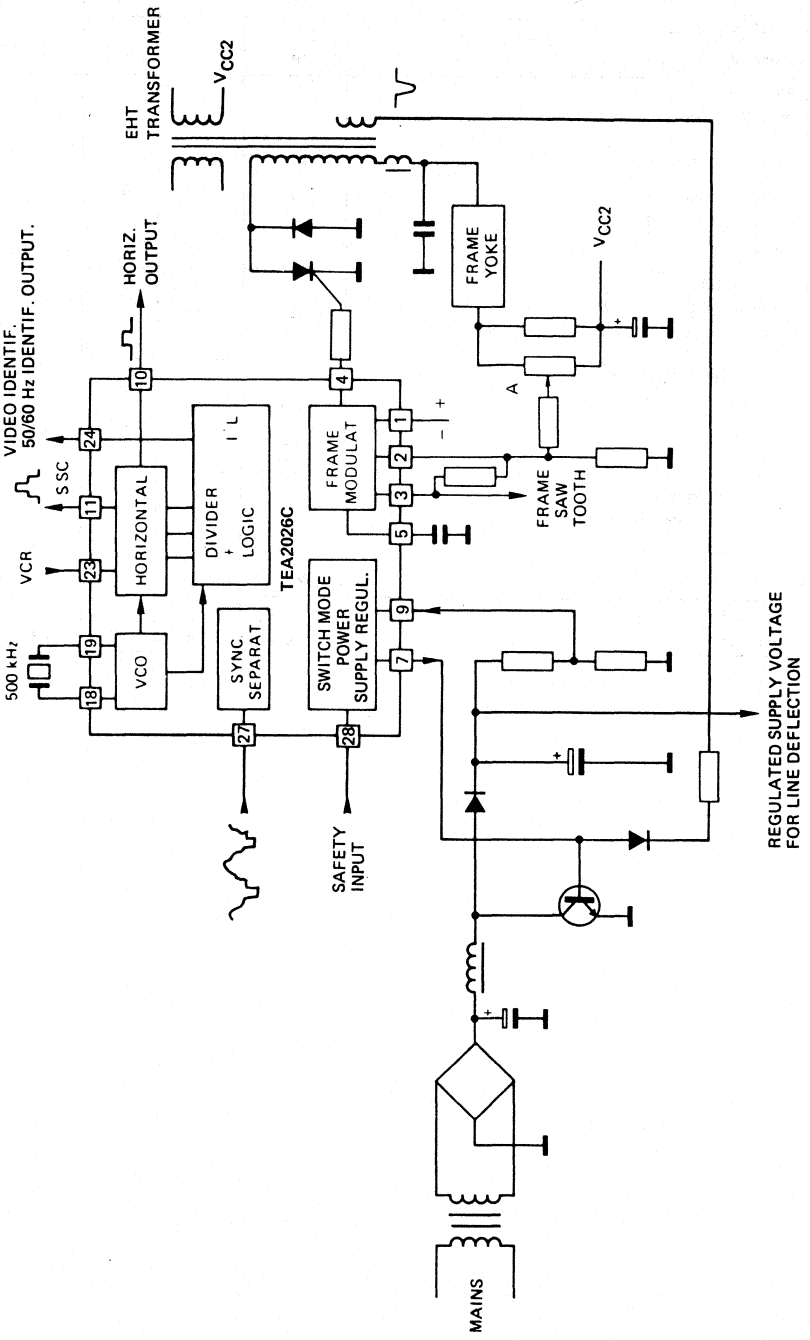
Characteristic	Symbol	Min	Typ	Max	Unit
Super sandcastle (continued)					
Delay between middle of synch. pulse (pin 27) and leading edge of burst key pulse	T_{B11}	2.3	–	3.0	µs
Duration of burst key pulse	–	3.7	4	5	µs
Delay between SSC cutting level at pin 12 and line blanding pulse	T_{O11}	–	–	0.35	µs
Frame blanking time (start with reset of frame divider)	–	21	–	24	Line
Negative line fly back input (pin 12)					
Threshold for SMPS safety	–	1.1	–	–	V
Threshold for blanking	V_{bl12}	11	11.5	12	V
Threshold for PLL2	$V_{\varphi 12}$	- 1	–	–	V
Input current $11\ V < V_{12}$	I_{12}	–	–	- 200	µA
Input current $1.3\ V < V_{12} < 11\ V$	I_{12}	- 3	–	+ 3	µA
Input current $0\ V < V_{12} < 1.3\ V$	I_{12}	0	–	- 80	µA
Input current $-1\ V < V_{12} < 0\ V$	I_{12}	0	- 1	- 2	mA
Line blanking trigger	–	–	–	80	µA
Phase comparator $\varphi 2$ (pin 16)					
Charging current	I_{16}	0.4	0.6	0.8	mA
Delay between the edges of $\varphi 1$ and $\varphi 2$ ($f_{VCO} = 500$ kHz)	–	1.5	2	2.8	µs
Line output (open collector) - (pin 10)					
Output voltage ($I_{10\ max} = 20$ mA)	–	–	1	1.5	V
Output pulse duration (when fly-back pulse is with in time T_{10}) ($f_{VCO} = 500$ kHz)	T_{10}	24	26	30	µs
$\varphi 2$ phase range	$\Delta\tau$	15	16	19	µs
Frame logic					
Free running period (with mute signal)	–	–	315	–	Line
Search window	–	247	–	361	Line
50 Hz window	–	309	–	315	Line
60 Hz window	–	247	–	276	Line
VCR mode window	–	247	–	361	Line
Frame saw-tooth generator (pins 3-5)					
Saw-tooth amplitude	–	2	3	4	Vpp
Internal current generator (60 Hz on)	$I_5(60)$	12	14	16	µA
Discharging time (with C= 0.47 µF, $\Delta V < 4$ V)	–	50	–	70	µs
Starting level ($0 < I_s < 10$ mA)	V_s	1	1.26	1.4	V
Saw-tooth amplitude ($I_s = 10$ mA)	–	2	3	4	Vpp
Frame feedback inputs (Pins 1-2)					
Positive and negative input current ($V_1 - V_2 > 25$ mA for frame blanking safety)	$I_{1,2}$	–	–	10	µA
Frame output (Pin 4)					
Output voltage ($0\ V < \lvert I_4 \rvert < 80$ mA)	–	10	–	–	V
$T_{ON\ max}$ ($f_{VCO} = 500$ kHz)	–	36	40	41	µs
Output phase range	–	0	–	$t_{ON\ max}$	–

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

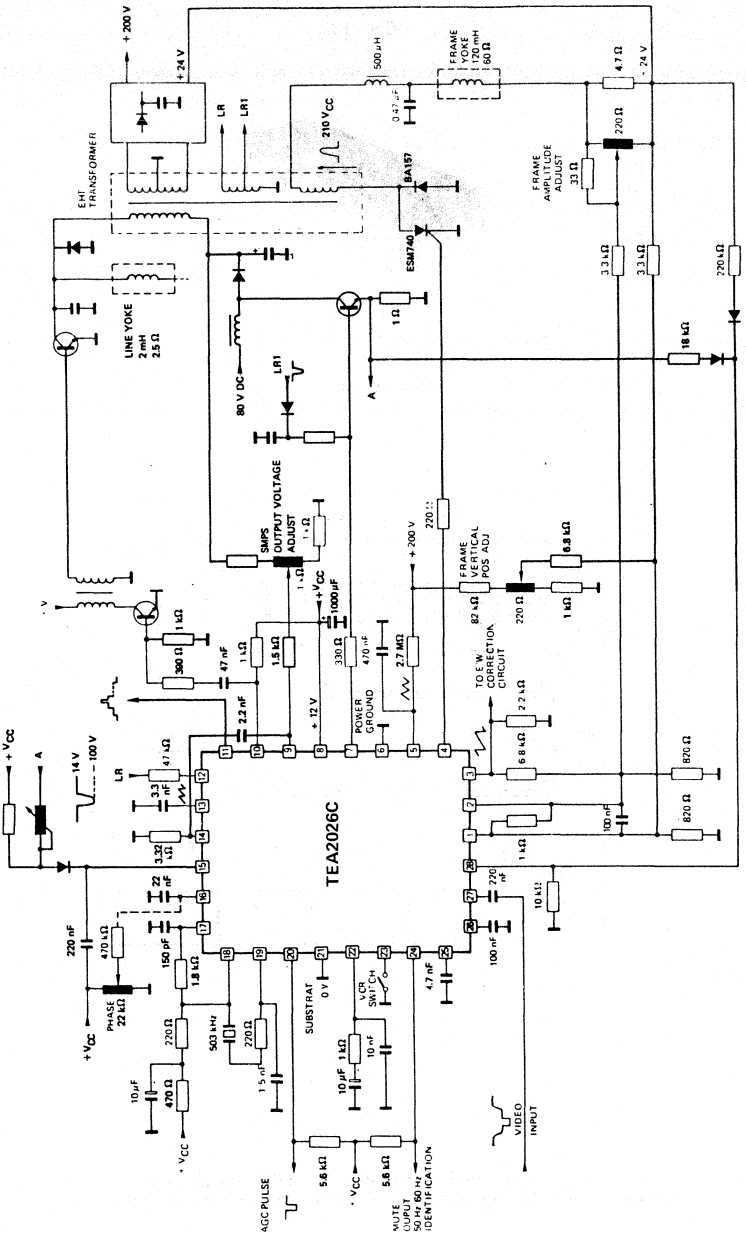
Characteristic	Symbol	Min	Typ	Max	Unit
SMPS control input (pin 9)					
Input current ($V_9 = V_{ref\ 14}$)	I_9	–	–	2	μA
SMPS output (pin 7)					
End of SMPS pulse (pin 7) and leading edge of line fly-back (pin 12) in phase					
Output voltage ($0 < I_7 < 20$ mA)	V_7	10	–	–	V
$t_{ON\ max}$ ($f_{VCO} = 500$ kHz)	T_7	30	32	34	μs
Nominal time ($V_9 = V_{ref\ 14}$)	–	26	–	31	μs
Output phase range	–	0	–	$t_{ON\ max}$	–
Safety input (pin 28)					
Threshold voltage ($V_{28} = V_{ref14}$)	V_{28}	1.15	1.26	1.37	V
Input current (if $V_{28} > V_{ref\ 14}$ then SMPS, line and frame are switched off during the next line retrace)	–	–	–	3	μA
Switch-on, switch-off processing (pin 15)					
Charging current ($t_c = 4$ μs, $T = 64$ μs)	I_{ch15}	70	–	130	μA
Ratio charging/discharging	$\frac{I_{ch15}}{I_{dis15}}$	0.8	1	1.2	–
Starting supply voltage (pin 8)					
SMPS*, frame and line starting (pin 7, 10, 4)	V_{CC}	5.25	–	6.5	V
SMPS stopping during line retrace	V_{CC}	5.25	–	6.5	V
Frame and line stopping	V_{CC}	5.25	–	6.5	V
Current reference (pin 14)					
Voltage reference	V_{ref14}	1.2	1.26	1.35	V

* Progressive starting by decreasing V_{15}

SIMPLIFIED APPLICATION DIAGRAM

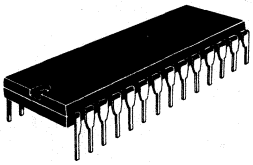


APPLICATION CIRCUIT
(WITH THYRISTOR FRAME POWER)

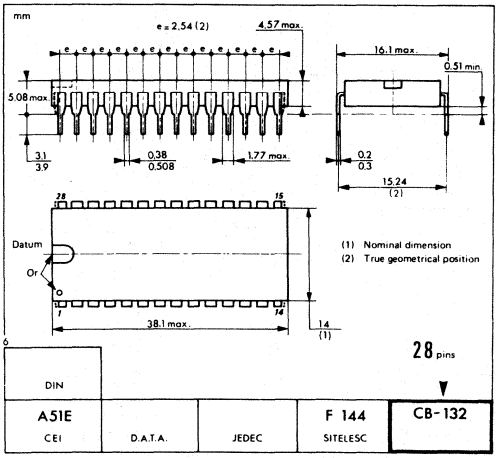


PHYSICAL DIMENSIONS

CB - 132



PLASTIC PACKAGE



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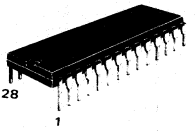
- No line and frame oscillator adjustment reference
- Dual PLL for line deflection.
- High performance synchronization.
- Super sandcastle output.
- Frame blanking with safety circuit.
- Video identification circuit.
- Automatic 50/60 Hz standard identification.
- Excellent interlacing control.
- Special patented frame synchro device for VCR operation.
- Frame saw-tooth generator.

SMPS Control :

- Error amplifier and phase modulator
- Synchronization with horizontal deflection
- Security circuit and start-up processor .
- Output pulses are sent to the primary SMPS IC (TEA2162) through a low cost synchro pulse transformer.

COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

CASE CB-132



PLASTIC PACKAGE

PIN ASSIGNMENT

NC	1	28	Safety input
Safety frame blanking input	2	27	Video input
Frame saw-tooth output	3	26	H. synchro capacitor (tip level)
Frame blanking output	4	25	Video identification capacitor
Frame ramp generator	5	24	Muting + 50/60 Hz ident. output
Ground power	6	23	V.C.R. input
Switch mode power supply output	7	22	Phase comparator ϕ 1 capacitor
V_{CC}	8	21	Ground substrat
S-M-P-S input regulation	9	20	A.G.C. key pulse output
Horiz. output	10	19	V.C.O. input
S. sandcastle output	11	18	V.C.O. output
Horiz. fly-back input	12	17	V.C.O 90° ref.
Horiz. saw-tooth	13	16	Phase comparator ϕ 2 capacitor
Current reference	14	15	Starting and safety capacitor

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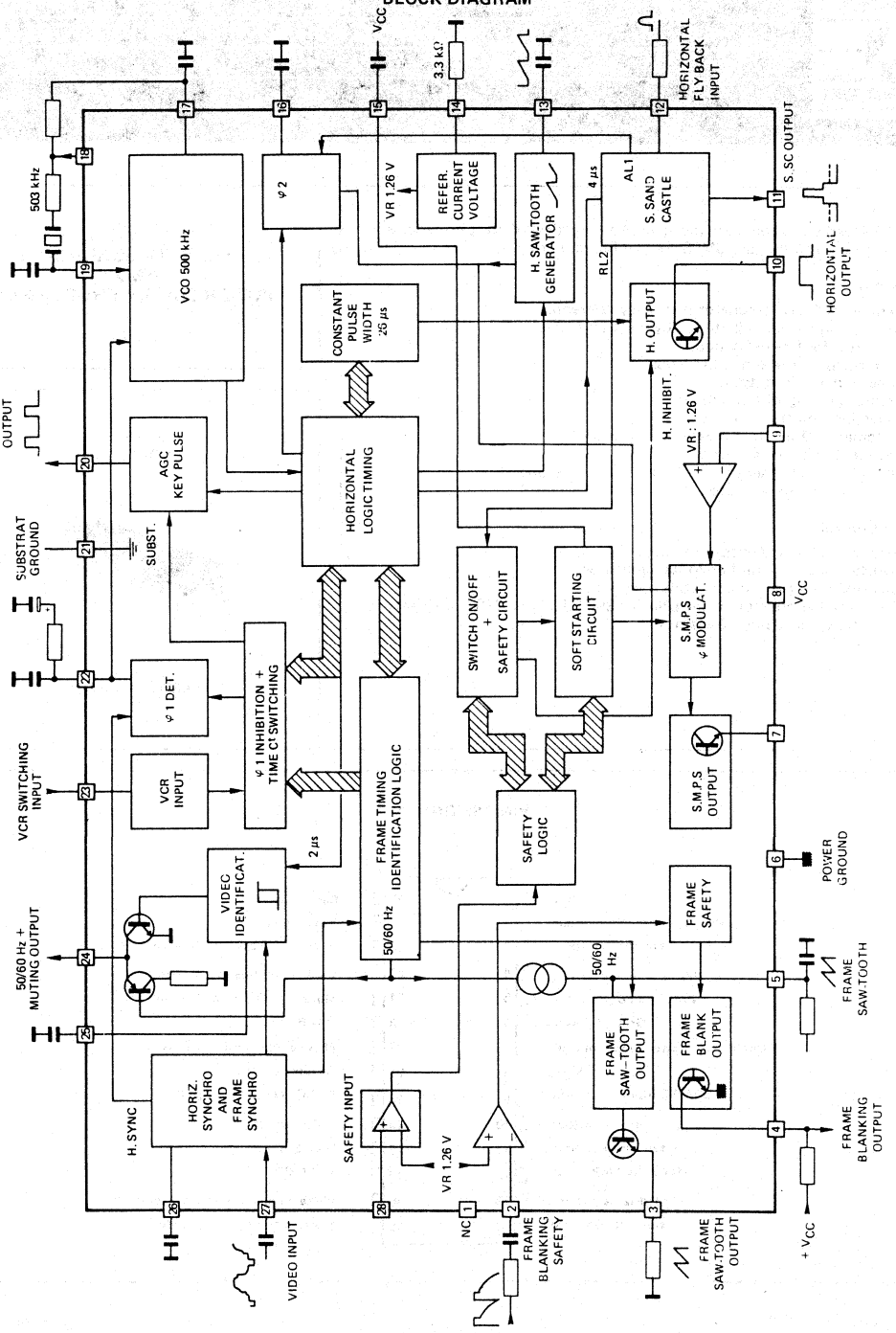
BLOCK DIAGRAM



MAXIMUM RATINGS (Limiting values) - T_{amb} = 25°C (unless otherwise noted)

Rating	Symbol	Min	Max	Unit
Supply voltage (Pin 8)		–	14	V
Operating supply voltage (Pin 8)	V_{CC}	Starting threshold	13.2	V
AGC current (Pin 20)	I_{20}	–	5	mA
Video identification current (Pin 24)	I_{24}	–	10	mA
Negative line retrace voltage (Pin 12)	V_{12}	- 20	–	V
Line retrace current (Pin 12)	I_{12}	–	+ 10	mA
Line output current (Pin 10)	I_{10}	- 10	40	mA
Frame saw-tooth generator (Pin 3)	I_3	–	20	mA
Frame blanking input current (Pin 4)	I_4	–	100	mA
SMPS output current (Pin 7)	I_7	- 40	40	mA
Safety input current (Pin 28)	I_{28}	–	5	mA
Safety input voltage (Pin 28)	V_{28}	–	V_{CC}	–

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction ambiant thermal resistance	$R_{th(j-a)}$	55	°C/W

GENERAL DESCRIPTION

INTRODUCTION

This integrated circuit uses I²L bipolar technology and combines analog signal processing with digital processing.

Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500 kHz by means of a cheap ceramic resonator. This avoids the frequency adjustment normally required with line and frame oscillators.

A chain of dividers and appropriate logic circuitry produce very accurately defined sampling pulses and the necessary timing signals.

The principal functions implemented are :

- Horizontal scanning processor.
- Frame scanning processor.
  - B Class Power stage using an external power amplifier with fly back generator such as the TEA 2116 I.C.
- Secondary switch mode power regulation.
  The SMPS output synchronize a primary I.C. (TEA 2162) at the mains part.
  This concept allows ACTIVE STANDBY facilities.
- Line and frame synchronization separation.
- Dual phase-locked loop horizontal scanning.
- High performance frame and line synchronization with interlacing control.
- AGC key pulse output
- Video identification circuit.
- Super sandcastle.
- Automatic 50-60 Hz standard identification.
- VCR input for PLL time constant and frame synchro switching.
- Frame saw-tooth generator.
- Frame blanking output.
- Switching mode regulated power supply comprising error amplifier and phase modulator.
- Security circuit and start-up processor.
- 500 KHz VCO.

The circuit is supplied in a 28 pin CB-132 case.

V_{CC} = 12 V.

SYNCHRONIZATION SEPARATOR

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.

The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signals in noise conditions.

FRAME SYNCHRONIZATION

Frame synchronization is fully integrated (no external capacitor required).

The frame timing identification logic permits automatic adaptation to 50 - 60 Hz standards or non-interlaced video.

An automatic synchronization window width system provides:

- fast frame capture (6.7 ms wide window),
- good noise immunity (0.4 ms narrow window).

The internal generator starts the discharge of the saw-tooth generator capacitor so that it is not disturbed by line fly-back effects.

Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line fly-back.

A 32 μs timing is automatically applied on standardized transmissions, for perfect interlacing.

In VCR mode, the discharge time is controlled by an internal monostable independant of the line frequency and gives a direct frame synchronization.

HORIZONTAL SCANNING

The horizontal scanning frequency is obtained from the 500 KHz VCO.

The circuit uses two phase-locked loops (PLL) :

the first one controls the frequency, the second one controls the relative phase of the synchronization and line fly-back signals.

The frequency PLL has two switched time constants to provide :

- capture with a short time constant,
- good noise immunity after capture with a long time constant.

The output pulse has a constant duration of 26 μs, indépendent of V_{CC} and any delay in switching off the scanning transistor

VIDEO IDENTIFICATION

The horizontal synchronization signal is sampled by a 2 μs pulse within the synchronization pulse. The signal is integrated by an external capacitor.

The identification function provides three different levels :

- 0 V : no video identification
- 6 V : 60 Hz video identification
- 12 V : 50 Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers and for audio muting.

SUPER SANDCASTLE with 3 levels : burst, line fly back, frame blanking.

In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.

VCR INPUT

This provides for continuous use of the short time constant of the first phase-locked loop (frequency).

In VCR mode, the frame synchronization window widens out to a search window and there is no delay of frame fly-back (direct synchronization).

FRAME SCANNING

Frame saw-tooth generator

The current to charge the capacitor is automatically switched to 60 Hz operation to maintain constant amplitude.

SWITCH MODE POWER SUPPLY (SMPS) SECONDARY TO PRIMARY REGULATION

This power supply uses a differential error amplifier with an internal reference voltage of 1.26 V and a phase modulator operating at the line frequency. The power transistor is turned off by the falling edge of the horizontal saw-tooth.

The «soft start» device imposes a very small conduction angle on starting up, this angle progressively increases to its nominal regulation value.

The maximum conduction angle may be monitored by forcing a voltage on pin 15. This pin may also be used for current limitation.

The output pulse is sent to the primary I.C. (TEA 2162) via a low cost synchro transformer.

SECURITY CIRCUIT AND START UP PROCESSOR

When the security input (pin 28) is at a voltage exceeding 1.26 V the three outputs are simultaneously cut off until this voltage drops below the 1.26 V threshold again. In this case the switch mode power supply is restarted by the «soft start» system.

If this cycle is repeated three times, the three outputs are cut off definitively. To reset the safety logic circuits, V_{CC} must be zero volt.

This circuit eliminates the risk to switch off the TV receiver in the event of a flash affecting the tube.

On starting up the horizontal scanning function comes into operation at $V_{CC} = 6$ V. The power supply then comes into operation progressively.

On shutting down, the two functions are interrupted simultaneously after the first line fly back.

FRAME BLANKING SAFETY (PIN 2)

The frame blanking safety checks the normal of frame scanning.

In case of any problem pin 4 is at a ligh level (frame blanking) in order to protect the tube.

ELECTRICAL OPERATING CHARACTERISTICS - $T_{amb} = 25°C$ - $V_{CC} = 12$ V (unless otherwise noted) - Pulse duration at 50 % of the ampl.

Characteristic	Symbol	Min	Typ	Max	Unit
Supply current (pin 8; frame, line and SMPS output without load)	I_{CC}	–	50	80	mA
Synch. separator (pins 26-27)					
Positive video input AC coupled (output impedance of signal source $< 200\ \Omega$)	–	0.2	1.8	3	Vpp
Negative clamping current (during synch. pulse).	$-I_{27}$	- 25	- 40	- 55	µA
Clamping current	I_{27}	3	6	9	µA
Pin for slicing level 0.2 V $< V_{27pp} <$ 2 V, (50 % of sync. amplitude)					
Positive current	$-I_{26}$	0	- 750	- 1000	µA
Negative current	I_{26}	17	25	36	µA
Pulse for keyed AGC (pin 20)					
Positive (function: without video signal: high level, with video signal: key pulses)					
Output current	I_{20}	–	–	5	mA
Output saturation voltage ($I_{20} = 5$ mA)	V_{20}	–	0.25	0.4	V
Pulse width (synchro pulse is always inside the key pulse)	t_k	6.5	8	8.5	µs
VCO (pins 17-18 and 19)					
Frequency control range after line divider (ceramic resonator : 503 kHz)	–	15.30 to 16.10	–	–	kHz
Phase comparator $\varphi 1$ (pin 22)					
Output current low loop gain	–	± 0.35	± 0.50	± 0.65	mA
high loop gain	–	± 1	± 1.5	± 2	mA
Window pulse width	–	7	10	13	µs
VCR switching (pin 23)					
Threshold voltage VCR operating	–	1.7	2.2	2.7	V
Input current ($V_{23} = 0$, $V_{CC} = 12$ V)	I_{23}	- 0.030	- 0.25	- 1	mA
Video identification (pin 24)					
Output saturation voltage (without video signal, $I_{24} = 3$ mA)	V_{24}	–	0.2	0.6	V
Output voltage (with 60 Hz video signal, $I_{24} = 2.5$ mA)	–	5	6.5	7.5	V
Output voltage (with 50 Hz video signal, $I_{24} = 10$ µA)	–	11.0	11.5	- 1	V
Video identification (pin 25)					
Output current (charging the capacitor)	I_{25}	0.5	0.75	1	mA
Identification time (charging the capacitor)	t_{25}	1.3	1.7	2.2	µs
Threshold (voltage changing from lower to higher value)	V_{25}	4	4.5	5	V
Hysteresis	L_{HYS}	–	350	–	mV
H-ramp generator (pin 13)					
Charge current	I_{ch13}	185	200	215	µA
Base voltage of saw-tooth	V_{I13}	–	–	0.5	V
Discharge current	I_{dis13}	3.5	7.0	–	mA
Super sandcastle (pin 11)					
Output voltages					
Burst key pulse level ($I_{11} = -5$ mA)	V_{B12}	9	–	–	V
Line blanking pulse level ($I_{11} = -5$ mA)	V_{L12}	4	4.5	5	V
Frame blanking pulse level (and frame out of function)-($I_{11} = -5$ mA)	V_{BT12}	2	2.5	3	V

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

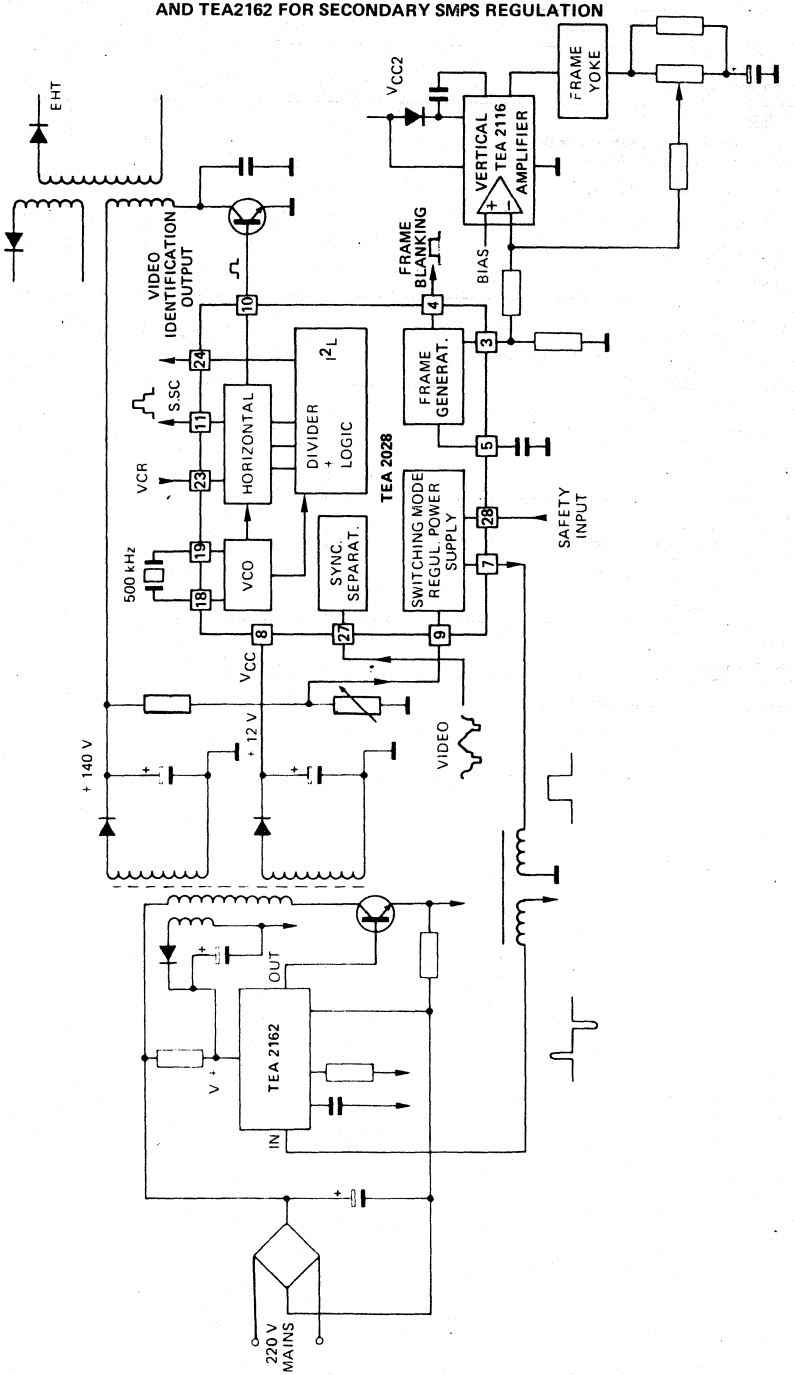
Characteristic	Symbol	Min	Typ	Max	Unit
Super sandcastle (continued)					
Delay between middle of synch. pulse (pin 27) and leading edge of burst key pulse	T_{B11}	2.3	–	3.0	µs
Duration of burst key pulse	–	3.7	4	5	µs
Delay between SSC cutting level at pin 12 and line blanding pulse	T_{O11}	–	–	0.35	µs
Frame blanking time (start with reset of frame divider)	–	21	–	24	Line
Positive line fly back input (pin 12)					
Threshold for SMPS safety	–	1.1	–	–	V
Threshold for blanking	V_{bl12}	–	0.3	–	V
Threshold for PLL2	$V_{\varphi 12}$	–	3	–	V
Input current $-0.4\ V < V_{12} < V_{bl12}$	I_{12}	–	- 20	–	µA
Input current $V_{bl12} < V_{12} < V_{\varphi 12}$	I_{12}	–	- 10	–	µA
Input current $V_{\varphi 12} < V_{12} < V_{CC}$	I_{12}	0	–	1	µA
Phase comparator $\varphi 2$ (pin 16)					
Charging current	I_{16}	0.4	0.6	0.8	mA
Delay between the edges of $\varphi 1$ and $\varphi 2$ ($f_{VCO} = 500$ kHz)	–	1.5	2	2.8	µs
Line output (open collector) (pin 10)					
Output voltage ($I_{10\ max} = 20$ mA)	–	–	1	1.5	V
Output pulse duration (when fly-back pulse is with in time T_{10}) ($f_{VCO} = 500$ kHz)	T_{10}	24	26	30	µs
$\varphi 2$ phase range	Δt	15	16	19	µs
Frame logic					
Free running period (with mute signal)	–	–	315	–	Line
Search window	–	247	–	361	Line
50 Hz window	–	309	–	315	Line
60 Hz window	–	247	–	276	Line
VCR mode window	–	247	–	361	Line
Frame saw-tooth generator (pins 3-5)					
Saw-tooth amplitude	–	2	3	4	Vpp
Internal current generator (60 Hz on)	$I_5(60)$	12	14	16	µA
Discharging time (with $C = 0.47$ µF, $\Delta V < 4$ V)	–	50	–	70	µs
Starting level ($0 < I_s < 10$ mA)	V_s	1	1.26	1.4	V
Saw-tooth amplitude ($I_s = 10$ mA)	–	2	3	4	Vpp
Frame blanking safety input (pin 2)					
Threshold voltage	–	1.15	1.26	1.37	V
Frame blanking output (open collector) - (pin 4)					
Output saturation voltage ($I_4 = 5$ mA)	–	–	–	0.4	V
Output current (low level)	–	–	–	10	mA
Blanking time	–	–	21	–	Line

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

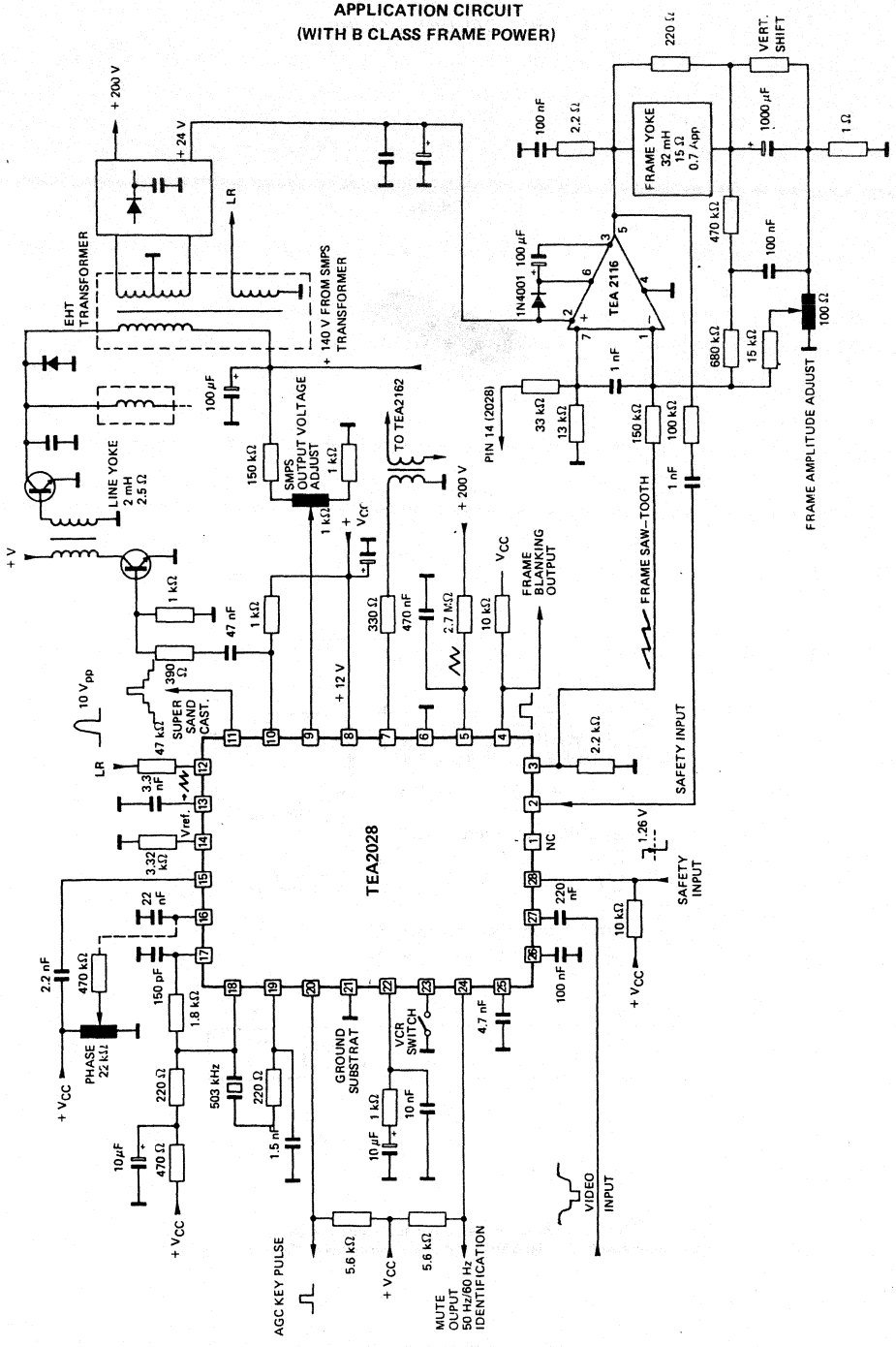
Characteristic	Symbol	Min	Typ	Max	Unit
SMPS control input (pin 9)					
Input current ($V_9 = V_{ref\ 14}$)	I_9	–	–	2	μA
SMPS output (pin 7)					
No relation between end of SMPS pulse (pin 7) and leading edge of line fly back (pin 12)					
Output voltage ($0 < I_7 < 20$ mA)	V_7	10	–	–	V
t_{ON} max ($f_{VCO} = 500$ kHz)	T_7	30	32	34	μs
Nominal time ($V_9 = V_{ret\ 14}$)	–	26	–	31	μs
Output phase range	–	0	–	t_{ON} max	–
Safety input (pin 28)					
Threshold voltage ($V_{28} = V_{ref14}$)	V_{28}	1.15	1.26	1.37	V
Input current (if $V_{28} > V_{ref\ 14}$ then SMPS, line and frame are switched off during the next line retrace)	–	–	–	3	μA
Switch-on, switch-off processing (pin 15)					
Charging current ($t_c = 4$ μs, $T = 64$μs)	I_{ch15}	70	–	130	μA
Ratio charging/discharging	$\frac{I_{ch15}}{I_{dis15}}$	0.8	1	1.2	–
Starting supply voltage (pin 8)					
SMPS*, frame and line starting (pins 7, 10 and 4)	V_{CC}	5.25	–	6.5	V
SMPS stopping during line retrace	V_{CC}	5.25	–	6.5	V
Frame and line stopping	V_{CC}	5.25	–	6.5	V
Current reference (pin 14)					
Voltage reference	V_{ref14}	1.2	1.26	1.35	V

* Progressive starting by decreasing V_{15}

APPLICATION WITH TEA2116 FOR B CLASS FRAME POWER AND TEA2162 FOR SECONDARY SMPS REGULATION

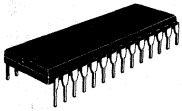


APPLICATION CIRCUIT
(WITH B CLASS FRAME POWER)

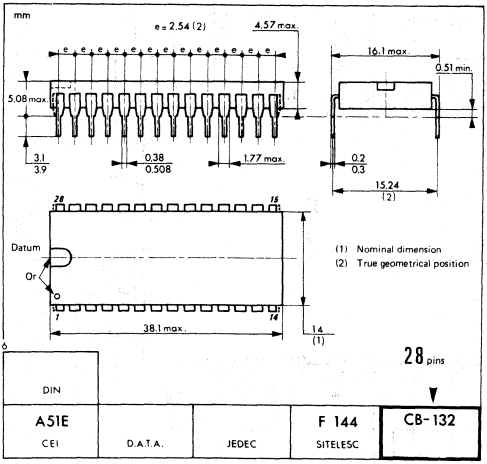


PHYSICAL DIMENSIONS

CB-132



PLASTIC PACKAGE



These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

HOMSON COMPONENTS EMICONDUCTEURS

TEA2029C

COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

The TEA2029C is a complete (horizontal and vertical) deflection processor with secondary to primary SMPS control for color TV sets.

Deflection :

- Ceramic 500 KHz resonator frequency reference.
- No line and frame oscillator adjustment.
- Dual PLL for line deflection.
- High performance synchronization.
- Super sandcastle output.
- Video identification circuit.
- Automatic 50/60 Hz standard identification.
- Excellent interlacing control.
- Special patented frame synchro device for VCR operation.
- Frame saw-tooth generator.
- Frame phase modulator for thyristor.

SMPS Control :

- Error amplifier and phase modulator.
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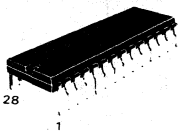
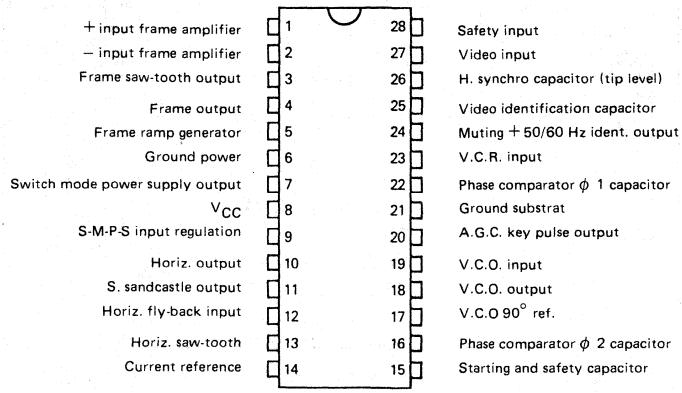
COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

CASE CB-132



PLASTIC PACKAGE

PIN ASSIGNMENT



JUNE 1986 – 1/14

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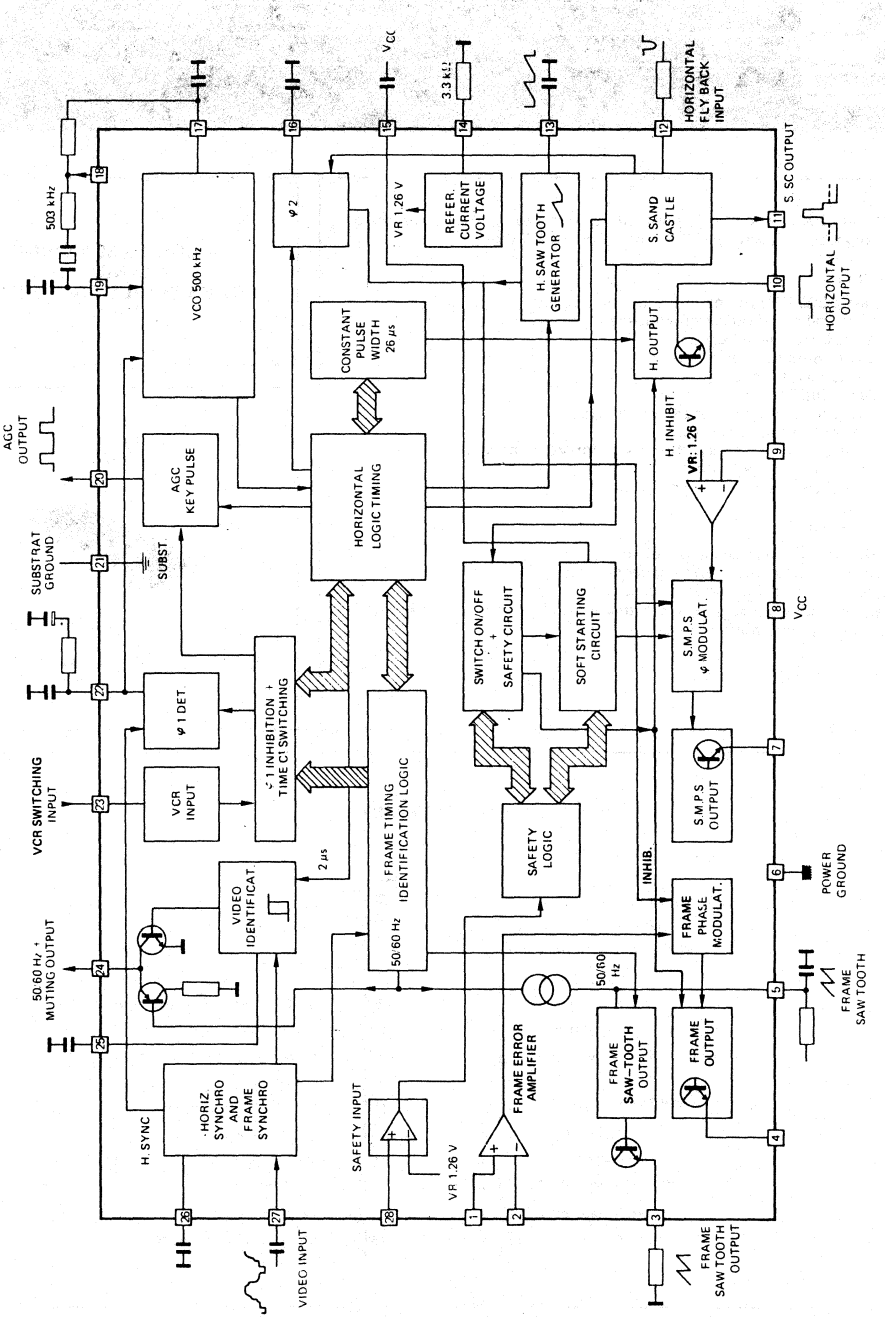

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Frame output current (Pin 4)	I_4	–	100	mA
SMPS output current (Pin 7)	I_7	- 40	40	mA
Safety input current (Pin 28)	I_{28}	–	5	mA
Safety input voltage (Pin 28)	V_{28}	–	V_{CC}	–
Common mode range (Pins 1–2)	V_1/V_2	–	10	V

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
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GENERAL DESCRIPTION

This integrated circuit uses I^2L bipolar technology and combines analog signal processing with digital processing.

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- Horizontal scanning processor.
- Frame scanning processor. Two applications are possible :
  - D Class Power stage using an external thyristor.
  - B Class Power stage using an external power amplifier with fly-back generator such as the TEA 2116 I.C.
- Secondary switch mode power regulation.
  The SMPS output synchronize a primary I.C. (TEA 2162) at the mains part.
  This concept allows ACTIVE STANDBY facilities.
- Dual phase-locked loop horizontal scanning.
- High performance frame and line synchronization with interlacing control.
- Video identification circuit.
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- AGC key pulse output.
- Automatic 50-60 Hz standard identification.
- VCR input for PLL time constant and frame synchro switching.
- Frame saw-tooth generator and phase modulator.
- Switching mode regulated power supply comprising error amplifier and phase modulator.
- Security circuit and start-up processor.
- 500 KHz VCO

The circuit is supplied in a 28 pin CB-132 case.

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The output pulse has a constant duration of 26 µs, independent of V_{CC} and any delay in switching off the scanning transistor

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This provides for continuous use of the short time constant of the first phase-locked loop (frequency).

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FRAME SCANNING

Frame saw-tooth generator

The current to charge the capacitor is automatically switched to 60 Hz operation to maintain constant amplitude.

Frame phase modulator (with two differential inputs)

The output signal is a pulse at the line frequency, pulse width modulated by the voltage at the differential pre-amplifier input.

This signal is used to control a thyristor which provides the scanning current to the yoke. The saw-tooth output is a low impedance, however, and can therefore be used in class B operation with a power amplifier circuit.

SWITCH MODE POWER SUPPLY (SMPS) SECONDARY TO PRIMARY REGULATION

This power supply uses a differential error amplifier with an internal reference voltage of 1.26 V and a phase modulator operating at the line frequency. The power transistor is turned off by the falling edge of the horizontal saw-tooth.

The «soft start» device imposes a very small conduction angle on starting up, this angle progressively increases to its nominal regulation value.

The maximum conduction angle may be monitored by forcing a voltage on pin 15. This pin may also be used for current limitation.

The output pulse is sent to the primary S.M.P.S. I.C. (TEA2162)via a low cost synchro transformer.

SECURITY CIRCUIT AND START UP PROCESSOR

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This circuit eliminates the risk to switch off the TV receiver in the event of a flash affecting the tube.

On starting up, the horizontal and vertical scanning functions come into operation at $V_{CC} = 6$ V. The power supply then comes into operation progressively.

On shutting down, the three functions are interrupted simultaneously after the first line fly-back.

ELECTRICAL OPERATING CHARACTERISTICS - $T_{amb} = 25°C$ - $V_{CC} = 12$ V (unless otherwise noted) - Pulse duration at 50 % of the ampl.

Characteristic	Symbol	Min	Typ	Max	Unit
Supply current (pin 8; frame, line and SMPS output without load)	I_{CC}	–	50	80	mA
Synch. separator (pins 26-27)					
Positive video input AC coupled (output impedance of signal source $< 200\ \Omega$)	–	0.2	1.8	3	Vpp
Negative clamping current (during synch. pulse).	$-I_{27}$	- 25	- 40	- 55	µA
Clamping current	I_{27}	3	6	9	µA
Pin for slicing level $0.2\ V < V_{27pp} < 2\ V$. (50 % of sync. amplitude)					
Positive current	$-I_{26}$	0	- 750	- 1000	µA
Negative current	I_{26}	17	25	36	µA
Pulse for keyed AGC (pin 20)					
Positive (function: without video signal: low level, with video signal: key pulses)					
Output current	I_{20}	–	–	5	mA
Output saturation voltage ($I_{20} = 5$ mA)	V_{20}	–	0.25	0.4	V
Pulse width (synchro pulse is always inside the key pulse)	t_k	6.5	8	8.5	µs
VCO (pins 17-18 and 19)					
Frequency control range after line divider (ceramic resonator : 503 kHz)	–	15.30 to 16.10	–	–	kHz
Phase comparator $\varphi 1$ (pin 22)					
Output current low loop gain high loop gain	– –	± 0.35 ± 1	± 0.50 ± 1.5	± 0.65 ± 2	mA mA
Window pulse width	–	7	10	13	µs
VCR switching (pin 23)					
Threshold voltage VCR operating	–	1.7	2.2	2.7	V
Input current ($V_{23} = 0$. $V_{CC} = 12$ V)	I_{23}	- 0.030	- 0.25	- 1	mA
Video identification (pin 24)					
Output saturation voltage (without video signal , $I_{24} = 3$ mA)	V_{24}	–	0.2	0.6	V
Output voltage (with 60 Hz video signal, $I_{24} = 2.5$ mA)	–	5	6.5	7.5	V
Output voltage (with 50 Hz video signal , $I_{24} = 10\ \mu A$)	–	11.0	11.5	–	V
Video identification (pin 25)					
Output current (charging the capacitor)	I_{25}	0.5	0.75	1	mA
Identification time (charging the capacitor)	t_{25}	1.3	1.7	2.2	µs
Threshold (voltage changing from lower to higher value)	V_{25}	4	4.5	5	V
Hysteresis	L_{HYS}	150	240	400	mV
H-ramp generator (pin 13)					
Charge current	I_{ch13}	185	200	215	µA
Base voltage of saw-tooth	V_{I13}	–	–	0.5	V
Discharge current	I_{dis13}	3.5	7.0	–	mA
Super sandcastle (pin 11)					
Output voltages					
Burst key pulse level ($I_{11} = -5$ mA)	V_{B11}	9	–	–	V
Line blanking pulse level ($I_{11} = -5$ mA)	V_{L11}	4	4.5	5	V
Frame blanking pulse level (and frame out of function)-($I_{11} = -5$ mA)	V_{BT11}	2	2.5	3	V

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

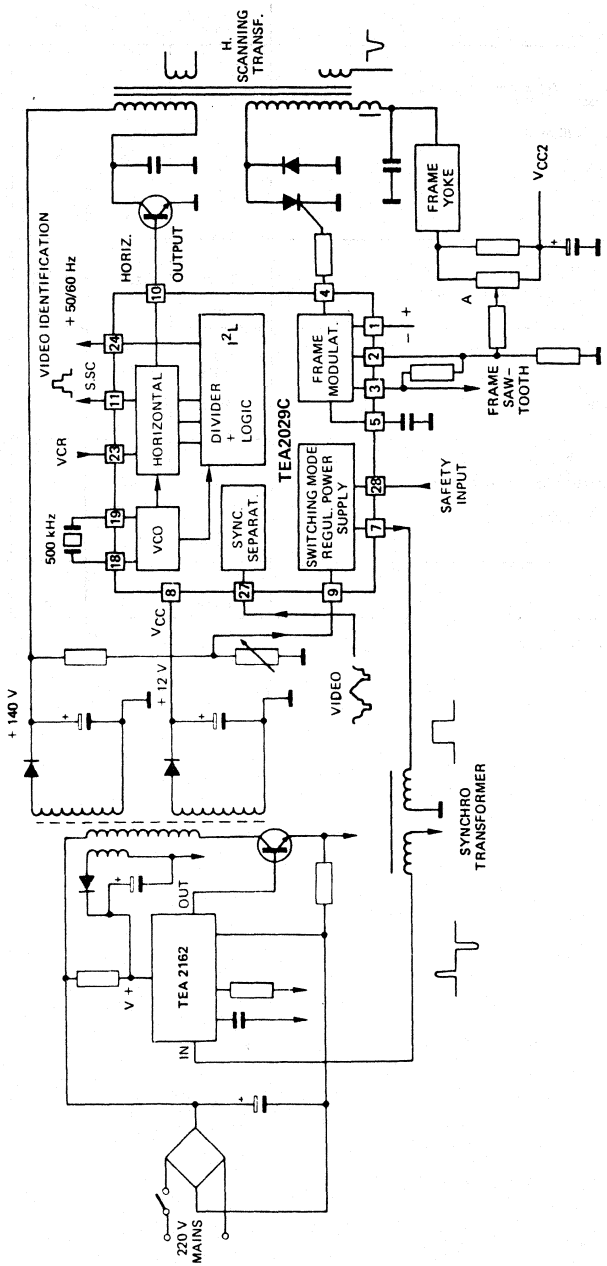
Characteristic	Symbol	Min	Typ	Max	Unit
Super sandcastle (continued)					
Delay between middle of synch. pulse (pin 27) and leading edge of burst key pulse	T_{B11}	2.3	–	3.0	µs
Duration of burst key pulse	–	3.7	4	5	µs
Delay between SSC cutting level at pin 12 and line blanding pulse	T_{O11}	–	–	0.35	µs
Frame blanking time (start with reset of frame divider)	–	21	–	24	Line
Negative line fly back input (pin 12)					
Threshold for SMPS safety	–	1.1	–	–	V
Threshold for blanking	V_{bl12}	11	11.5	12	V
Threshold for PLL2	$V_{\varphi 12}$	- 1	–	–	V
Input current $11\ V < V_{12}$	I_{12}	–	–	- 200	µA
Input current $1.3\ V < V_{12} < 11\ V$	I_{12}	- 3	–	+ 3	µA
Input current $0\ V < V_{12} < 1.3\ V$	I_{12}	0	–	- 80	µA
Input current $-1\ V < V_{12} < 0\ V$	I_{12}	0	- 1	- 2	mA
Line blanking trigger	–	–	–	80	µA
Phase comparator $\varphi 2$ (pin 16)					
Charging current	I_{16}	0.4	0.6	0.8	mA
Delay between the edges of $\varphi 1$ and $\varphi 2$ ($f_{VCO} = 500$ kHz)	–	1.5	2	2.8	µs
Line output (open collector) - (pin 10)					
Output voltage ($I_{10\ max} = 20$ mA)	–	–	1	1.5	V
Output pulse duration (when fly-back pulse is with in time T_{10}) ($f_{VCO} = 500$ kHz)	T_{10}	24	26	30	µs
$\varphi 2$ phase range	Δt	15	16	19	µs
Frame logic					
Free running period (with mute signal)	–	–	315	–	Line
Search window	–	247	–	361	Line
50 Hz window	–	309	–	315	Line
60 Hz window	–	247	–	276	Line
VCR mode window	–	247	–	361	Line
Frame saw-tooth generator (pins 3-5)					
Saw-tooth amplitude	–	2	3	4	Vpp
Internal current generator (60 Hz on)	$I_5(60)$	12	14	16	µA
Discharging time (with $C = 0.47\ \mu F$, $\Delta V < 4\ V$)	–	50	–	70	µs
Starting level ($0 < I_s < 10$ mA)	V_s	1	1.26	1.4	V
Saw-tooth amplitude ($I_s = 10$ mA)	–	2	3	4	Vpp
Frame feedback inputs (Pins 1-2)					
Positive and negative input current ($V_1 - V_2 > 25$ mV for frame blanking safety)	$I_{1,2}$	–	–	10	µA
Frame output (Pin 4)					
Output voltage ($0\ V < \lvert I_4 \rvert < 80$ mA)	–	10	–	–	
T_{ON} max ($f_{VCO} = 500$ kHz)	–	36	40	41	
Output phase range	–	0	–	t_{ON} max	

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

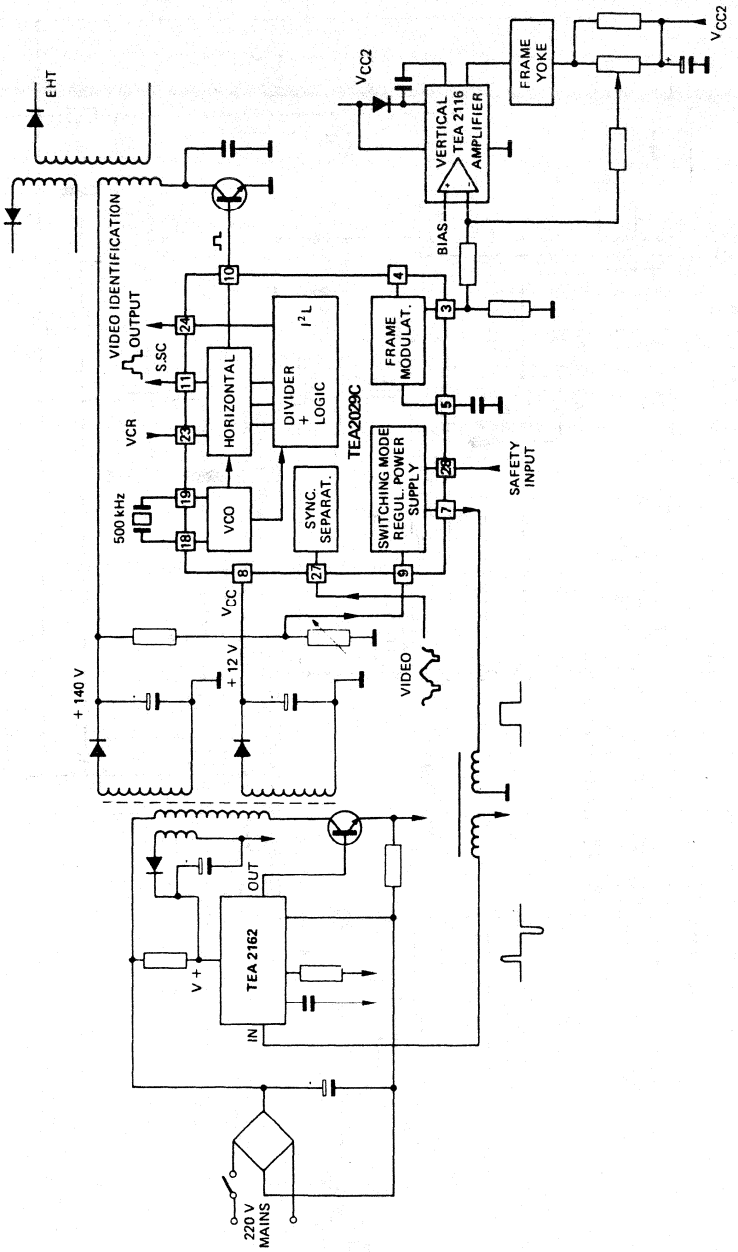
Characteristic	Symbol	Min	Typ	Max	Unit
SMPS control input (pin 9)					
Input current ($V_9 = V_{ref\ 14}$)	I_9	–	–	2	μA
SMPS output (pin 7)					
No relation between end of SMPS pulse (pin 7) and leading edge of line fly back (pin 12)					
Output voltage ($0 < I_7 < 20$ mA)	V_7	10	–	–	V
$t_{ON\ max}$ ($f_{VCO} = 500$ kHz)	T_7	30	32	34	μs
Nominal time ($V_9 = V_{ref\ 14}$)	–	26	–	31	μs
Output phase range	–	0	–	$t_{ON\ max}$	–
Safety input (pin 28)					
Threshold voltage ($V_{28} = V_{ref14}$)	V_{28}	1.15	1.26	1.37	V
Input current (if $V_{28} > V_{ref\ 14}$ then SMPS, line and frame are switched off during the next line retrace)	–	–	–	3	μA
Switch-on, switch-off processing (pin 15)					
Charging current ($t_c = 4$ μs, T = 64μs)	I_{ch15}	70	–	130	μA
Ratio charging/discharging	$\frac{I_{ch15}}{I_{dis15}}$	0.8	1	1.2	–
Starting supply voltage (pin 8)					
SMPS*, frame and line starting (pins 7, 10 and 4)	V_{CC}	5.25	–	6.5	V
SMPS stopping during line retrace	V_{CC}	5.25	–	6.5	V
Frame and line stopping	V_{CC}	5.25	–	6.5	V
Current reference (pin 14)					
Voltage reference	V_{ref14}	1.2	1.26	1.35	V

* Progressive starting by decreasing V_{15}

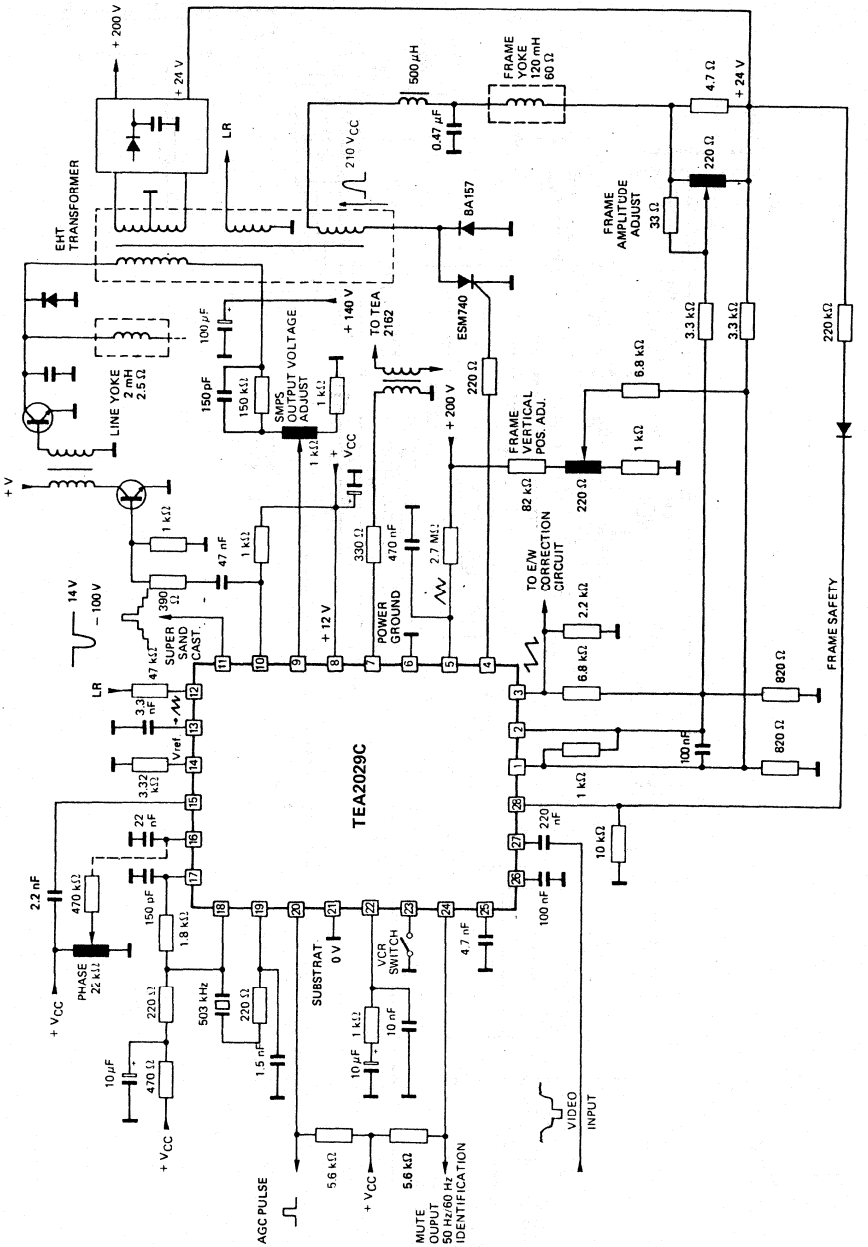
APPLICATION WITH THYRISTOR FOR FRAME POWER
AND TEA2162 FOR SECONDARY SMPS REGULATION



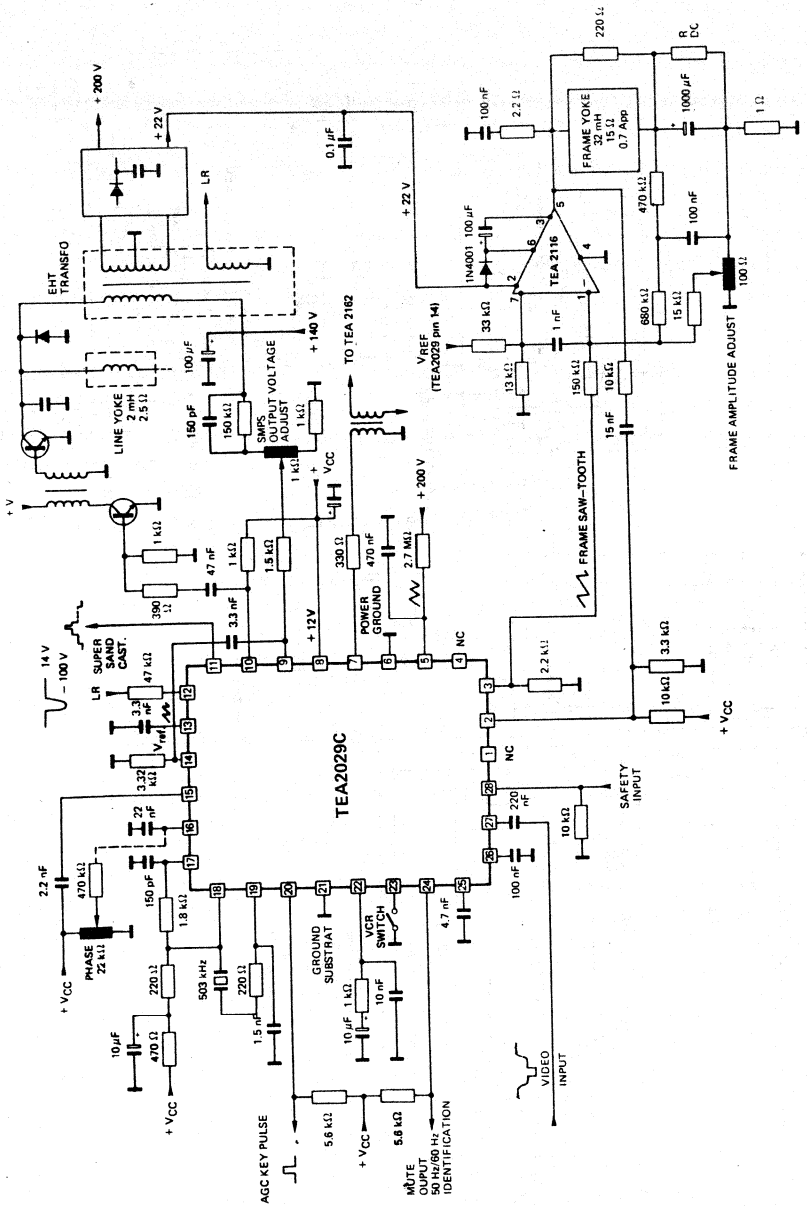
APPLICATION WITH TEA2116 FOR B CLASS FRAME POWER AND TEA2162 FOR SECONDARY SMPS REGULATION



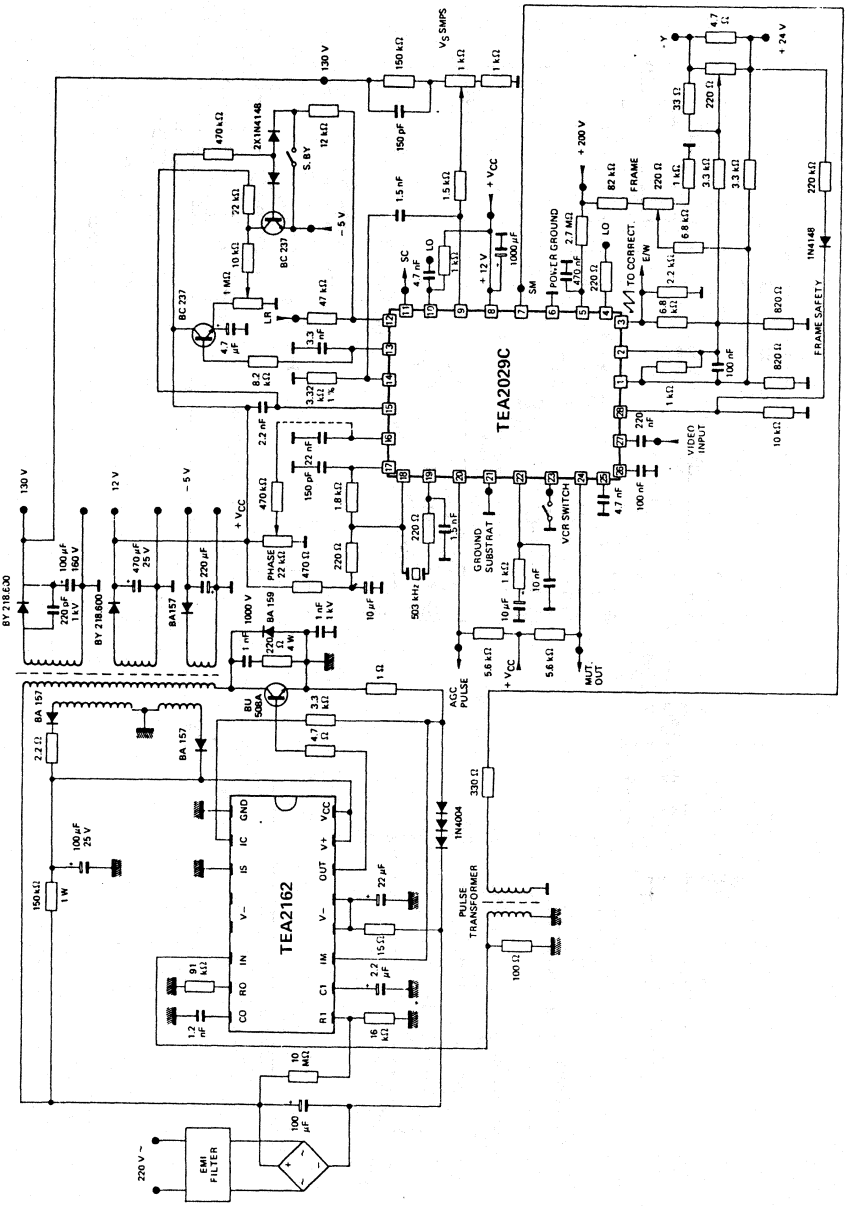
APPLICATION CIRCUIT
(WITH THYRISTOR FRAME POWER)



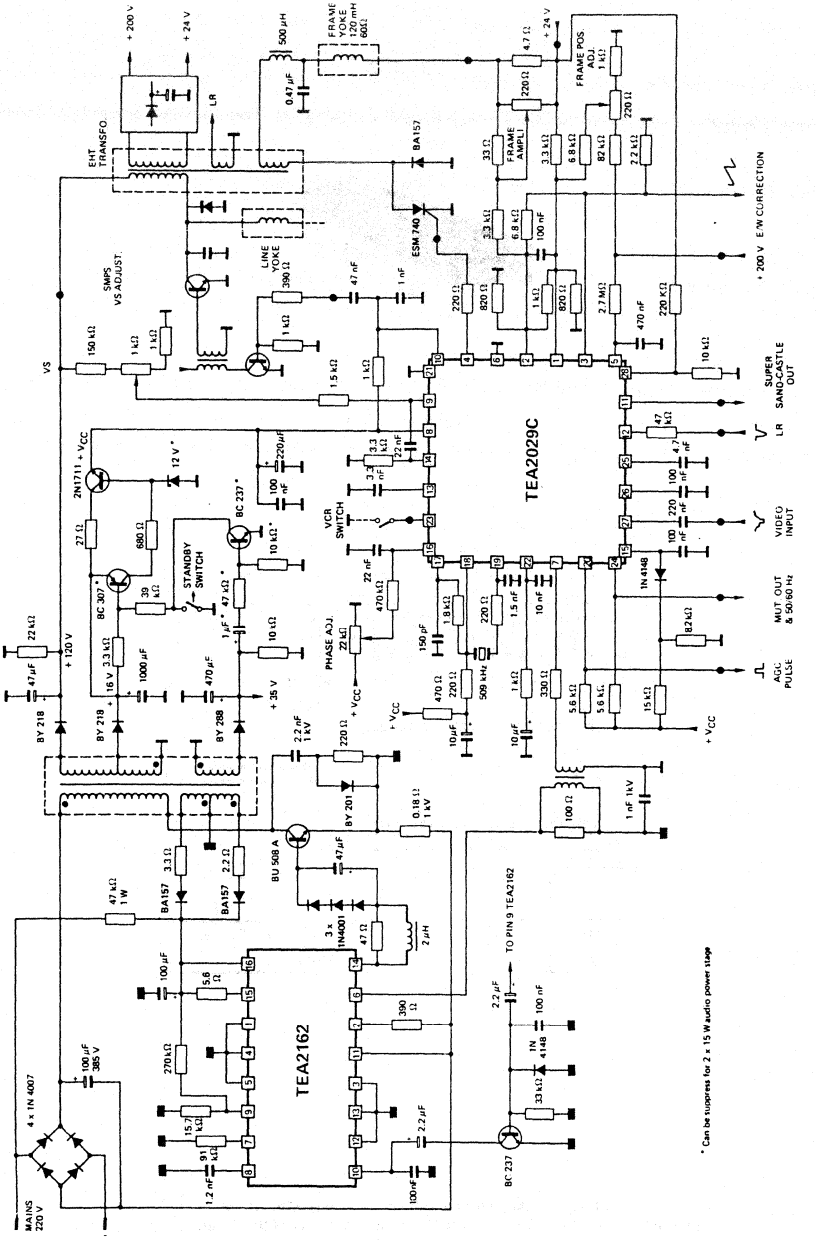
APPLICATION CIRCUIT
(WITH B CLASS FRAME POWER)



APPLICATION CIRCUIT
(WITH TEA2162 SMPS IC)

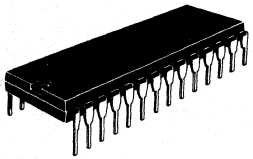


APPLICATION WITH LOW POWER STANDBY
3 W ON THE MAINS AND AUDIO POWER 2 x 30 W

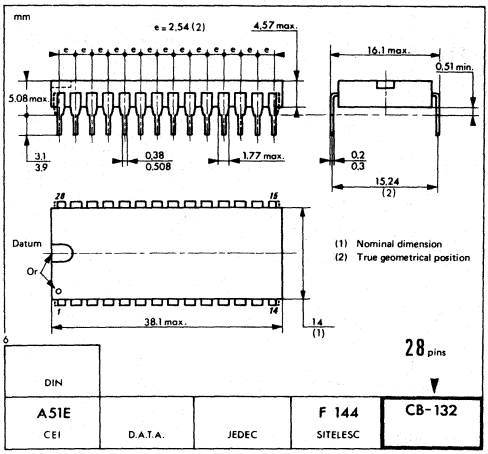


PHYSICAL DIMENSIONS

CB - 132



PLASTIC PACKAGE



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THOMSON COMPONENTS SEMICONDUCTEURS

TEA2037A

HORIZONTAL AND VERTICAL DEFLECTION MONITOR

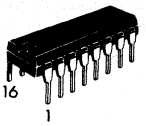
The TEA2037A is an horizontal and vertical deflection circuit. It uses the same concept as TEA2017 but optimised for small screens, for a very low cost solution.

Mains features

- Direct line darlington drive
- Direct frame-yoke drive (± 1 A)
- Composite video signal input capability
- Frame output protection against short circuits
- PLL
- Very few external component
- Very low cost power package

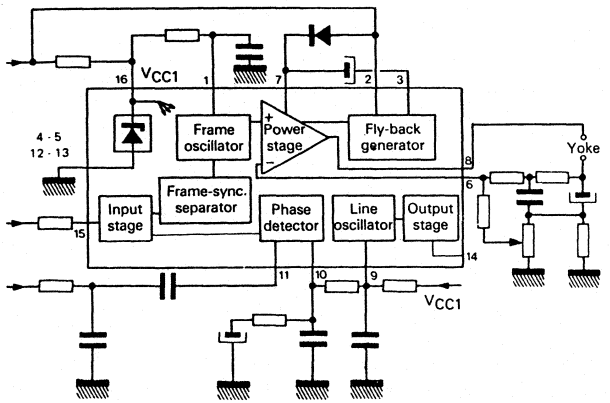
HORIZONTAL AND VERTICAL DEFLECTION MONITOR

CASE CB-79

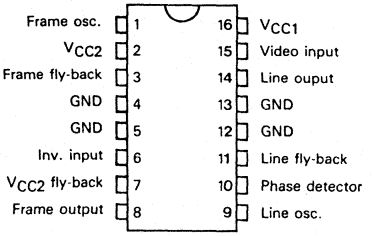


PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Direct frame supply voltage	V_{CC2}	30	V
Flyback peak voltage	V_{FB}	60	V
Supply voltage	V_{CC1}	30	V
Storage and junction temperature		− 40 + 150	°C
Frame output current (non repetitive)	I8	± 1,5	A
Line output voltage (external)	V_{14}	60	V
Line output peak current	I_p 14	0.8	A
Line output continuons current	I_p14	0.4	A

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Max junction-case thermal resistance	$R_{th\ (j\text{-}c)}$	15	°C/W
Typical junction ambient thermal resistance	$R_{th\ (j\text{-}a)}$	60	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$

Characteristic	Symbol	Min	Typ	Max	Unit
FRAME OSCILLATOR					
Low threshold voltage	$V_1 L$	1.8	2	2.2	V
High threshold voltage	$V_1 H$	2.6	3.1	3.6	V
Discharge impedance		300	500	700	Ω
Leakage current		–	40	–	nA
Free running period (R=845 kΩ, C = 180 nF)		20.5	–	25	ms
Frame supply voltage	V_{CC2}	10	–	30	V
Frame supply current (V_{CC2} = 30 V unloaded)	I_{CC2}	8	25	50	mA
FRAME FLYBACK GENERATOR					
High level during the flyback (V_{CC2} = 30 V)	V_3	–	29●	–	V
FRAME OUTPUT					
Saturation voltage to ground (V_{CC2} = 25 V, I8 = 1 A)	I8	–	–	1	V
Saturation voltage to V_{CC2} (V_{CC2} = 25 V, I8 = 1 A)	I8	–	–	2.4	V
Saturation resistor to ground		–	–	1	Ω
Saturation resistor to V_{CC2}		–	–	1.2	Ω
LINE OSCILLATOR					
Leakage current		–	100	–	nA
Low threshold voltage	VgL	2.8	3.2	3.6	V
High threshold voltage	VgH	5.4	6.6	7.8	V
Discharge impedance		1	1.4	1.8	kΩ
PHASE DETECTOR					
Output current during sync-pulse	I_{10}	–	±0.5	–	mA
Pull-in range (With application fig. 8)		±600	–	–	Hz
LINE FLYBACK INPUT					
Input impedance		4.5	5.6	7	KΩ
LINE OUTPUT					
Saturation voltage (I_{14} = 200 mA)		–	–	2	V
Pulse width		20	–	24	µs
VIDEO INPUT					
Threshold voltage		1.4	1.6	2	V
SHUNT REGULATOR					
Typical voltage (I_{16} = 15 mA)		9	–	10.5	V
Supply current		10	–	20	mA

GENERAL DESCRIPTION

The TEA2037A performs all the video and power functions required to provide signals for the direct drive of the line darlington and frame yoke.

It contains :

- A shunt regulator
- A synchronization separator
- An integrated frame separator without external components.
- A saw-tooth generator for the frame.
- A power amplifier for direct drive of frame yoke (short circuit protected).
- An open collector output for the line darlington drive.
- A line phase detector and a voltage control oscillator.

SYNCHRONIZATION SEPARATOR CIRCUIT

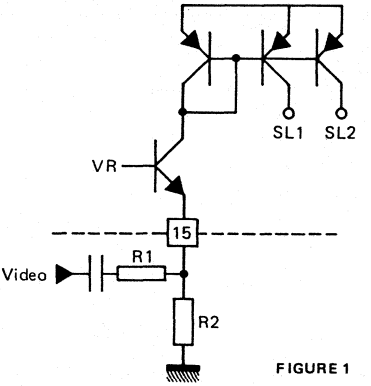


FIGURE 1

The slice level of sync-separation is fixed by value of the external resistors R_1 and R_2. V_R is an internally fixed voltage.

FRAME SEPARATOR

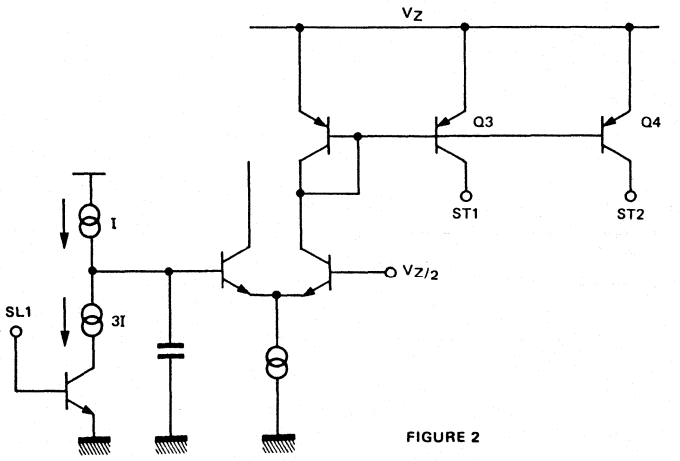


FIGURE 2

The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync pulse permits the complete discharging of the capacitor, so during the frame sync-pulse Q3 and Q4 provide current for the other parts of the circuit.

LINE OSCILLATOR

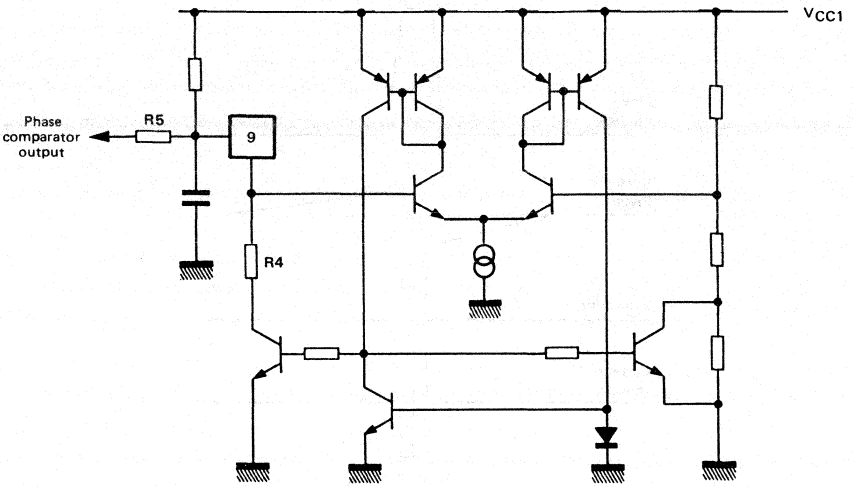


FIGURE 3

The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

PHASE COMPARATOR

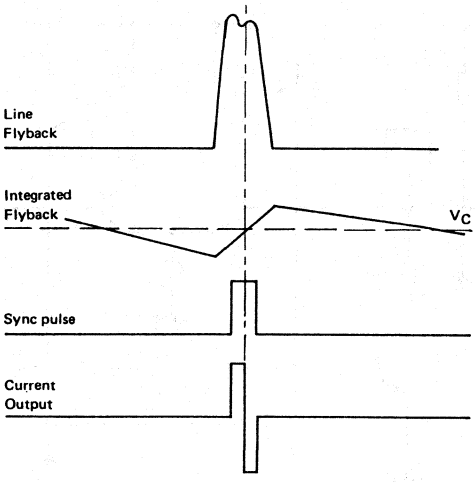


FIGURE 4

The sync-pulse drives the current in the comparator. The line flyback integrated by the external network gives on pin 11 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 11 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

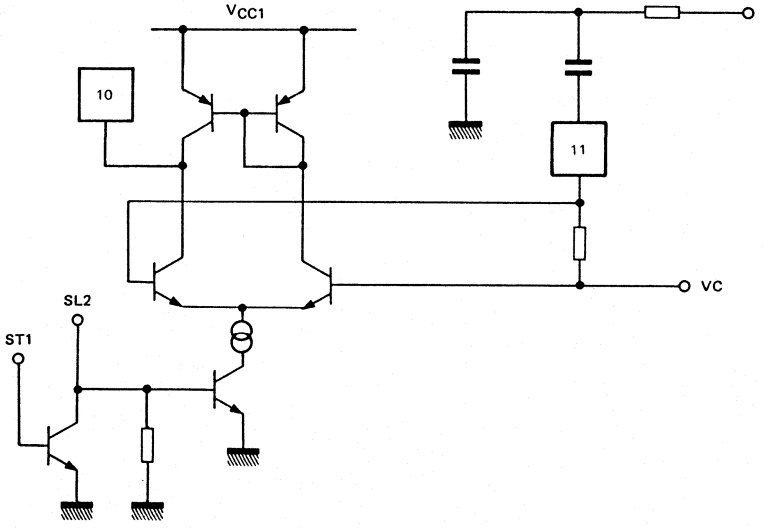


FIGURE 5

LINE OUTPUT (PIN 14)

It is an open collector output which is able to drive pulse current of 800 mA for a rapid discharging of the darlington base. The output pulse time is 22 μs for a 64 μs period.

FRAME OSCILLATOR

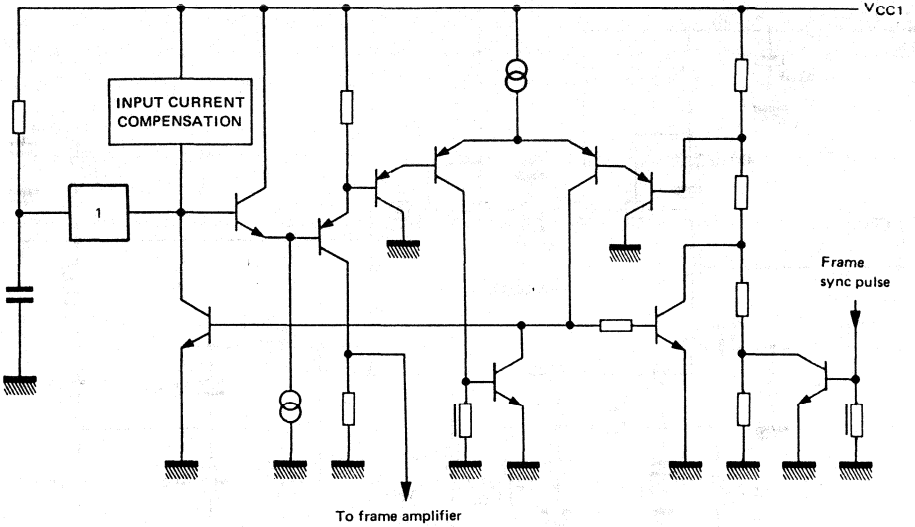


FIGURE 6

The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100 nA.

FRAME OUTPUT AMPLIFIER

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected ; it contains also a thermal protection.

TYPICAL APPLICATION FOR DISPLAY UNITS
(without flyback generator and with sync-pulse drive-yoke : 72 mH, 40 Ω)

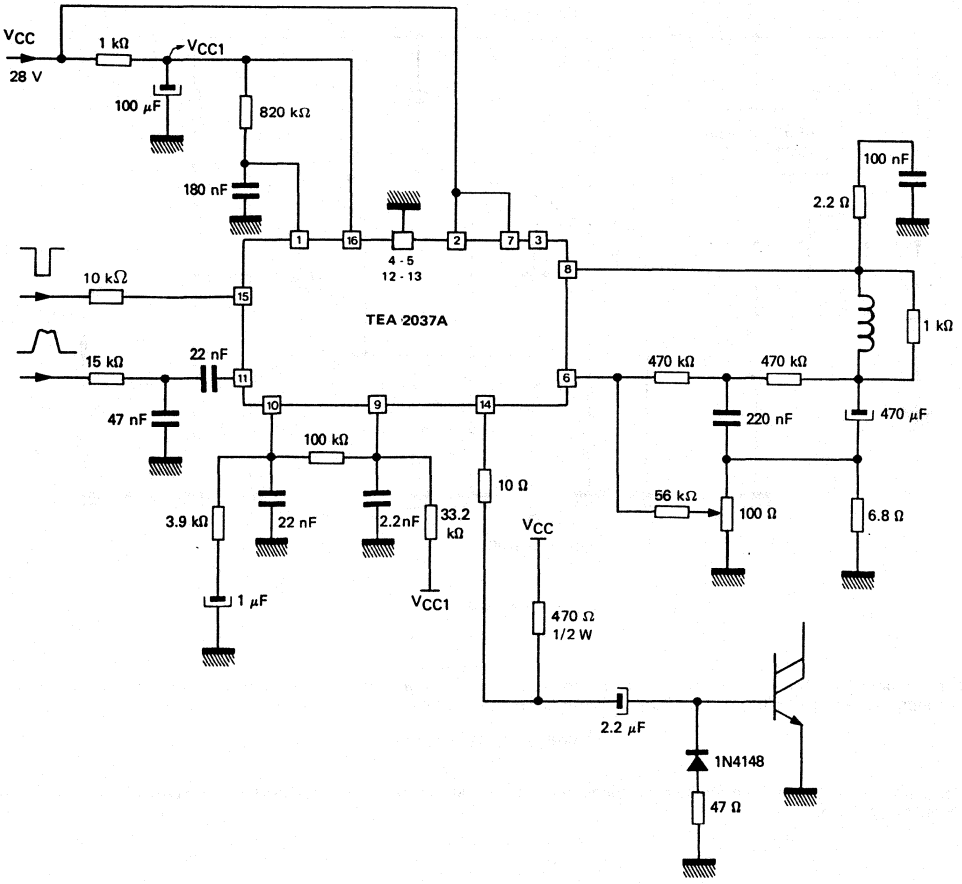


FIGURE 7

TYPICAL APPLICATION FOR DISPLAY UNITS
(with flyback generator and video drive-yoke : 72 mH, 40 Ω)

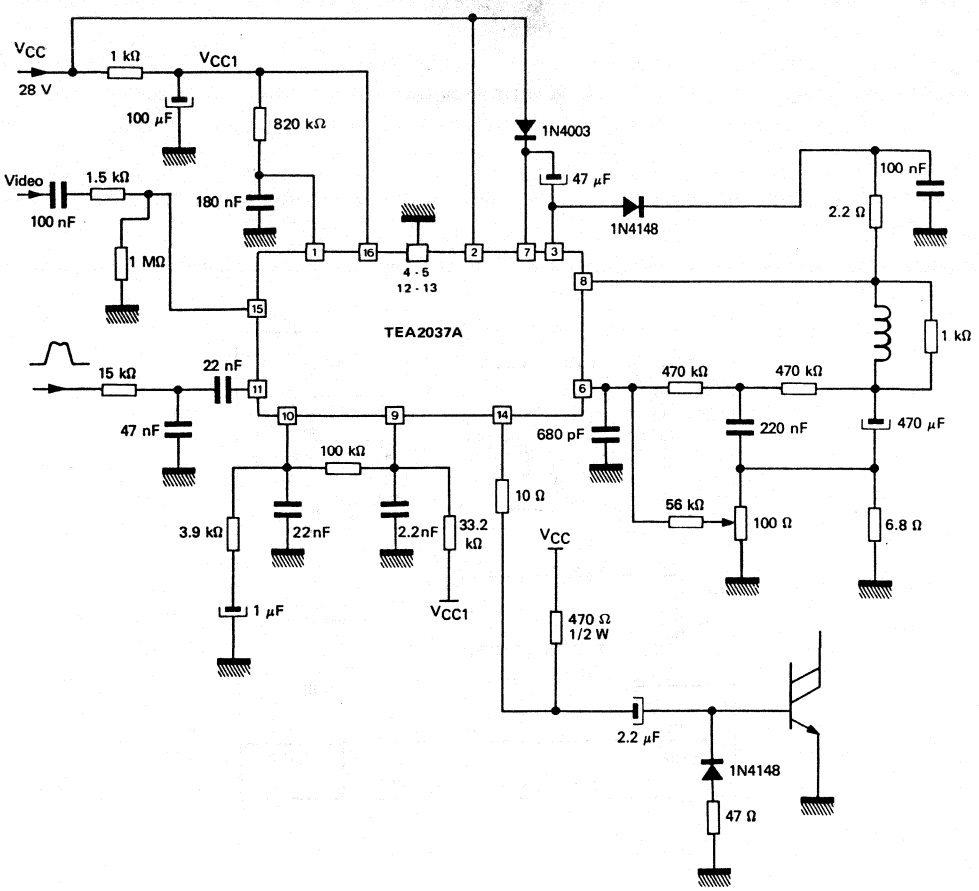
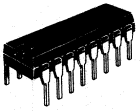


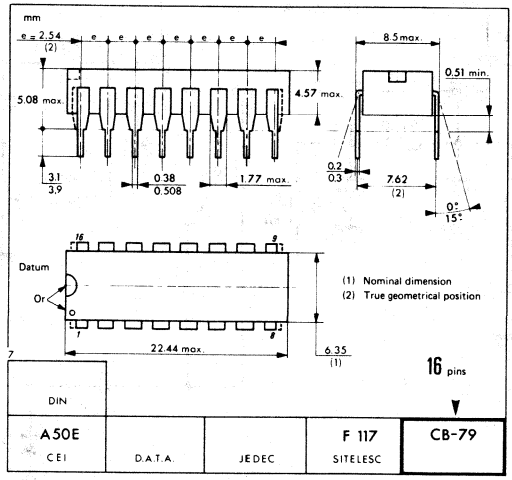
FIGURE 8

PHYSICAL DIMENSIONS

CB-79



PLASTIC PACKAGE



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HOMSON
COMPONENTS
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TEA2115

TV VERTICAL DEFLECTION AMPLIFIER

ADVANCE INFORMATION

The TEA2115 is a power amplifier for frame TV yoke direct drive.
It is intented for color or black and white TV sets, monitors, and displays.

MAIN FEATURES

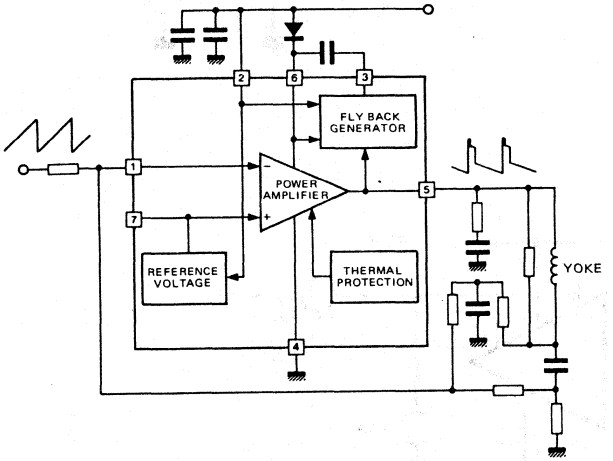
- Fly-back generator
- Voltage reference
- Thermal protection
- Protection against electrostatic discharges

TV VERTICAL DEFLECTION AMPLIFIER

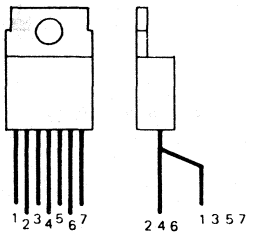
CASE
CB-512

PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



1 : Inverting input
2 : V_{CC} output stage
3 : Flyback generator
4 : Ground
5 : Output
6 : V_{CC}
7 : Non inverting input and reference voltage.

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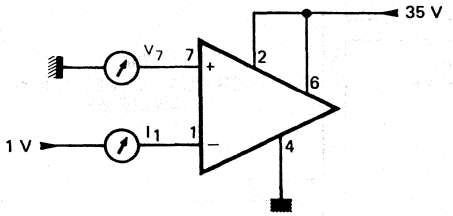
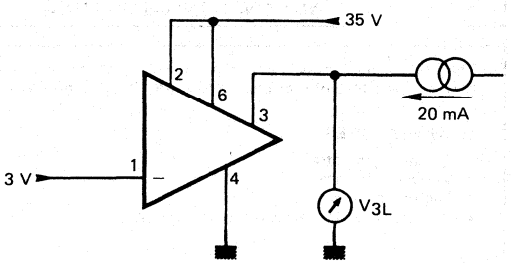
DC TEST CIRCUITS

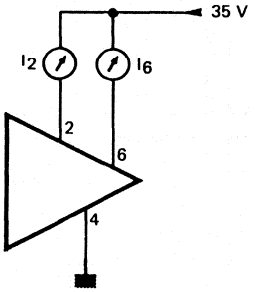
– Measurement of I_1, V_7 and / V_7 /ΔV_{CC}.



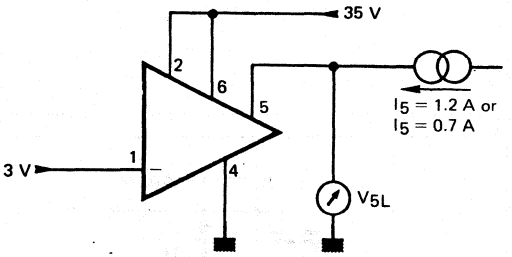
– Measurement of V_{3L}



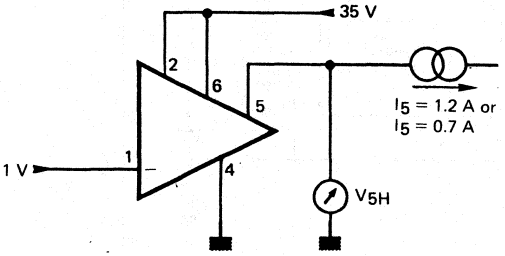
– Measurement of I_2 and I_6



– Measurement of V_{5L}



– Measurement of V_{5H}



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	35	V
Fly back peak voltage	V5, V6	60	V
Amplifier input voltage	V_1, V_7	V_{CC}	
Pin 3 voltage	V_3	V_{CC}	
Output peak current ($t < 10\mu s$)	I_5	± 2	A
Output peak current ($t > 10\mu s$)	I_5	1.5	A
Pin 3 DC current (during frame) ($V_5 < V_2$)	I_3	150	mA
Pin 3 fly back peak-to-peak current	I_3	2	A
Power dissipation (T case = 70°C)	P	20	W
Storage and junction temperature	T_{stg}, T_j	- 40 to 150	°C

THERMAL CHARACTERISTICS

	R_M (j.c)	Unit
Max thermal resistance (junction case)	4	°C/W

ELECTRICAL OPERATING CHARACTERISTICS - T_{amb} = 25° ; V_2 = 35 V (unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Amplifier input bias current (V_1 = 1 V)	I_1	–	- 0.2	- 1.0	μA
Pin 2 quiescent current ($I_3 = 0$, $I_5 = 0$)	I_2	–	2	–	mA
Reference voltage	V_7	–	2.2	–	V
Reference voltage drift VS. Supply voltage	$\frac{\Delta V_7}{\Delta V_{CC}}$	–	1	–	mV/V
Fly back saturation voltage to GND (I_3 = 20 mA)	V_{3L}	–	1.5	–	V
Output saturation voltage to ground (I_5 = 1.2 A)	V_{5L}	–	1	–	V
(I_5 = 0.7 A)	V_{5L}	–	0.8	–	V
Output saturation voltage to supply (I_5 = 1.2 A)	V_{5H}	–	1.5	–	V
(I_5 = 0.7A)	V_{5H}	–	1.4	–	V
Pin 6 quiescent current ($I_3 = 0$, $I_5 = 0$)	I_6	–	15	–	mA
Drift versus supply ($V_2 = V_6$ = 15 to 30 V)	ΔV_5	–	1	–	mV
Junction temperature for thermal shut down	T_j	–	140°		°C

GENERAL DESCRIPTION

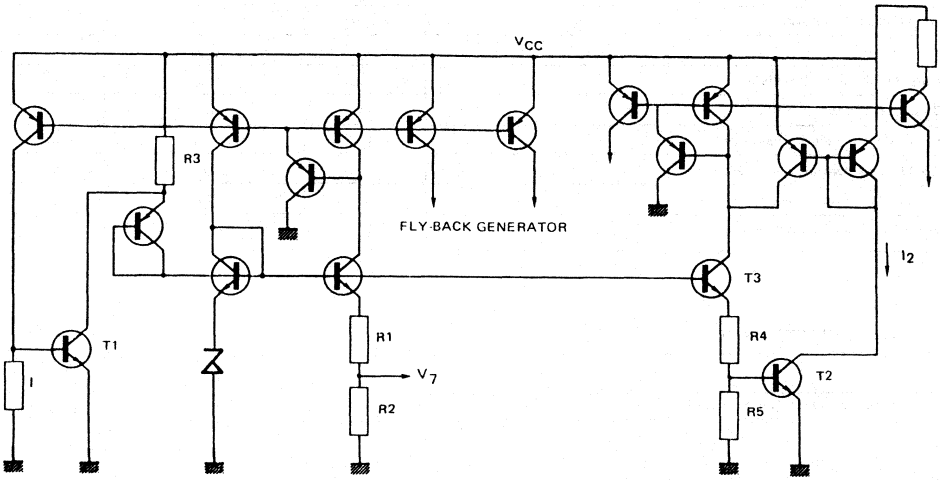
The TEA2115 permits direct frame yoke driving for a TV set working in B class with a peak current of ± 2A.

INTERNAL SUPPLY

The supply stage is intented to provide current and a voltage reference independants on main supply voltage. It uses a Zener diode.

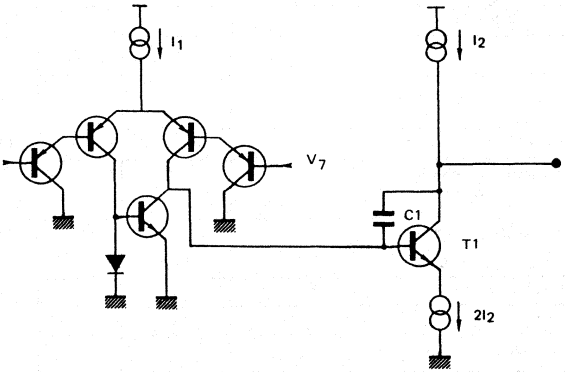
The two resistors R1 and R2 determine a 370 μA current (I_1) for fly back generator, the input stage and the supply starting system.

R4 and R5 fixe the current value of the power stage at 1 mA (I_2) with transistor T2, R4 and R5 ensure a thermal protection at 140°C.



INPUT STAGE AND OFFSET

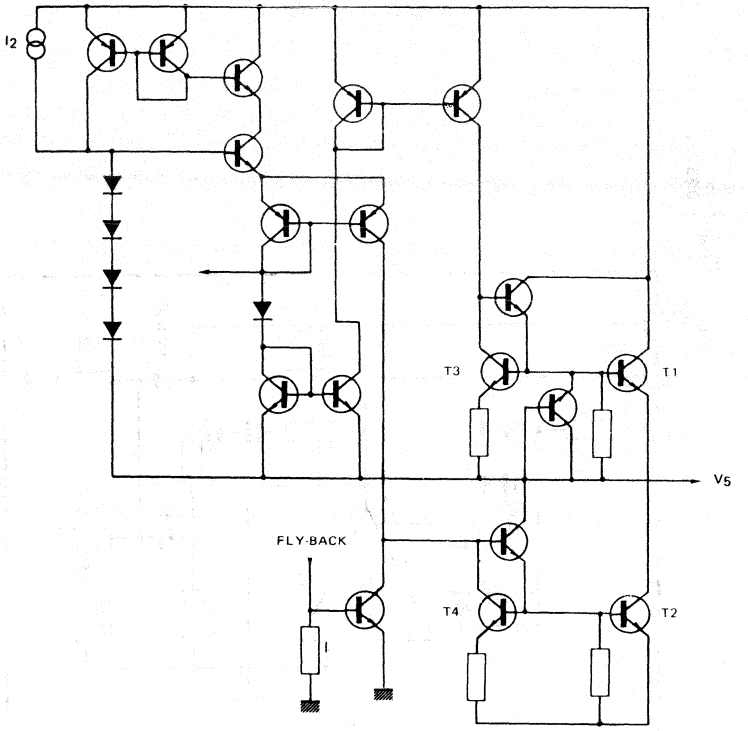
The two current sources directly come from the power supply. The current source $2I_2$ is dedicated to limit the driving current at ± 1 mA.



POWER STAGE

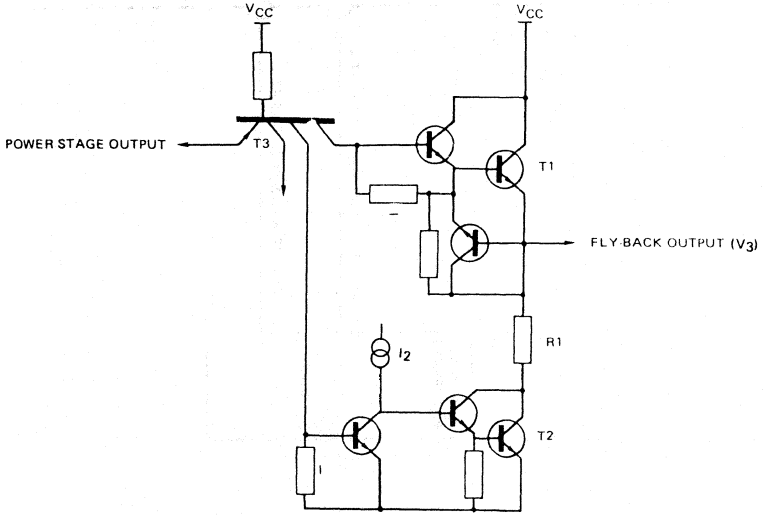
The current amplification of this stage is egal to 2040.

So for an input current of ± 1 mA, the output current is ± 2A.

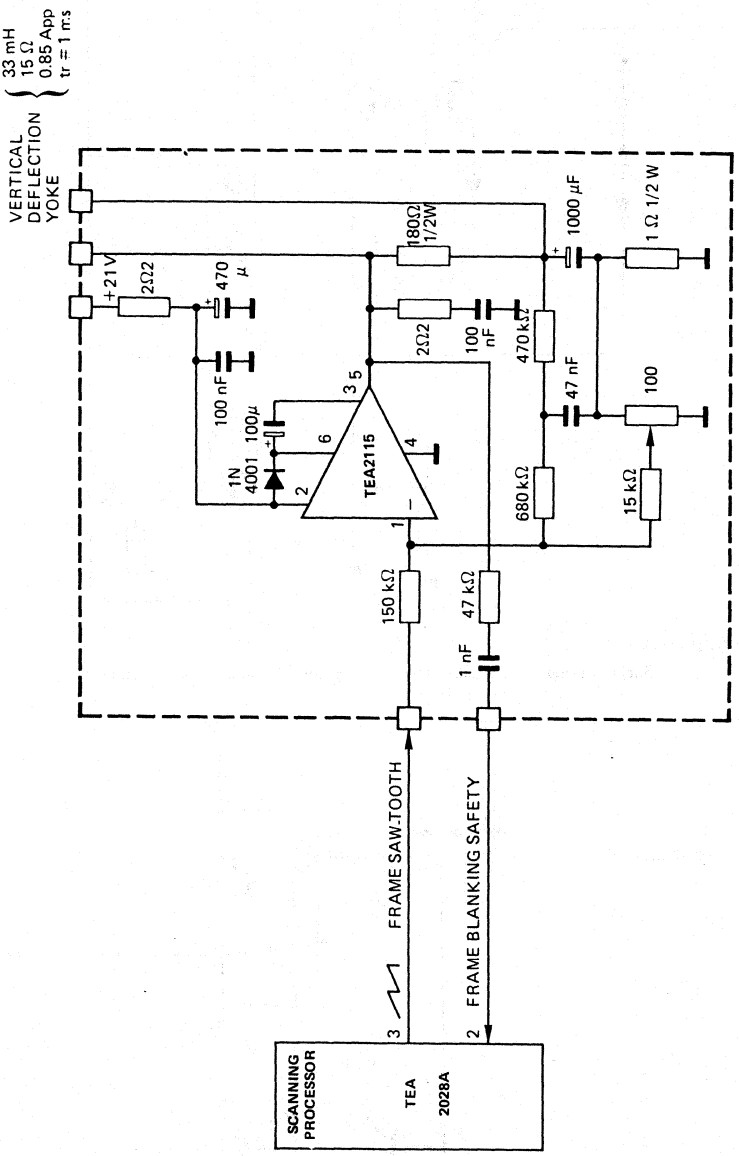


FLY BACK GENERATOR

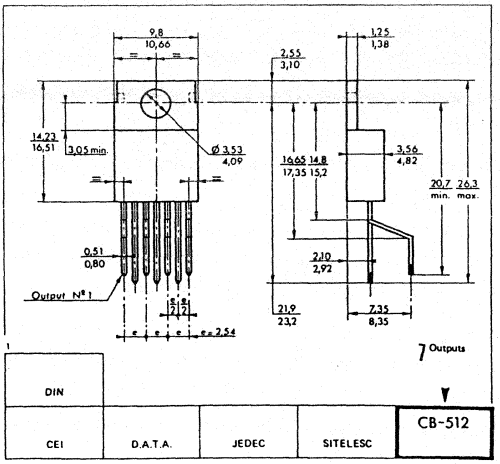
The transistor T3 is conductor during the fly-back. The resistor R1 limits the output current.



APPLICATION CIRCUIT



PHYSICAL DIMENSIONS



CB-512

PLASTIC PACKAGE

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NOTES

Printed in France

THOMSON
COMPONENTS
SEMICONDUCTEURS

TBA920—TBA920S

LINE OSCILLATOR COMBINATION FOR TV SET

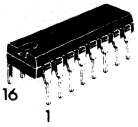
The line oscillator combination TBA920 is a monolithic integrated circuit intended for the horizontal deflection of the black and white and colour TV sets picture tube.

This circuit is able to perform the following functions (see block diagram, page 2) :

- Sync-pulse separation
- Optional noise inversion
- Generation of a line frequency voltage by means of on oscillator
- Phase comparaison between sync-pulse and the oscillator waveform
- Phase comparaison between the oscillator waveform and the middle of the line fly-back pulse
- Automatic switching of the variable transconductance and the variable time constant to achieve noise suppression and, by switching off, possibility of tape-video-registered reproduction
- Shaping and amplification of the oscillator waveform to obtain pulses for the control of driving stages in horizontal, deflection circuits using either transistors or thyristors.

LINE OSCILLATOR COMBINATION FOR TV SET

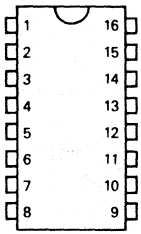
CASE CB-79



PLASTIC PACKAGE

PIN ASSIGNMENT

1 - Positive supply
2 - Driver line stage pulse, driving and output stage
3 - Input control voltage for pulse width
4 - Phase discriminator output between fly-back pulse and oscillator
5 - Fly-back pulse input
6 - Synchro pulse input
7 - Synchro pulse output
8 - Video signal input
9 - Noise gate input
10 - Switch emission-magnetoscope
11 - Time constant switch
12 - Oscillator control voltage loop
13 - Oscillator decoupling
14 - Tuning oscillator capacitor
15 - Oscillator control voltage
16 - Ground



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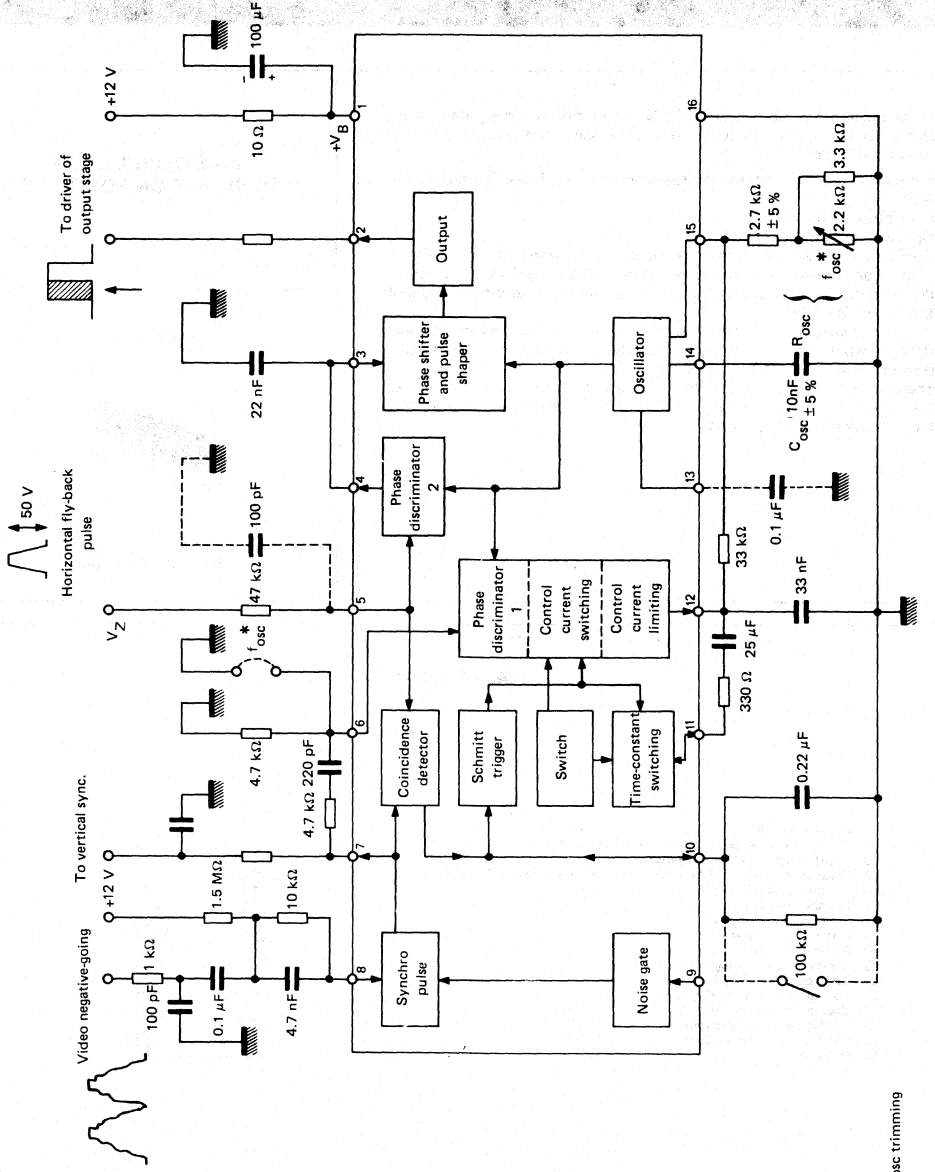
BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage V_{1-16}	V_{CC}	4 to 14	V
Total power dissipation	P_{tot}	600	mW
Ambiant temperature	T_{amb}	− 20 to + 60	°C
Storage temperature	T_{stg}	− 55 to + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C V_{CC} = 12 V (Unless otherwise specified)

Characteristic	Symbol	Min.	Typ	Max	Unit
Video signal (pin 8)					
Input voltage (positive synchro-pulse)	V_I	1	3	7	V
Input current	I_I	–	–	0.2	mA
Fly-back pulse (pin 5)					
Input current	I_I	0.1	1	2	mA
Input voltage	V_I	–	±0.8	–	V
Input resistance	Z_I	–	0.4	–	kΩ
Noise gate (pin 9)					
Input current	I_I	–	20	–	μA
Input voltage	V_I	–	0.7	–	V
Synchro pulse (pin 7)					
Output voltage	V_O	9	10	–	V
Output impedance on rise time	Z_O	–	50	–	Ω
Output impedance on fall time	Z_O	–	2.2	–	kΩ
Line amplifier					
Output current (peak to peak)	I_O	–	25	200	mA
Output voltage	V_O	9	10	–	V
Output pulse duration (adjust by V_{3-16})	t_p	12	–	32	μs
Fly-back pulse phase control					
Delay accepted between output pulse and fly-back pulse		0	–	15	μs
Output current during fly-back pulse	I_O	–	±0.5	–	mA
Line oscillator (no synchronized) for 625 lines		–	15625 ±5 %	–	Hz
for 819 lines		–	20475 ±5 %	–	Hz
At supply cut-off, without synchronized					
for 625 lines		–	15625 ±10 %	–	Hz
for 819 lines		–	20475 ±10 %	–	Hz
Phase control between oscillator and synchro-pulse					
• With emission					
Pull in range		–	±1	–	kHz
Keep in range		–	±1	–	kHz
Sensibility	S	–	3	–	kHz/μs

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)
T_{amb} = 25°C V_{CC} = 12 V (unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
• With magnetoscope					
Keep in range		–	±350	–	Hz
Pull in range		–	±350	–	Hz
Sensibility	S	–	±1	–	kHz/µs
Oscillator (pin 14)					
Oscillator frequency spead R_{15-16} = 3.3 kΩ C_{14-16} = 10 nF	ΔF_O	–	⩽1.5	–	%
Oscillator frequency range (figure 1 and 2)	ΔF_O	–	±5	–	%
Phase position (pin 5-6)					
Phase spead between front end synch pulse and fly-back pulse center (figure 1)	Δt	–	⩽±0.4	–	µs

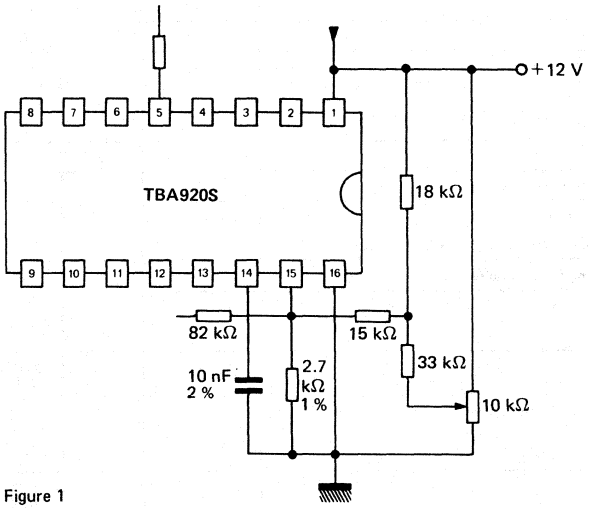
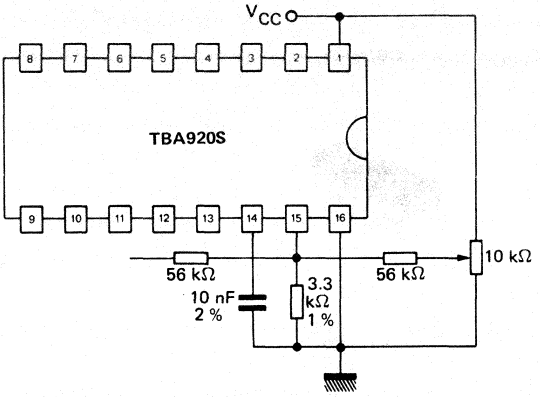


Figure 1

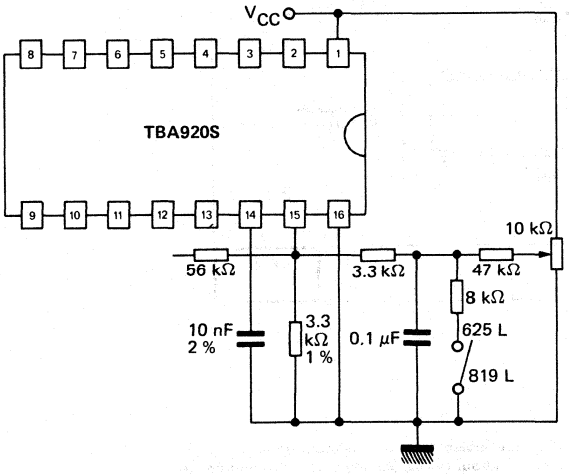
APPLICATION : EUROPEAN STANDARD 625 LINES



Control : $\Delta_f = \pm 5\ \%$

Figure 2

APPLICATION : FRENCH STANDARD 625 - 819 LINES
Progressive change 625 819 lignes



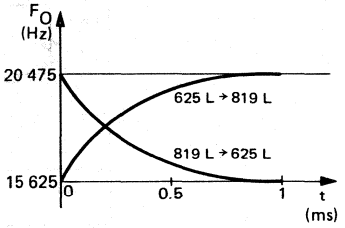
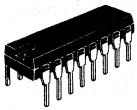


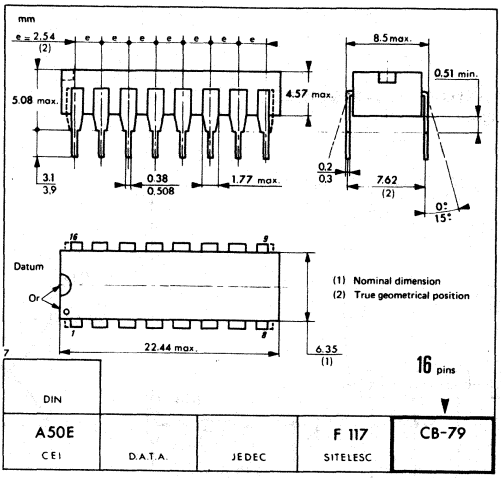
Figure 3

PHYSICAL DIMENSIONS

CB-79



PLASTIC PACKAGE



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HOMSON COMPONENTS
EMICONDUCTEURS

TDA2593

SYNCHRO AND HORIZONTAL DEFLECTION CONTROL FOR COLOR TV SET

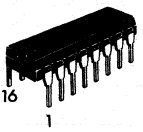
The TDA2593 is a circuit intended for the horizontal deflection of solid-state color TV sets, supplied with transistors or SCR'S.

It performs the following functions :

- Line oscillator (two levels switching)
- Phase comparison between synchro-pulse and oscillator voltage ϕ 1, enabled by an internal pulse, (better parasitic immunity)
- Phase comparison between the fly-back pulses and the oscillator voltage ϕ 2
- Coincidence detector providing a large hold-in-range
- Filter characteristics and gate switching for video recorder application
- Noise gated synchro separator
- Frame pulse separator
- Blanking and sand castle pulses generators compatibles with new decoder circuits
- Horizontal power stage phase lagging circuit
- Switching of control output pulse width
- Separated supply voltage output stage allowing direct drive of SCR'S circuit
- Security circuit makes the output pulse suppressed when poor supply voltage

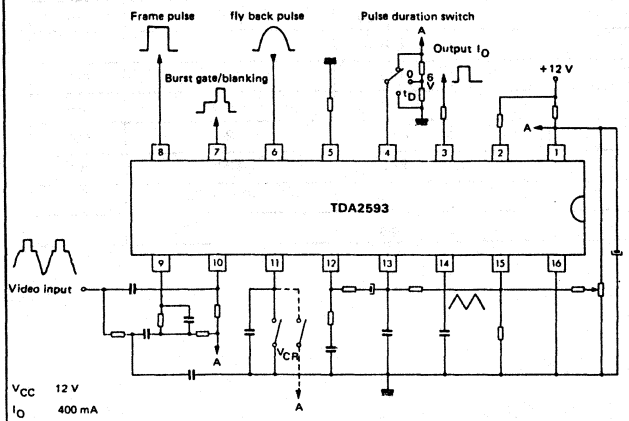
SYNCHRO AND HORIZONTAL DEFLECTION CONTROL FOR COLOR TV SET

CASE CB-79

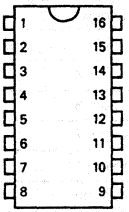


PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



1 - Supply voltage
2 - Output stage supply voltage
3 - Output pulse
4 - Selection of output pulse duration
5 - Decoupling
6 - Reference pulse (fly-back) for the 2nd phase comparator
7 - Sand castle pulse
8 - Vertical synchro output
9 - Synchro separator output
10 - Noise separator input
11 - V.C.R. switching
12 - Time constant switching (third phase comparator)
13 - First phase comparator output
14 - Ramp oscillator capacitance
15 - Adjustment of the charge current
16 - Ground

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MAIN CHARACTERISTICS

Characteristic	Symbol	Typ	Unit
Supply voltage	V(1–16)	12	V
Supply current	I(1)	30	mA
INPUT SIGNALS			
Synchro separator input voltage	V(9–16) (pp)	3 to 4	V
Noise separators input voltage	V(10–16((pp)	3 to 4	V
Control voltage of the output pulse switching circuit			
$t = 7\ \mu s$ (thyristor)	V(4–16)	9.4 to V(1–16)	V
$t = 14\ \mu s + t_d$ (transistor)	V(4–16)	0 to 3.5	V
$t = 0$(V3–16 = 0)	V(4–16)	5.4 to 6.6	V
OUTPUT SIGNALS			
Frame synchro pulse	V(8–16) (pp)	11	V
Sandcastle pulse	V(7–16) (pp)	11	V
Horizontale driver stage control pulse	V(3–16) (pp)	10.5	V

MAXIMUM RATINGS

Maximum ratings according to CEI 134 data sheet

Rating	Symbol	Value	Unit
Supply voltage to pin 1	V(1–16)	13.2	V
Supply voltage to pin 2	V(2–16)	18	V
Voltage to pin 4	V(4–16)	13.2	V
Voltage to pin 9	V(9–16)	±6	V
Voltage to pin 10	V(10–16)	±6	V
Voltage to pin 11	V(11–16)	13.2	V
Current at pins 2 and 3 (with thyristor)	$I_{2M} = -I_{3M}$	650	mA
Current at pins 2 and 3 (with transistor)	$I_{2M} = I_{3M}$	400	mA
Current to pin 4	I(4)	1	mA
Current to pin 6	I(6)	±10	mA
Current to pin 7	I(7)	−10	mA
Current to pin 11	I(11)	2	mA
Power dissipation	P_{tot}	800	mW
Operating ambient temperature	T_{amb}	−20 to +70	°C
Storage temperature	T_{stg}	−25 to +125	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V1–V16 = 12 V (Unless otherwise specified).

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT SIGNALS					
Synchro separator (pin 9)					
Input threshold voltage	V(9–16)	–	0.8	–	V
Input threshold current	I(9)	–	–	5	μA
On-state input current	I(9)	–	5 to 100	–	μA
Disconnect input current	I(9)	100	150	–	μA
Off-state input current (V9 – 16 = – 5 V)	I(9)	–	–	– 1	μA
Video input signal (positive synchro pulses) (note 1)	V(9)	–	3 to 4	–	Vpp
Noise separator (pin 10)					
Input threshold voltage	V(10–16)	–	1.4	–	V
Input threshold current	I(10)	100	150	–	μA
Input current	I(10)	–	5 to 100	–	μA
Off-state input current (V10 – 16 = – 5 V)	I(10)	–	–	– 1	μA
Video input signal (positive synchro pulses) (note 1)	V(10)	–	3 to 4	–	Vpp
Allowed superimposed parasitic signal	V(10)	–	–	7	V
Fly-back pulse (pin 6)					
Input threshold voltage	V(6–16)	–	1.4	–	V
Input limitation level	V(6)	–	–07 and + 1.4	–	V
Input current	I(6)	0.01	1	2	mA
Output pulse width control switch (pin 4)					
Input voltage t = 7 μs (thyristor)	V(4–16)	–	9.4 to V(1–16)	–	V
t = 14 μs + t_d (transistor)	V(4–16)		0 to 3.5	–	V
t = 0 (V3 – 16 = 0) (note 2)	V(4–16)	–	5.4 to 6.6	–	V
Input current t = 7μs (thyristor)	I(4)	200	–	–	μA
t = 14 μs + t_j (transistor)	I(4)	200	–	–	μA
t = 0 (V3 – 16 = 0)	I(4)	–	0	–	–
Video recorder switch (pin 11)					
Input voltage (Pin 11 low level)	V(11–16)	–	0 to 2.5	–	V
(Pin 11 to + V_{CC})	V(11–16)	–	9 to V(1–16)	–	V
Input current (Pin 11 low level)	I(11)	–	–	200	μA
(Pin 11 to + V_{CC})	I(11)	–	–	2	mA
OUTPUT SIGNALS					
Frame synchro pulses (positive) (pin 8)					
Output voltage (Peak value)	V(8–16)	10	11	–	V
Output impedance	R(8)	–	2	–	kΩ
Delay between leading edge of input signal and leading edge of output signal	t_{on}	–	15	–	μS
Delay between trailing edge of input signal and trailing edge of output signal	t_{off}	–	15	–	μS

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)
T_{amb} = 25°C, V1–V16 = 12 V (Unless otherwise specified).

Characteristic	Symbol	Min	Typ	Max	Unit
Sandcastle pulse (positive) (pin 7)					
Output voltage (Peak valve)	V(7–16)	10	11	–	V
Output impedance	R(7)	–	70	–	Ω
Output current during trailing edge	I(7)	–	2	–	mA
Sandcastle pulse width (V7 = 7V)	t_7	3.7	–	4.3	µS
Phase between middle input synchro pulse and leading edge of sandcastle pulse (V7 = 7V)	Δt	2.15	–	3.15	µS
Fly-back blanking pulse (pin 7)					
Output voltage (Peak valve)	V(7–16)	4	–	5	V
Output impedance	R(7)	–	70	–	Ω
Output current during trailing edge	I(7)	–	2	–	mA
Control pulse for horizontal driver (positive) (pin 3)					
Output voltage (Peak valve)	V(3–16)	–	10.5	–	V
Output impedance (Leading edge)	R(3)	–	2.5	–	Ω
(Trailing edge)	R(3)	–	20	–	Ω
Control pulse width V4 = 9.4 to V(1 – 16)	t_3	5.5	–	8.5	µS
V4 = 0 to 4V (note 3)	t_3	–	$14 + t_c$	–	µS
Control pulse is disabled for	V(1–16)	–	4	–	V
Overall phase relation ship					
Phrase between middle synchro pulse and middle fly-back pulse t_r = 12 µs (note 4)	t_z	1.9	–	3.3	µS
Sensitivity to current adjust	$\Delta I / \Delta t$	–	30	–	µA/µS
Oscillator (pins 14 and 15)					
Threshold voltage (low level)	V(14–16)	–	4.4	–	V
(high level)	V(14–16)	–	7.6	–	V
Current generator	I(14)	–	±0.47	–	mA
Free running frequency (C_{osc} = 4700 pF R_{osc} = 12 kΩ)	f	–	15625	–	Hz
Tolerance on frequency (note 5)	Δf	–	–	±5	%
Frequence control sensitivity	$\Delta f / I15$	–	31	–	Hz/µA
Spread of frequency	Δf	–	±10	–	%
Influence of supply voltage on frequency (note 5)	$\frac{\Delta f/f}{\Delta V/V \text{ nom.}}$	–	–	±0.05	%
Frequency change when decreasing the supply down to 5 V V (1 – 16) = 5 V (note 5)	Δf	–	–	±10	%
Frequency temperature cœfficient (note 5)	T	–	–	$\pm 10^{-4}$	/°K
Phase comparator ϕ 1 (pin 13)					
Control voltage range	V(13–16)	–	3.8 to 8.2	–	V
Control current (peak value)	I(13)	–	±1.9 to ±2.3	–	mA
Off-state output current (V (13 – 16) = 4 to 8 V)	I(13)	–	–	–1	µA

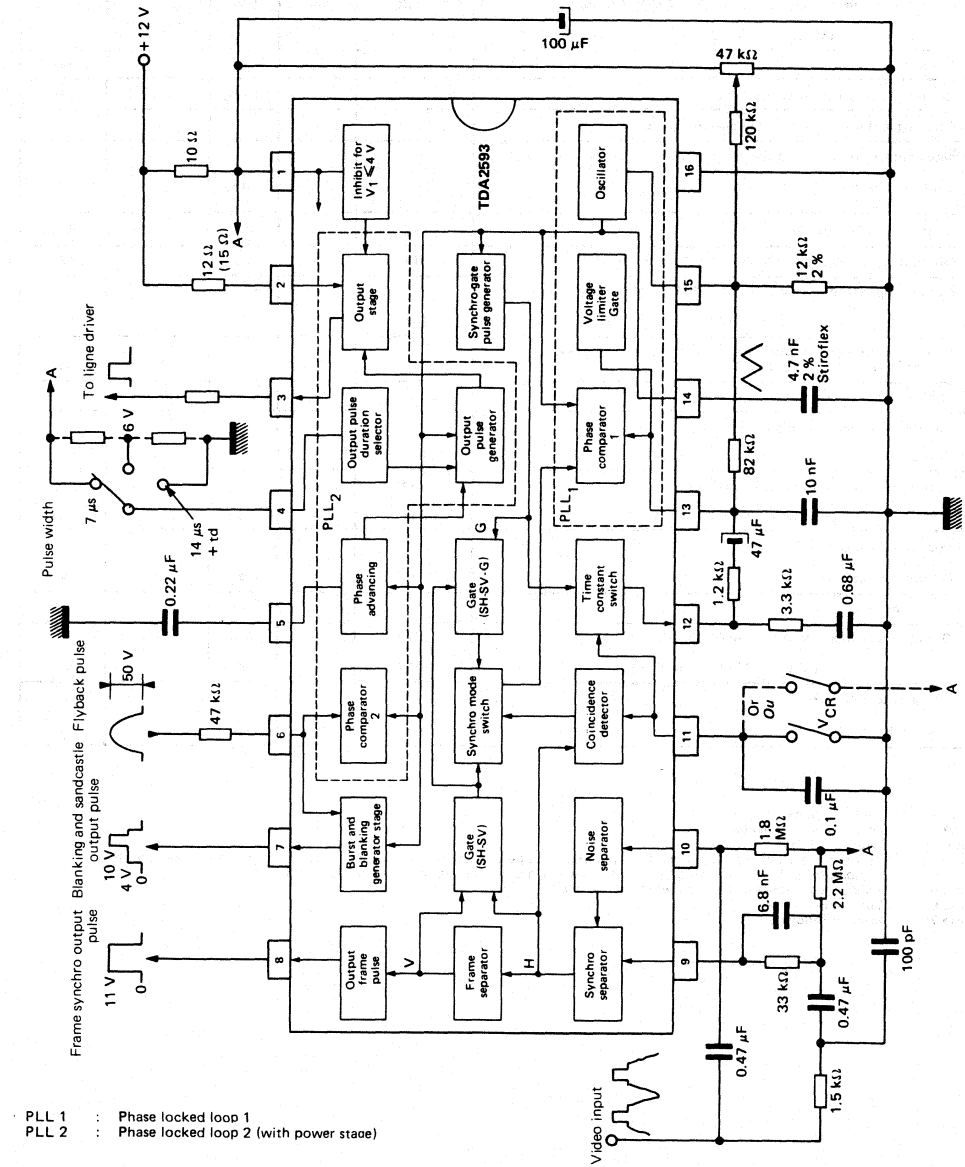
ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

T_{amb} = 25°C, V1–V16 = 12 V (Unless otherwise specified).

Characteristic	Symbol	Min	Typ	Max	Unit
Output impedance (V (13 – 16) = 4 to 8 V (note 6))	R(13)	–	High	–	–
(V (13 – 6) < 3.8 V or > 8.2 V (note 7))	R(13)	–	Low	–	–
Control sensibility		–	2	–	kHz/μS
Catching and holding range	Δf	–	± 780	–	Hz
Catching and holding range tolerance (note 5)	Δf/f	–	± 10	–	%
Phase comparator φ 2 and phase-shift (pin 5)					
Control voltage range	V(5–16)	–	5.4 to 7.6	–	V
Control current (Peak value)	I(5)	–	± 1	–	mA
Off-state output current (V (5 – 16) = 5.4 to 7.6 V)	I(5)	–	–	– 5	μA
Output impedance (V (5 – 16) = 5.4 to 7.6 V (note 6))	R(5)	–	High	–	–
(V (5 – 16) < 5.4 V or > 7.6 V)	R(5)	–	8	–	kΩ
Max. dalay between output pulse leading edge and fly-back pulse trailing edge (t_r = 12 μS)	t_d	–	–	15	μS
Static control error	$\Delta t/\Delta t_d$	–	–	0.2	%
Coïncidence detector φ 3 (pin 11)					
Output voltage	V(11–16)	–	0.5 to 6	–	V
Output current (without coïncidence)	I(11)	–	0.1	–	mA
(with coïncidence)	I(11)	–	– 0.5	–	mA
Time constant switch (pin 12)					
Output voltage	V(12–16)	–	6	–	V
Output current	I(12)	–	± 1	–	mA
Output impedance (V (11 – 16) = 2.5 to 7 V)	R(12)	–	100	–	Ω
(V (11 – 16) < 1.5 or 9 V)	R(12)	–	60	–	kΩ
Pulse generator (internal)					
Pulse width	t	–	7.5	–	μS

Note 1 : Allowed range 1 to 7 V
Note 2 : Or pin 4 not connected
Note 3 : With t_r = 12 μS
Note 4 : The adjustment of overall phase relation (and output pulse leading edge position) is automatically performed by phase comparator φ 2. If additional adjustment is needed, a current have to be imposed at pin 5.
Note 5 : Tolerance of peripheral components not included
Note 6 : Current generator
Note 7 : Emitter-follower

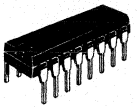
APPLICATION SCHEMA



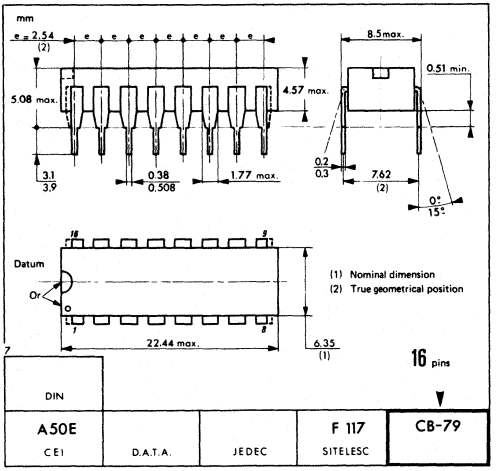
PLL 1 : Phase locked loop 1
PLL 2 : Phase locked loop 2 (with power stage)

PHYSICAL DIMENSIONS

CB-79



PLASTIC PACKAGE



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NOTES

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TEA2031A

COLOR TV EAST-WEST CORRECTION

The TEA2031A is intended to ensure frame rate modulated parabolic and keystone corrections to the horizontal deflection circuitry of 110° color TV sets.

The linear frame saw-tooth is applied to appropriate circuitry from which a corresponding parabolic waveform is obtained. This waveform is then fed to a comparator together with the linear line saw-tooth for comparison. Comparator's output drives the output power stage which is capable of sinking the external coil currents of up to 0.5 A.

An internal recovery diode feeds back to the power supply the coil fly-back current pulses of as high as 0.5 A.

Main features

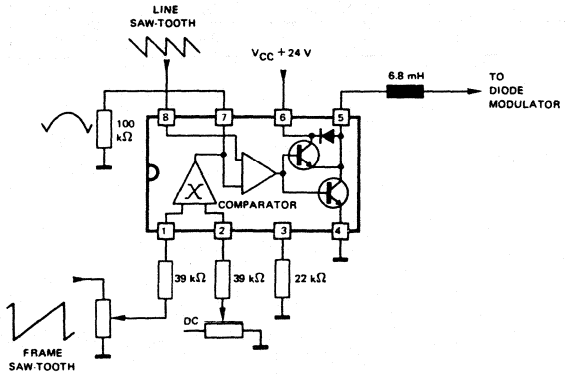
- Build in frame parabola from external saw-tooth.
- Parabola correction adjustment.
- Keystone correction adjustment.
- Line size adjustement.
- Line dynamic correction possibility (beam current).
- D Class output modulator with build in recovery diode.
- 50 or 60 Hz operation.
- Low dissipation.
- Few external components.

COLOR TV
EAST - WEST CORRECTION

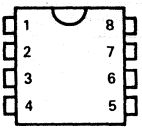
CASE CB-98

MINIDIP

BLOCK DIAGRAM



PIN ASSIGNMENT



1 - Multiplier input 1
2 - Multiplier input 2 (1 and 2 can be inverted)
3 - Current reference
4 - Ground
5 - Output
6 - V_{CC} power supply
7 - Multiplier output and comparator input 1
8 - Comparator input 2

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FUNCTIONAL DESCRIPTION

The TEA2031A is intended to provide to 110° color TV sets a parabolic and keystone frame rate modulated correction in addition to the main horizontal scanning.

A stable 6.3 V internal reference provides current and voltage references to the whole IC.

Pins 1 and 2 are two symmetrical inputs of an on-chip multiplier circuit and are internally held at 6.3 V reference potential level. Current inputs to these pins are drawn from external sources via appropriate resistors. The frame saw-tooth waveform which has a peak-to-peak value of around 3 volts and a mean value of about 2.5 volts, supplies the required current via a series resistor to pin 1. Likewise, the current to pin 2 is drawn through a series resistor from an external DC voltage source. These series resistors can have values of around 40 kΩ resulting in input currents of approximately 0.1 mA ± modulation current.

Pin 7 should be loaded to ground through a 100 kΩ resistor which as a result will produce a parabola of 5 volts peak-to-peak at pin 7. This parabola is symmetrical if the DC current flowing into pin 2 is equal to the mean input current of pin 1. Otherwise, the parabola becomes dissymmetrical and produces a keystone effect correction.

The line saw-tooth at pin 8 is obtained by feeding the line fly-back voltage through an integrator network formed by a diode and a grounded capacitor (see typical application diagram). The DC component of the line saw-tooth is compensated by an internal current sinking source; so that the mean DC values of line saw-tooth and frame parabola voltages are equal.

Line saw-tooth and frame parabola signals are applied to a comparator whose output is in the form of width modulated pulses. During every pulse duration, the output (pin 5) can sink external coil currents of up to 0.5 A associated with diode modulator of the main horizontal scanning circuit.

An internal recovery diode feeds back the fly-back energy of the coil to the power supply. This diode can carry currents of up to 0.5 A.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{6-4}	35	V
Output simk current	I_{5-4}	0.5	A
Diode output current	I_{5-6}	0.5	A
Input current	I_1 and I_2	− 0.5	mA
Storage temperature range		− 20 to + 150	°C

THERMAL OPERATING CHARACTERISTICS

$T_{amb} = + 50°C$

Characteristic	Symbol	Value	Unit
Thermal resistance	(R_{TH}. ja)	80	°C/W
Max total dissipated power	–	0.8	W

ELECTRICAL OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{6-4}	16	24	35	V
Supply current ($R_{(3-4)} = 22\ k\Omega$; $I_{OUT} = 0$)	I_6	–	4	6	mA
No load consumption ($R_{(3-4)} = 22\ k\Omega$, $I_{OUT} = 0$; $V_{(6-4)} = 24$ V)		–	100	150	mW
V Reference ($R_{(3-4)} = 22\ k\Omega$)	V_{3-4}	5.9	6.3	6.7	V
Frame saw-tooth input DC mean current $R_1 = 39\ k\Omega$ at 2.5 V mean - saw-tooth voltage.	I_1 mean	–	0.1	–	mA
Frame saw-tooth input peak-to-peak current $R_1 = 39\ k\Omega$ at 2.5 V mean - Saw-tooth voltage	I_{1pp}	–	70	–	µA
Keystone correction input DC current If I_1 mean $= I_2$: no keystone effect. $R_2 = 39\ k\Omega$ at 2.5 V DC ref.	I_2	–	0.1	–	mA
Keystone correction input DC current for maximum keystone effect	ΔI_2	–	± 12.5	–	µA
Top parabola voltage ($2\ V < V_1 = V_2 < 3V$)	V_{7H}	10	–	15	V
Top parabola temperature drift	ΔV_{7H}	–	–	0.5	mV/°C
Symmetrical parabola for no keystone effect (see figure 2)					
Parabola amplitude ($V_2 = 2.5$ V ; V_1 mean $= 2.5$ V , $V_{1pp} = 3$ V)	$V_{7H} - V_{7L}$	3.5	5.2	6	V
Parabola amplitude drift versus temperature	$\frac{\Delta(V_{7H} - V_{7L})}{}$	–	–	1	mV/°C
Symmetry	$\frac{V_{7H} - V_{7L1}}{V_{7H} - V_{7L2}}$	0.8	1	1.2	–
Maximum dissymmetrical parabola for maximum keystone effect (see figure 3)					
Parabola amplitude ($V_2 = 2$ V or $V_2 = 3$ V ; V_1 mean $= 2.5$ V ; $V_{1pp} = 3$ V)	$V_{7H} - V_{7B}$	5.3	8.5	9.2	V
Parabola amplitude ratio	$\frac{V_{7H} - V_{7B}}{V_{7H} - V_{7A}}$	2.6	–	4.1	–
Differential amplifier					
Input 8 sink current source		0.04	–	0.06	mA
Input 8 current drift versus temperature	$\Delta I_8 = F(\theta)$	–	–	0.1	%/°C
Transfer characteristics (pins 7-8) (F = 1 MHz)		5	–	500	mA/mV
Input noise (pins 7-8)		–	–	50	µV
Rise and fall time - Ioutput = 250 mA		1	–	–	A/µs
Output saturation voltage to ground ($I_5 = 0.5$ A)	V_{5-4}	–	–	1.2	V
Output saturation voltage to V_{CC} ($I_5 = 0.1$ A)	V_{6-5}	–	–	2	V
Output diode direct voltage ($I_5 = +0.5$ A)	V_{5-6}	–	–	1.2	V

PARABOLA OUTPUT

FIGURE 1

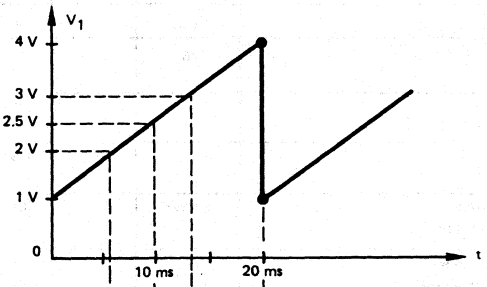


FIGURE 2

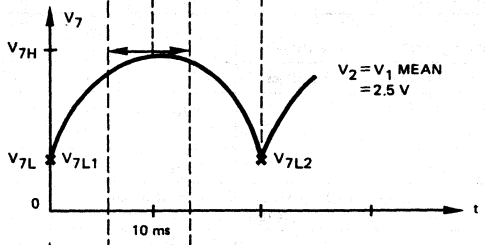
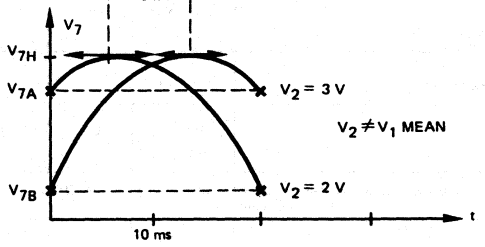
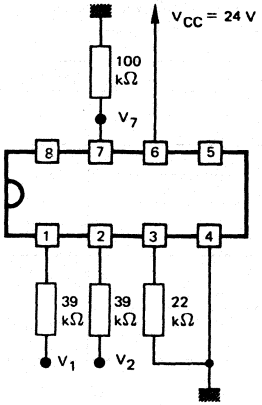


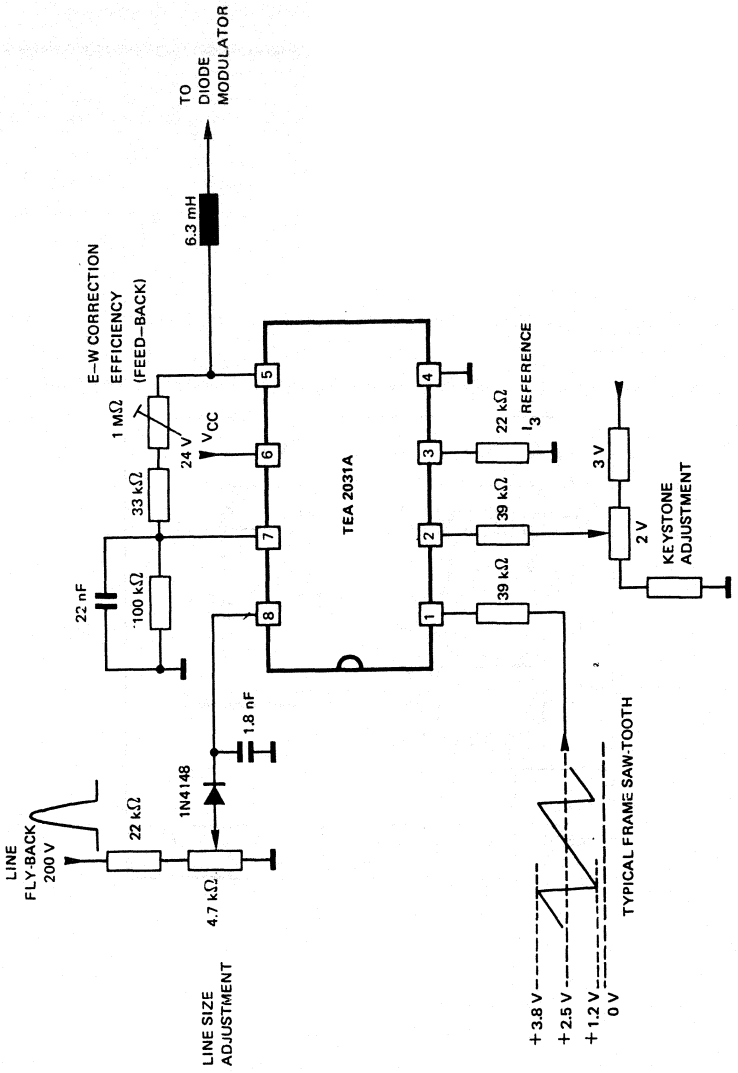
FIGURE 3



PARABOLA TEST DIAGRAM



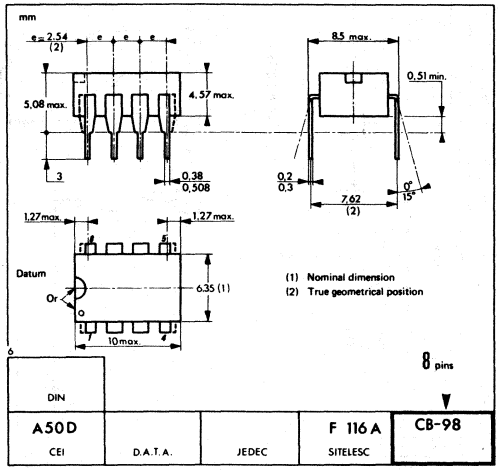
TYPICAL APPLICATION



PHYSICAL DIMENSIONS

CB-98

MINIDIP



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TEA2018A

CURRENT MODE SWITCHING POWER SUPPLY CONTROL CIRCUIT

The TEA2018A is an 8-pin mini-dip low cost integrated circuit designed for the control of switch mode power supplies.

Due to its current mode regulation, the TEA2018A facilitates design of power supplies with following features:

- High stability regulation loop.
- Automatic input voltage feed-forward in discontinuous mode fly-back.
- Automatic pulse-by-pulse current limitation.

Typical applications : Video Display Units, TV sets, typewriters, micro-computers and industrial applications.

Main features:

- Direct drive of the external switching transistor.
- Positive and negative output currents up to 0.5A.
- Current limitation.
- Demagnetization sensing.
- Full overload and short-circuit protection.
- Proportional base current driving.
- Low standby current before starting (< 1.6 mA).
- Thermal protection.

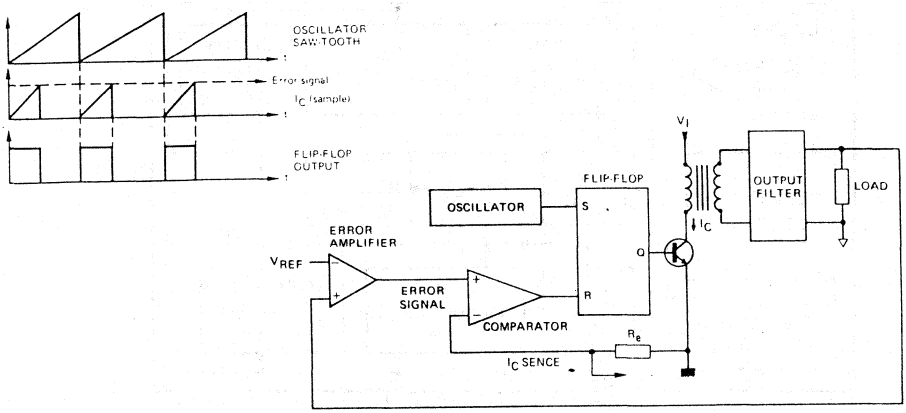
Where synchronization is required, use the TEA2019.

CURRENT MODE SWITCHING POWER SUPPLY CONTROL CIRCUIT

CASE CB-98

PLASTIC PACKAGE

CURRENT MODE CONTROL



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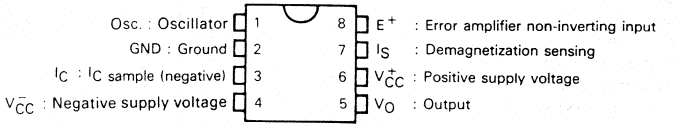
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Positive supply voltage	V_{CC}^{+}	15	V
Negative supply voltage	V_{CC}^{-}	−5	V
Peak output current (Duty cycle<5%)	I_O (peak)	±1	A
Input current (Pin 3)	I_I	±5	mA
Junction temperature	T_j	+150	°C
Operating ambient temperature range	T_{oper}	−20 to + 70	°C
Storage temperature range	T_{stg}	−40 to +150	°C

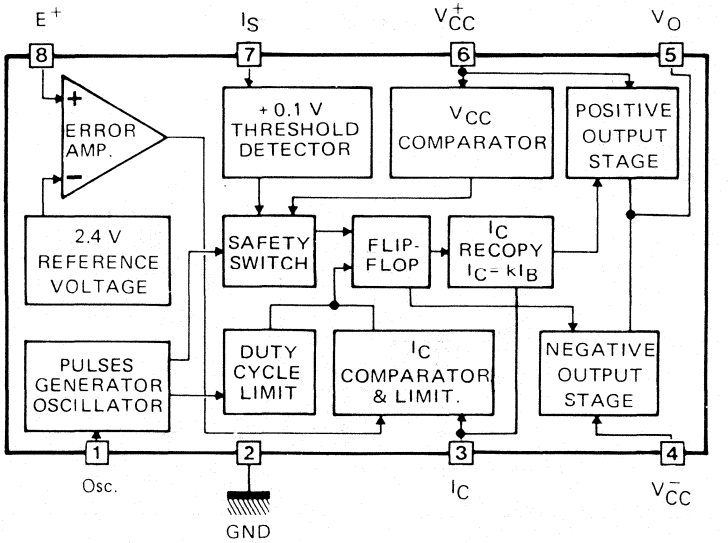
THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

PIN ASSIGNMENT



BLOCK DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = − 25°C, potentials referenced to ground (Unless otherwise specified)

Characteristic	Symbol	Min.	Typ	Max.	Unit
Positive supply voltage	V_{CC}	6.6	8	15	V
Negative supply voltage	V_{CC}	− 1	− 3	− 5	V
Minimum positive supply voltage required for starting (V_{CC} rising)	$V_{CC(start)}$		6.0	6.6	V
Minimum positive voltage below which device stops operating (V_{CC} falling)	$V_{CC(stop)}$	4.2	4.9	5.6	V
Hysteresis on V_{CC} threshold	ΔV_{CC}	0.7	1.1	1.6	V
Standby supply current before starting [$V_{CC} < V_{CC(start)}$]	$I_{CC(sb)}$		1	1.6	mA
Current limitation threshold voltage (pin 3)	$V_{th(I_C)}$	− 1100	− 1000	− 880	mV
Current sample input resistance	R_{sample}		1000		Ω
Demagnetization sensing threshold	I_S	75	100	125	mV
Demagnetization sensing input current (Pin 7 grounded)			1		μA
Maximum duty cycle	τ_{max}	60	70		%
Error amplifier gain	A_V		50		
Error amplifier input current (Non-inverting input)	I_i		2		μA
Internal reference voltage	$V_{(ref)}$	2.3	2.4	2.5	V
Reference voltage temperature drift	$\frac{\Delta V_{(ref)}}{\Delta T}$		10^{-4}		V/°C
Oscillator frequency drift with temperature (V_{CC} = + 8 V)	$\frac{\Delta f_{osc}}{\Delta T}$		0.05		%/°C
Oscillator frequency drift with V_{CC} (+ 8 V < V_{CC} < + 14 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$		0.5		%/V
Minimum conducting time (C_t = 1 nF)	$t_{on}(min)$		2		μs

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min.	Typ	Max.	Unit
Positive supply voltage	V_{CC}		8		V
Negative supply voltage	V_{CC}		− 3		V
Output current	I_O			0.5	A

GENERAL DESCRIPTION

OPERATING PRINCIPLES (Figure 1)

On every period, the beginning of the conduction time of the transistor is triggered by the fall of the oscillator sawtooth which acts as clock signal. The period T_{osc} is given by:

$$T_{osc} = 0.66\, C_t (R_t + 2000)$$

(T_{osc} in seconds, C_t in Farad, R_t in Ohm)

The end of the conduction time is determined by a signal issued from comparing the following signals:

a) the sawtooth waveform representing the collector current of the switching transistor, sampled across the emitter shunt resistor,

b) the output of the error amplifier.

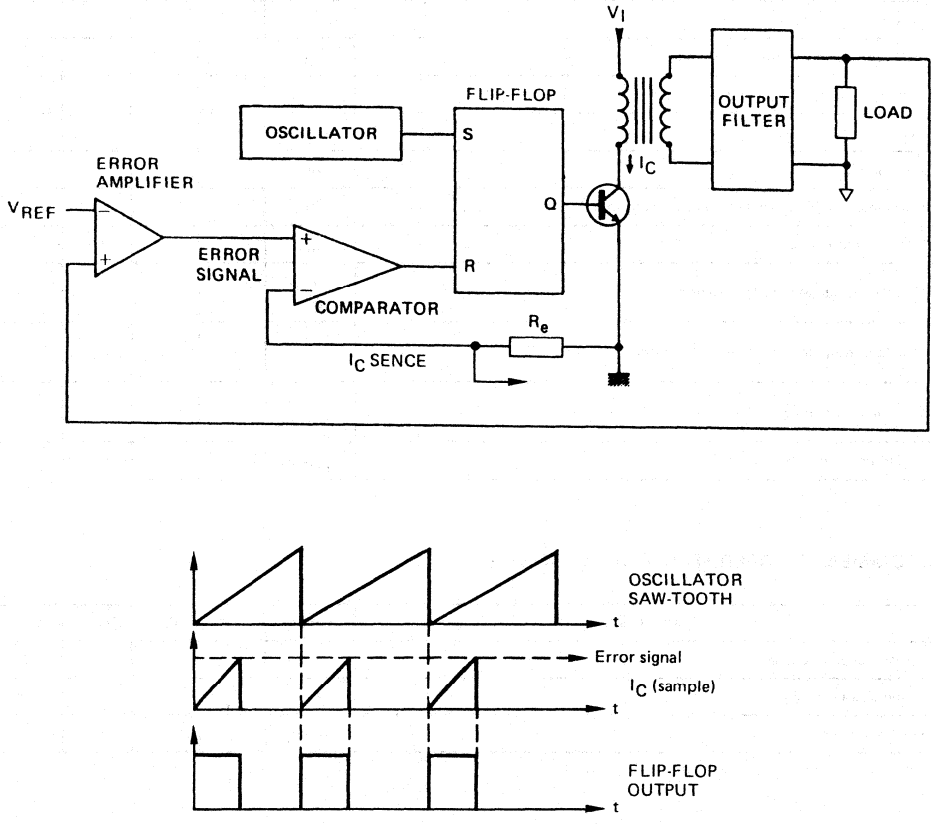


FIGURE 1 — CURRENT MODE CONTROL

BASE DRIVE

- **Fast turn-on**
  On each period, a current pulse ensures fast transistor switch-on.
  This pulse performs also the $t_{on(min)}$ function at the beginning of the conduction.

- **Proportional base drive**
  In order to save power, the positive base current after the starting pulse becomes an image of the collector current.
  The ratio $\frac{I_C}{I_B}$ is programmed as follows (Figure 2):

$$\frac{I_C}{I_B} = \frac{R_B}{R_e}$$

- **Efficient and fast switch-off**
  When the positive base drive is removed, 1 μs (typically) will elapse before the application of negative current therefore allowing a safe and rapid collector current fall.

SAFETY FUNCTIONS

- **Overload & short-circuit protection**
  When the voltage applied to pin 3 exceeds the current limitation threshold voltage [$V_{th(Ic)}$], the output flip-flop is reset and the transistor is turned off.
  The shunt resistor R_e must be calculated so as to obtain the current limitation threshold on pin 3 at the maximum allowable collector current.

- **Demagnetization sensing**
  This function disables any new conduction cycle of the transistor as long as the core is not completely demagnetized.
  When not used, pin 7 must be grounded.

- **$t_{on(max)}$**
  Outside the regulation area and in the absence of current limitation, the maximum conduction time is set at about 70% of the period.

- **$t_{on(min)}$**
  A minimum conducting time is ensured during each period (see figure 2).

- **Supply voltage monitoring**
  The TEA2018A will stop operating if V_{CC}^{+} on pin 6 falls below the threshold level $V_{CC(stop)}$.

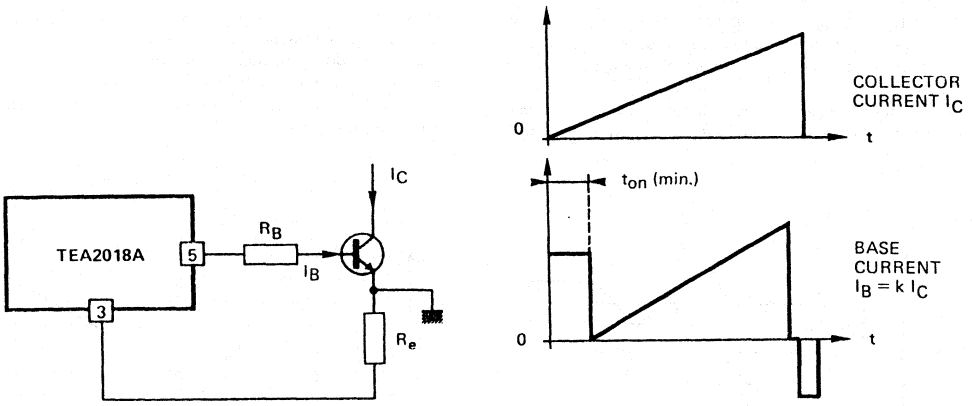
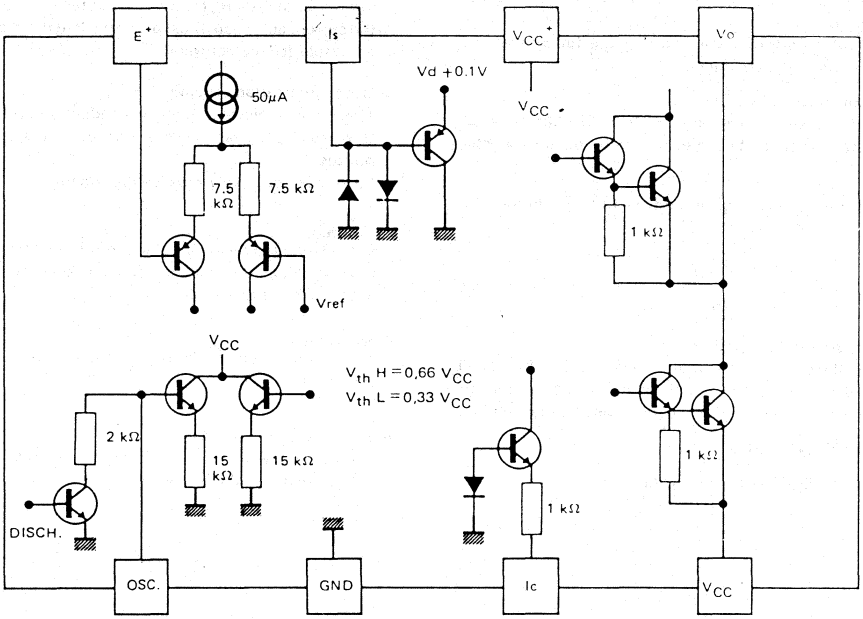


FIGURE 2

SCHEMATICS OF INPUTS AND OUTPUTS



STARTING PROCESS (Figure 3)

Prior to starting, a low current is drawn from the high voltage source through a high value resistor.

This current charges the power supply storage capacitor of the device.

No output pulses are available before the voltage on pin 6 has reached the threshold level [$V_{CC(start)}$, V_{CC} rising].

During this time the TEA2018A draws only 1 mA (typically). When the voltage on pin 6 reaches this threshold, base drive pulses appear.

The energy drawn by these pulses tends to discharge the power supply storage capacitor. However a hysteresis of about 1.1 V (typically) (ΔV_{CC}) is implemented to avoid the device from stopping.

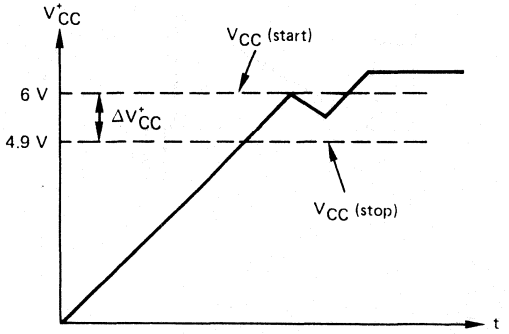


FIGURE 3 — NORMAL TEA2018A START-UP SEQUENCE

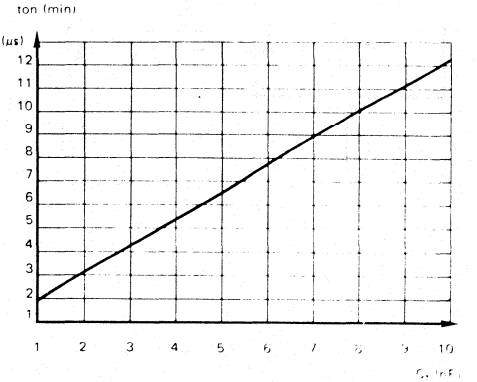
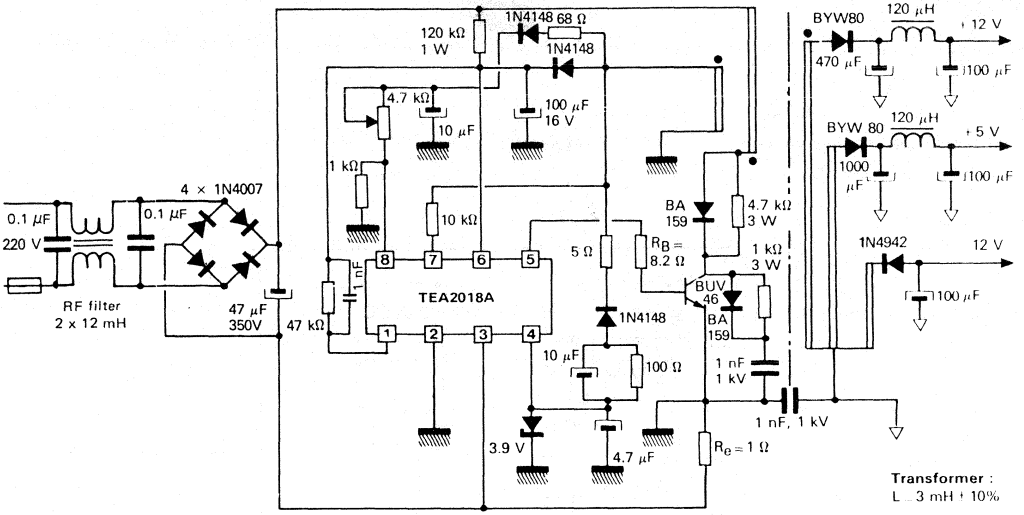


FIGURE 4 — t_{on}(min) VERSUS C_t

TYPICAL APPLICATION



MONITOR APPLICATION

- Maximum power ≃ 30 W
- Operating frequency ≃ 30 kHz
- $I_{nominal}$: 0.75 A
- I_{limit} : 1 A

$$R_e = \frac{1\ V}{1\ A} = 1\ \Omega$$

$$R_B = 8.2\ \Omega \Rightarrow \frac{I_C}{I_B} = 8.2$$

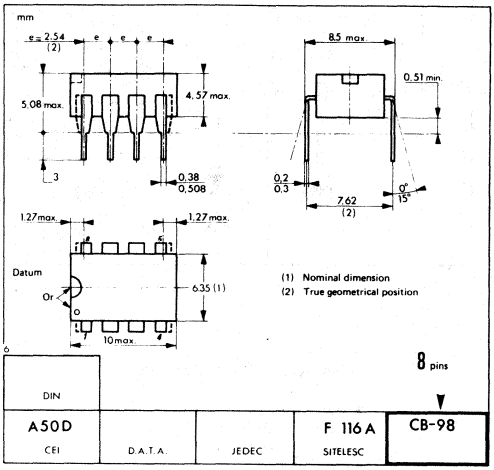
Note : Primary Ground

Secondary Ground

PHYSICAL DIMENSIONS

CASE CB-98

PLASTIC PACKAGE



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THOMSON COMPONENTS SEMICONDUCTEURS

TEA2019

CURRENT MODE SWITCHING POWER SUPPLY CONTROL CIRCUIT

The TEA2019 is an 14-pin mini-dip low cost integrated circuit designed for the control of switch mode power supplies. It has the same basic functions as the TEA2018A but with synchronization capability by internal PLL. It is particularly switable for applications where oscillator synchronization is required.

Due to its current mode regulation, the TEA2019 facilitates design of power supplies with following features:

- High stability regulation loop.
- Automatic input voltage feed-forward in discontinuous mode fly-back.
- Automatic pulse-by-pulse current limitation.

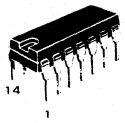
Typical applications : Video Display Units, TV sets, typewriters, micro-computers and industrial applications.

Main features:

- Direct drive of the external switching transistor.
- Positive and negative output currents up to 0.5A.
- Current limitation.
- Demagnetization and power transistor saturation sensing.
- Full overload and short-circuit protection.
- Proportional base current driving.
- Low standby current before starting (< 1.6 mA).
- Synchronization capability with internal PLL.
- Thermal protection.

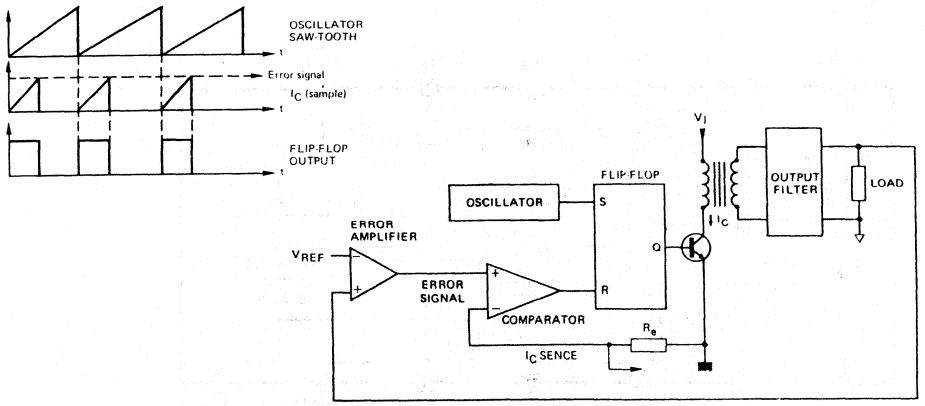
CURRENT MODE SWITCHING POWER SUPPLY CONTROL CIRCUIT

CASE CB-2



PLASTIC PACKAGE

CURRENT MODE CONTROL



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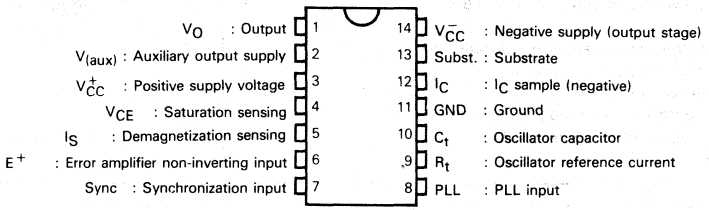
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Positive supply voltage	V_{CC}^{+}	15	V
Auxiliary output supply voltage	$V_{(aux)}$	15	V
Negative supply voltage	V_{CC}^{-}	−5	V
Peak output current (Duty cycle<5%)	I_O (peak)	±1	A
Input current (Pins 4-5)	I_I	±5	mA
Junction temperature	T_j	+150	°C
Operating ambient temperature range	T_{oper}	−20 to + 70	°C
Storage temperature range	T_{stg}	−40 to +150	°C

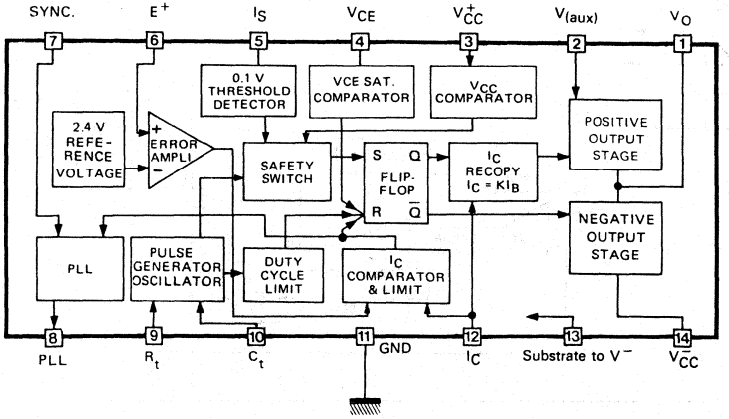
THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

PIN ASSIGNMENT



BLOCK DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = +25°C$, potentials referenced to ground (Unless otherwise specified)

Characteristic	Symbol	Min.	Typ	Max.	Unit
Positive supply voltage	V_{CC}^{*}	6.6	8	15	V
Negative supply voltage	V_{CC}	- 1	- 3	- 5	V
Minimum positive supply voltage required for starting (V_{CC}^{*} rising)	$V_{CC(start)}$	-	6.0	6.6	V
Minimum positive voltage below which device stops operating (V_{CC}^{*} falling)	$V_{CC(stop)}$	4.2	4.9	5.6	V
Hysteresis on V_{CC}^{*} threshold	ΔV_{CC}^{*}	0.7	1.1	1.6	V
Standby supply current before starting [$V_{CC}^{*} < V_{CC(start)}$]	$I_{CC(sb)}$	-	1	1.6	mA
Current limitation threshold voltage (pin 12)	$V_{th(I_C)}$	- 1100	- 1000	- 880	mV
Current sample input resistance	R_{sample}	-	1000	-	Ω
Demagnetization sensing threshold	I_S	75	100	125	mV
Demagnetization sensing input current (Pin 5 grounded)	-	-	1	-	μA
Maximum duty cycle	τ_{max}	70	80	-	%
Error amplifier gain	A_V	-	50	-	
Error amplifier input current (Non-inverting input) (pin 6)	I_I^{*}	-	2	-	μA
Internal reference voltage	$V_{(ref)}$	2.3	2.4	2.5	V
Reference voltage temperature drift	$\frac{\Delta V_{(ref)}}{\Delta T}$	-	10^{-4}	-	V/°C
Oscillator frequency drift with temperature ($V_{CC}^{*} = +8$ V)	$\frac{\Delta f_{osc}}{\Delta T}$	-	0.05	-	%/°C
Oscillator frequency drift with V_{CC}^{*} ($+8$ V $< V_{CC}^{*} < +14$ V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	-	0.5	-	%/V
Minimum conducting time ($C_t = 1$ nF)	$t_{on(min)}$	-	2	-	μs

SYNCHRONIZATION INPUT (PIN 7)

Peak to peak sawtooth voltage	V_{7pp}	–	0.5	2.5	V
Input impedance	$R_{(7)}$	–	20		kΩ

PLL CHARACTERISTICS

$C_t = 1.5$ nF, $R_t = 68$ kΩ, $R_{(8-9)} = 50$ kΩ, $+I_B / -I_B - 1.25$, $V_{7pp} - 0.5$ V
(See typical application)

Frequency sensitivity	–	–	100		Hz/μA
Capture range ($T_O = 64$ μs)	ΔT	–	± 8		μs

SATURATION SENSING (PIN 4)

Input threshold	$V_{(4)}$	–	3.2		V
Input current ($V_4 > 3.2$ V)	$I_{(4)}$	50	–		μA
Input internal resistance	–	–	1		kΩ

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min.	Typ	Max.	Unit
Positive supply voltage	V_{CC}		8		V
Negative supply voltage	V_{CC}		3		V
Output current	I_O			0.5	A

GENERAL DESCRIPTION

OPERATING PRINCIPLES (Figure 1)

On every period, the beginning of the conduction time of the transistor is triggered by the fall of the oscillator saw-tooth which acts as clock signal. The period T_{osc} is given by:

$$T_{osc} = 0.66\ C_t\ (R_t + 2000)$$

(T_{osc} in seconds, C_t in Farad, R_t in Ohm)

The end of the conduction time is determined by a signal issued from comparing the following signals.

a) the sawtooth waveform representing the collector current of the switching transistor, sampled across the emitter shunt resistor,

b) the output of the error amplifier

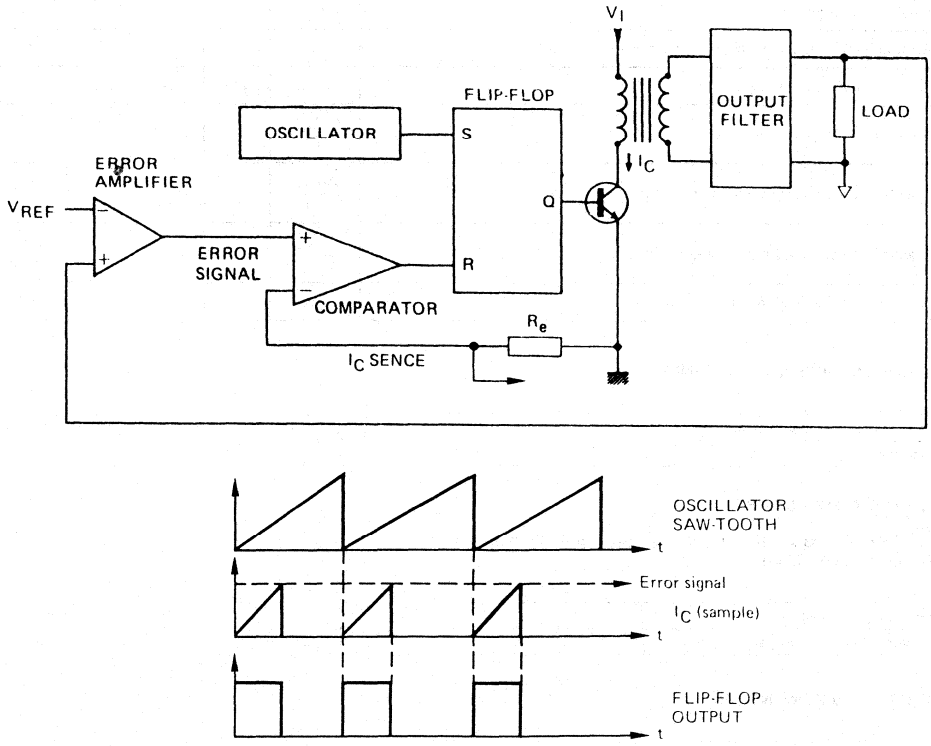


FIGURE 1 – CURRENT MODE CONTROL

BASE DRIVE

- **Fast turn-on**
  On each period, a current pulse ensures fast transistor switch-on.
  This pulse performs also the $t_{on(min)}$ function at the beginning of the conduction.

- **Proportional base drive**
  In order to save power, the positive base current after the starting pulse becomes an image of the collector current.
  The ratio $\frac{I_C}{I_B}$ is programmed as follows (Figure 2):

$$\frac{I_C}{I_B} = \frac{R_B}{R_e}$$

- **Efficient and fast switch-off**
  When the positive base drive is removed, 1 μs (typically) will elapse before the application of negative current therefore allowing a safe and rapid collector current fall.

SAFETY FUNCTIONS

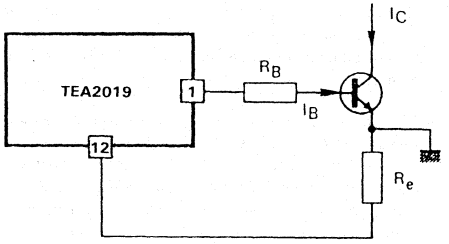
- **Overload & short-circuit protection**
  When the voltage applied to pin1-2 exceeds the current limitation threshold voltage [$V_{th(Ic)}$], the output flip-flop is reset and the transistor is turned off.
  The shunt resistor R_e must be calculated so as to obtain the current limitation threshold on pin12 at the maximum allowable collector current.

- **Demagnetization sensing**
  This function disables any new conduction cycle of the transistor as long as the core is not completely demagnetized.
  When not used, pin 5 must be grounded.

- **$t_{on(max)}$**
  Outside the regulation area and in the absence of current limitation, the maximum conduction time is set at about 70% of the period.

- **$t_{on(min)}$**
  A minimum conducting time is ensured during each period (see figure 2).

- **Supply voltage monitoring**
  The TEA2019 will stop operating if V_{CC}^{+} on pin 3 falls below the threshold level $V_{CC(stop)}$



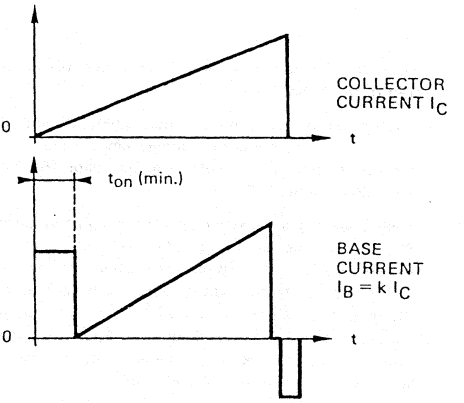


FIGURE 2

STARTING PROCESS (Figure 3)

Prior to starting, a low current is drawn from the high voltage source through a high value resistor.
This current charges the power supply storage capacitor of the device.
No output pulses are available before the voltage on pin 3 has reached the threshold level [$V_{CC(start)}$, $V_{CC}^{\cdot}$ rising].
During this time the TEA2019 draws only 1 mA (typically). When the voltage on pin 3 reaches this threshold, base drive pulses appear.
The energy drawn by these pulses tends to discharge the power supply storage capacitor. However a hysteresis of about 1.1 V (typically) ($\Delta V_{CC}^{\cdot}$) is implemented to avoid the device from stopping.

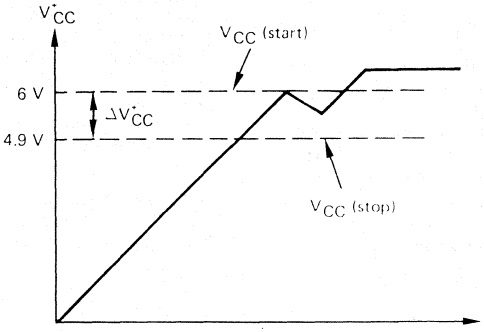
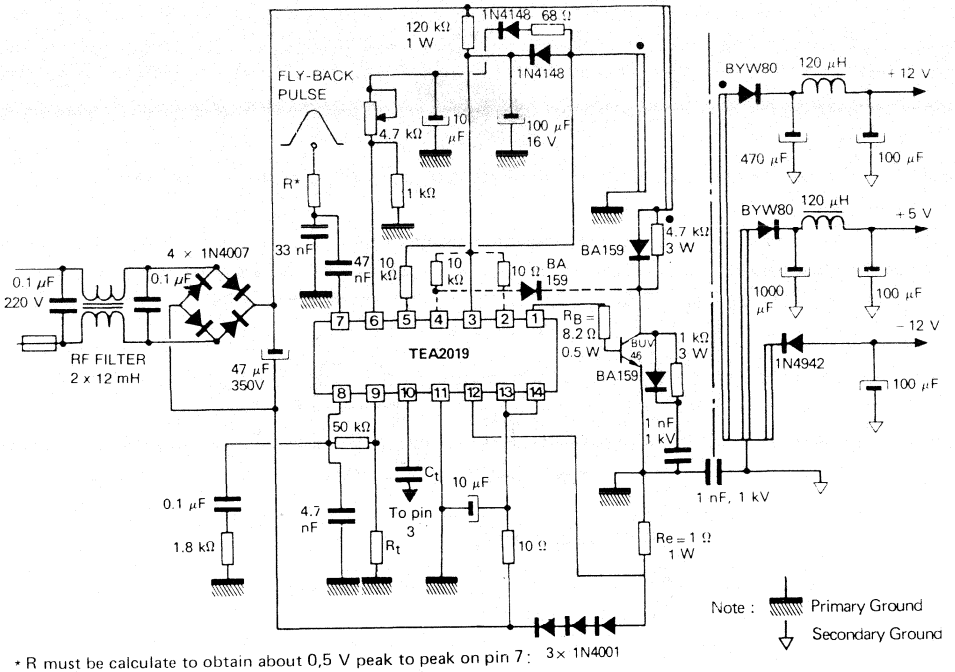


FIGURE 2 – NORMAL TEA 2019 START-UP SEQUENCE

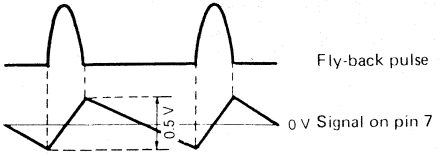
THE TEA2019 has some additional capabilities compared to the TEA2018A:

- The oscillator charge current its supplied through an internal current generator, programmed externally - instead of using an external charging resistor. The sawtooth so obtained is linear.
- The oscillator can be synchronized through an internal PLL circuit. This feature provides synchronization between the external sync pulse and the end of the switching transistor current. The sync pulse can be for example the fly-back pulse of a TV horizontal sweep circuit. As indicated in the application diagram, this pulse is applied first to a R.C. network to obtain a low voltage sawtooth and then to pin 7 of the circuit. The PLL output (pin 8) supplies a correction current to pin 9 through an external resistor, so as to maintain the oscillator at the correct frequency.
- In the TEA2019, the power supply of the positive output stage is separated from the main power supply, so that it can be supplied from a lower voltage in order to reduce the I.C. power dissipation.
  For low power applications, the circuit can be normally supplied by connecting pins 2 and 3 together.
- In order to proted the substrate (pin 13) from the parasitic voltage peaks produced by negative output current peaks at pin 14, the substrate (pin 13) is internally separated from the negative supply (pin 14). They must be externally connected together.
- The switching transistor saturation voltage can be monitored at pin 4. To achieve this, a high voltage diode must be connected between the collector of the switching transistor and pin 4. Also a resistor must be connected from pin 4 to $V_{CC}^{\cdot}$ (see application diagram). This arrangement is useful when the chosen value of base current is very low and as a consequence the saturation voltage will be high. In this event, when $V_{CE(sat)}$ increases above 2.5 V, the base current is interrupted before the normal end of the period.
  Remark: the TEA2019 can also operate without this protection.

TYPICAL APPLICATION



* R must be calculate to obtain about 0,5 V peak to peak on pin 7 : 3× 1N4001



MONITOR APPLICATION

- **Maximum power** ≃ 30 W
- **Operating frequency** ≃ F_{line}

  = 15.625 Hz R_t = 68 KΩ C_t = 1.5 nF

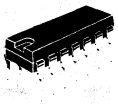
- $I_{nominal}$: 0.75 A
- I_{limit} : 1 A

$$R_e = \frac{1\ V}{1\ A} = 1\ \Omega$$

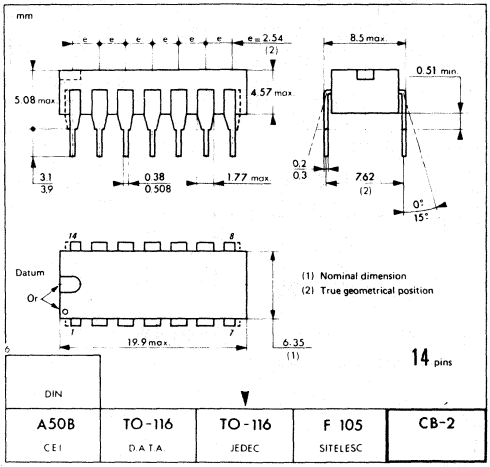
with R_B = 8.20 Ω we obtain $\frac{I_C}{I_B} = 8.2$

PHYSICAL DIMENSIONS

CB-2



PLASTIC PACKAGE



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TEA2162

SWITCH MODE POWER SUPPLY PRIMARY CIRCUIT

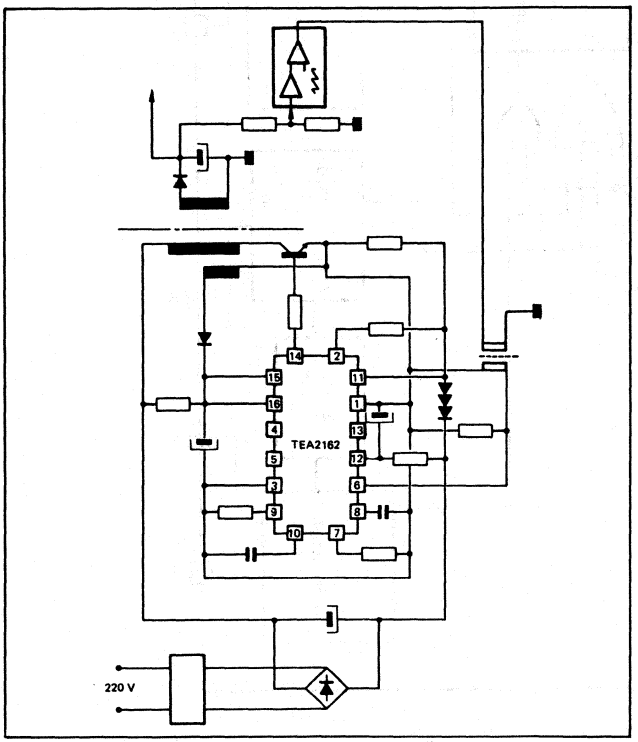
ADVANCE INFORMATION

The TEA2162 is a switch mode power supply control integrated circuit especially designed to perform according to the "master slave" concept.

Consequently the TEA2162 takes place in the primary side of an off-line SMPS, it receives from a secondary circuit regulation signals and it ensures the base drive and protection of a switching power transistor.

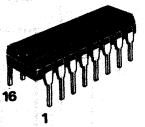
Main features

- Direct drive of the switching power transistor.
- Positive and negative output currents up to 1 A.
- Switching transistor collector current limitation.
- Optional transformer demagnetization sensing.
- Under and overvoltage lock-out.
- Low stand-by current before starting.
- Soft starting by progressive current limitation.



SWITCH MODE POWER SUPPLY PRIMARY CIRCUIT

CASE CB-79



PLASTIC PACKAGE

PIN ASSIGNMENT

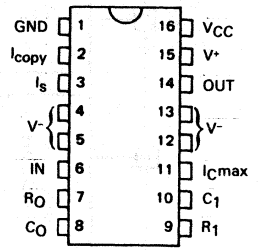


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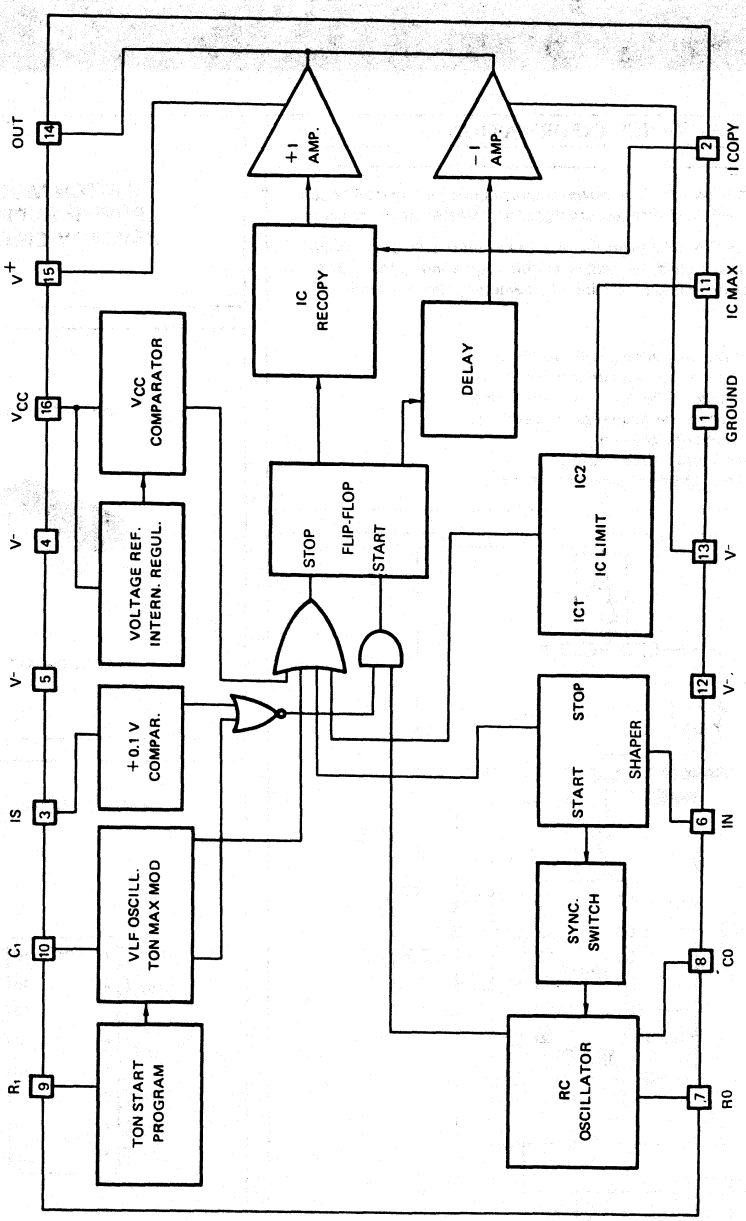
FIGURE 1 : TEA2162 SIMPLIFIED BLOCK DIAGRAM



MAXIMUM RATINGS

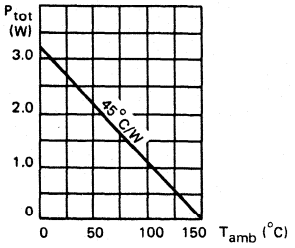
Rating	Symbol	Value	Unit
Positive power supply V_{16} - V_1	V_{CC}	+ 18	V
Positive power supply V_{15} - V_1	V^+	+ 18	V
Negative power supply $V_{4,5,12,13}$ - V_1	V^-	— 5	V
Total power supply V_{16} - $V_{4,5,12,13}$	V_{CC} - V^-	20	V
or	or		
V_{15} - $V_{4,5,12,13}$	V^+ - V^-	20	V
Positive output current	I_{out}^+	1.5	A
Negative output current	I_{out}^-	1.5	A
Voltage on pin 6 (IN)	V_6 - V_1	± 3	V
Operating junction temperature	T_j	150	°C
Operating ambient temperature range	T_{oper}	— 20 to + 70	°C
Storage temperature range	T_{stg}	— 40 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal resistance			
Junction case	$R_{th(j-c)}$	11	°C/W
Junction ambient	$R_{th(j-a)}$*	45	°C/W

* Soldered on a 35 μm thick 40 cm² PC board copper area.

MAXIMUM POWER DISSIPATION



RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Positive power supply	V_{CC}	-	10	15	V
Negative power supply (absolute value)	$\|V^-\|$	0	-	5	V
Total power supply	$V_{CC} - V^-$	-	-	18	V
Positive output current	I_{out}^+	-	-	1	A
Negative output current	I_{out}^-	-	-	1	A
Switching frequency	F_{sw}	-	-	50	kHz
Oscillator resistor	R_O	30	-	150	kΩ
Oscillator capacitor	C_O	0.45	-	3	nF

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = +25°C$, potentials referenced to ground (pin 1).
(Unless otherwise specified).

Characteristic	Symbol	Min	Typ	Max	Unit
Starting voltage on V_{CC} (V_{CC} increasing)	$V_{CC\ start}$	-	9	-	V
Stopping voltage on V_{CC} (V_{CC} decreasing)	$V_{CC\ stop}$	-	6.2	-	V
Starting positive supply current (V_{CC} = 8 V)	$I_{CC\ start}$	-	0.8	-	mA
Positive supply current (V_{CC} = 10 V)	I_{CC}	-	6	-	mA
Current limitation first threshold	V_{ICM1}	-	−1	-	V
Current limitation second threshold	V_{ICM2}	-	−1.3	-	V
Is input threshold	V_{IS}	-	+100	-	mV
Input threshold	V_{IN}	-	±200	-	mV
Output current amplifier gain	I_{out}/I_{Icopy}	-	1 000	-	-

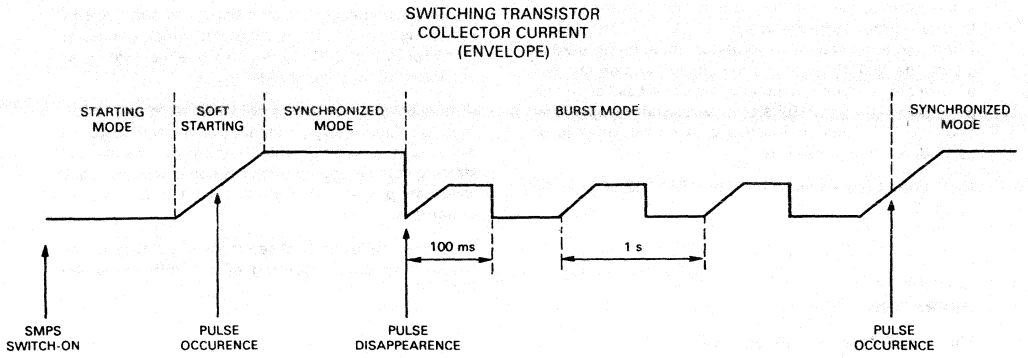


FIGURE 2 : EXAMPLE OF SEQUENCE OF STARTING UP AND SECURITY FUNCTION (TIMES ARE EXAMPLES OF TYPICAL TIMES).

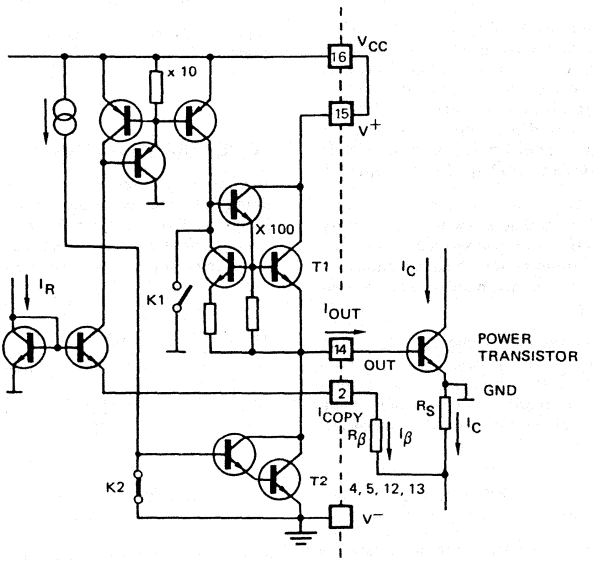


FIGURE 3 : OUTPUT STAGE SIMPLIFIED DIAGRAM

GENERAL DESCRIPTION

The integrated circuit TEA2162 takes place in the primary side of an isolated off-line switch mode power supply. During normal operation the circuit receives conduction signals from a secondary regulator circuit (integrated or discret device), through a small pulse transformer, and achieves an efficient switching transistor base drive and protection. The TEA2162 also ensures starting operation and SMPS protection in case of overload, off-load or secondary regulator failure.

A simplified block diagram of the TEA2162 is given by figure 1.

OPERATION

Three modes can be distinguished :

— the starting mode,
— the "Burst" mode (or security mode),
— the synchronized mode (or normal operating mode).

— The starting mode occurs when V_{CC} is less than 9 V typ, V_{CC} increasing, or less than 6.2 V typ, V_{CC} decreasing, due to an hysteresis of 2.8 V typ. In this mode the switching transistor remains cut-off and the supply current of the I_C is very low : typically 0.8 mA.

— The burst mode occurs when V_{CC} is greater than 9 V (or 6.2 V due to the hysteresis). In this mode the switching transistor receives conduction signals organized in burst. The switching frequency is fixed by external components R_O and C_O. The duration between two consecutive bursts is fixed by external capacitor C_1. A typical burst period is about 1 s. The burst duration is fixed internally to the circuit to 10% of the burst period.

During the burst mode, the maximum duty cycle of conduction is programmed by an external resistor R_1 in order to limit the power transmitted during this mode. The current limitation threshold is modified by an internally programmed law in order to achieve an efficient soft starting.

— The synchronized mode occurs when V_{CC} is greater than 9 V (or 6,2 V due to the hysteresis) and the input receives from the secondary regulation and synchronization signals. In this mode, the conduction of the switching power transistor is controlled by the secondary regulator.

— Sequence
The typical sequence after SMPS switching on is Starting mode → Burst mode → Synchronized mode.

During the starting mode the current I_{CC} is very low (typically 0.8 mA), so the I_C can be supplied by a high impedance generator, for example a high value low power resistor connected to the rectified mains, which charges the filtering capacitor of V_{CC}. In addition the switching transistor remains cut-off eliminating all risks of erratic operation during V_{CC} establishment. When V_{CC} reaches 9 V the I_C goes into the burst mode. The switching transistor receives conduction signals. Due to an efficient soft starting by collector current limitation and duty cycle limitation, a limited energy is transferred to the secondary of the SMPS. Under normal condition this energy is sufficient for supplying the secondary regulator which generates synchronization and regulation signals providing an accurate output voltage regulation.

In case of synchronization pulses missing (secondary regulator failure, regulation loop open), the TEA2162 remains in burst mode indefinitely or returns into the starting mode (depending on the application). In each case the power transmitted by the power supply remains very low.

Figure 2 is an example of sequence of starting up and security function triggering of a SMPS using the TEA2162.

POWER TRANSISTOR CONTROL

The sophisticated output stage of the TEA2162 offers high performance control of the power transistor :

— fast turn-on by virtue of high positive base current,
— transistor held in conduction by base current proportional to collector current,
— fast turn-off by virtue of high negative base current.

Figure 3 is a simplified diagram of the TEA2162 output stage.

POWER TRANSISTOR CONDUCTION

To minimize the base current, it is made a direct function of the necessary collector current with respect of a programmable forced gain β_f. A negative I_C sample is obtained across the shunt resistor R_S. As the potential of pin I copy is internally maintained to ground :

$$R_\beta . I_\beta = R_S . I_C$$

T_1 is a current source such as :

$$I_{out} = 1\,000 \, . \, I_\beta \text{ (internal gain)}$$

So :
$$\frac{I_{out} . R_\beta}{1\,000} = R_S \, I_C$$

$$\beta_f = \frac{I_C}{I_{out}} = \frac{R_\beta}{R_S} \times \frac{1}{1\,000}$$

R_S must be calculated first to obtain the current limitation when the negative voltage across it reaches 1 V.

$$R_S = \frac{1\ V}{I_{C\,max}} \qquad \text{So} \qquad R_\beta = 10^3 \times R_S \times \beta_f$$

At the output current beginning, a constant width pulse is delivered to make the switching transistor quickly saturated.

POWER TRANSISTOR TURN-OFF

After a fast positive base current cut-off, the negative base current occurs by darlington T_2 switching-on. A 0.7 μs delay allows to remove the collector and base charges off and eliminates all risks of simultaneous conduction of T_1 and T_2.

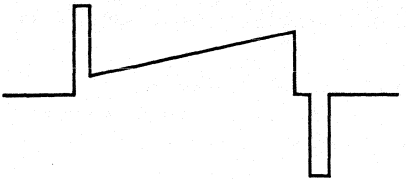


FIGURE 4 : TYPICAL BASE CURRENT WAVEFORM

COLLECTOR CURRENT LIMITATION

The TEA2162 contains a double threshold current limitation device.

When the first threshold I_{CM1} is reached the switching transistor is turned-off for the period but this action is not memorized.

In some converters, in case of hard over-load, the current may continue increasing in spite of the first threshold current limitation triggering (generally on account of the storage time of bipolar power transistors). For that reason a second threshold : I_{CM2} exists.

$$I_{CM2} = I_{CM1} \times 1.3$$

When this threshold is reached, the power transistor is turned-off and this is memorized in an internal flip-flop. So the output voltage decreases, the regulation pulses disappear and the TEA2162 returns in the burst-mode. It remains in this mode as long as the overload occurs.

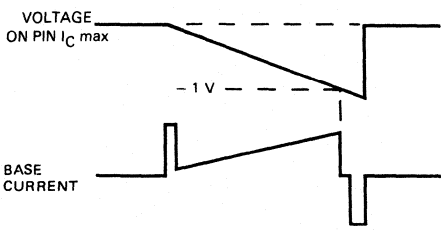


FIGURE 5 : CURRENT LIMITATION TRIPPING

I_{CM1} ADAPTATION DURING BURST-MODE

To achieve an efficient soft-starting the threshold I_{CM1} is internally reduced during the burst-mode.

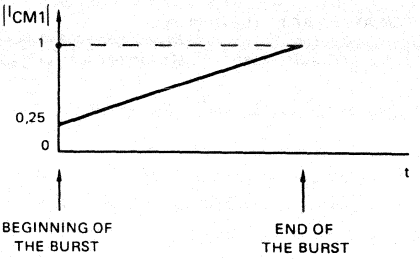


FIGURE 6 : I_{CM1} ADAPTATION DURING THE BURST FOR ACHIEVING A "SOFT-START"

SWITCHING OSCILLATOR - SYNCHRONIZATION

In the burst-mode the switching frequency is fixed by an internal oscillator, the frequency of which is determined by two external components : C_O and R_O.

$$Fo \simeq \frac{3}{2} \times \frac{1}{R_O C_O}$$

(neglecting the sawtooth return duration).

The return of the sawtooth corresponds to the discharge of C_O in an internal resistor. Typical value is 0.9 μs for C_O = 1 nF.

To get the synchronization, the free frequency F_o must be slightly lower than the frequency of synchronization (Typically: $T_o < Tsync < 0.65 \times T_o$). The synchronization pulses are applied to a small isolation transformer constitued only of two few turns windings on a ferrite stick and separated by the necessary space to get the required mains isolation.

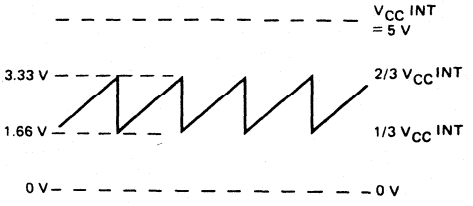


FIGURE 7 : SAWTOOTH AVAILABLE ON CAPACITOR C_O

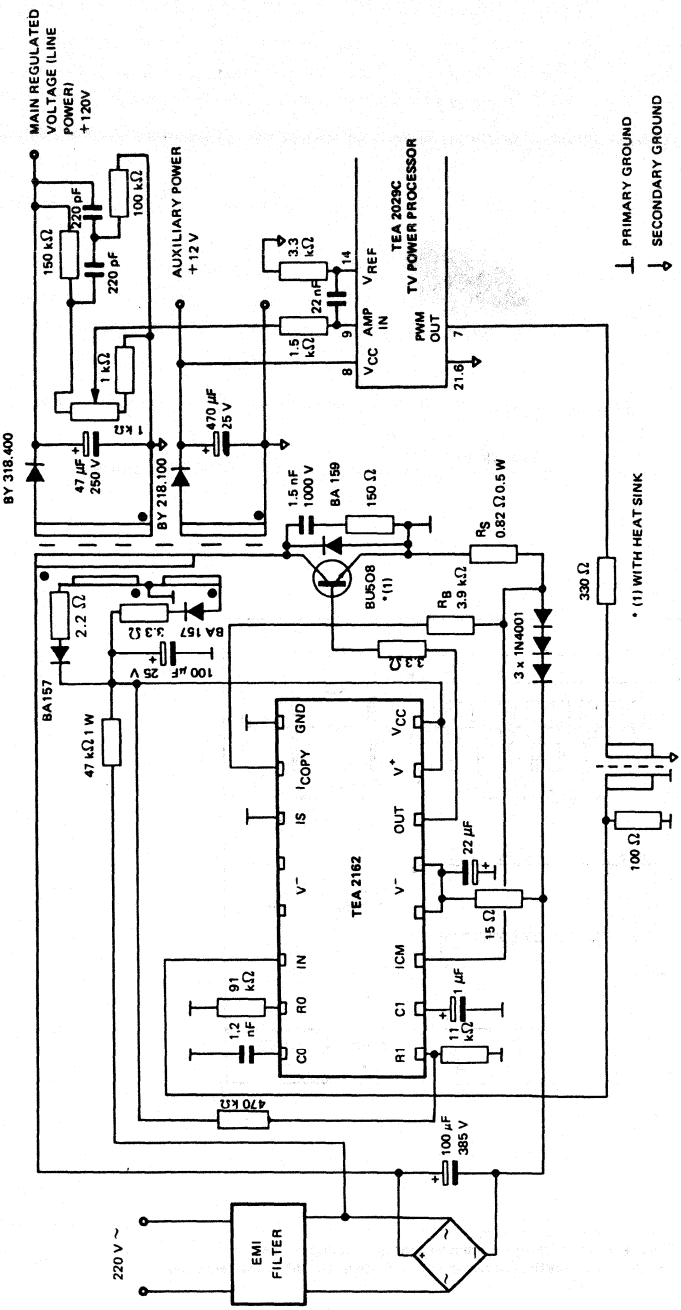
The secondary produces a derivated voltage : a positive pulse for the beginning of conduction and a negative pulse for the end.

The TEA2162 is sensitive to such positive and negative pulses on pin 6. The sensitivity is ± 0.2 V.

OVERVOLTAGE PROTECTION

The circuit is protected against overvoltage by V_{CC} supply voltage checking. If this voltage reaches 15 V an internal comparator set a flip-flop which stops output conduction signals. In the normal use of the circuit, this causes the supply voltage to decrease since the circuit is self-powered by the SMPS. In addition to integrated circuit protection, this device provides a full SMPS output protection against overvoltages, when the supply voltage (V_{CC}) is proportional to the output voltage (depending on the application). It is also possible to sense the input voltage of the SMPS using correctly coupled windings.

TEA2162 TYPICAL APPLICATION : 90 W FLY-BACK SMPS FOR TV SET



Main features :

Input voltage range : 220 V + 10%

Main output voltage regulation :

Line : $\frac{\Delta V_{out}}{V_{out}} \leqslant 0.6\%$

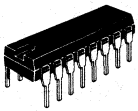
Load : $\frac{\Delta V_{out}}{V_{out}} \leqslant 0.25\%$

for 15 W < P_{out} < 90 W

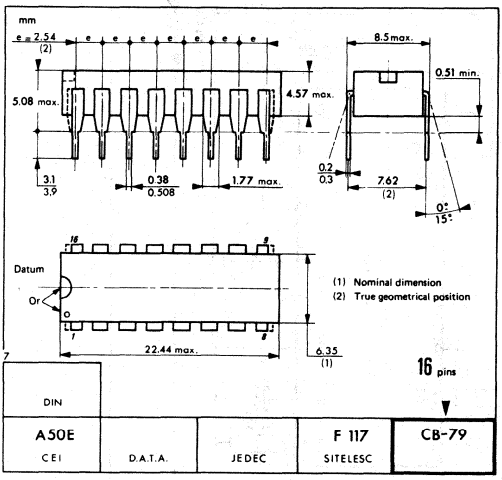
Efficiency : 86% typ. at nominal power.

PHYSICAL DIMENSIONS

CB-79



PLASTIC PACKAGE



These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

THOMSON COMPONENTS SEMICONDUCTEURS

UAA4006B

SWITCH MODE POWER SUPPLY CONTROL CIRCUIT

ADVANCE INFORMATION

The UAA4006B is a regulation and control device for fly-back switch mode power supplies using one external switching transistor.

- Includes oscillator, PWM and error amplifier
- Direct drive of the switching transistor
- Self-regulated positive base current (peak 1.5 A)
- Negative base current providing fast turn-off and allowing the best use of the safe operating area (peak 1.5 A)
- Switching transistor protected against saturation failure
- Instantaneous collector current limitation
- Positive power supply monitoring
- On chip thermal protection
- Adjustable minimum conducting time for use of a snubber circuit
- Internal reference voltage
- Start up with very low supply current

SWITCH MODE POWER SUPPLY CONTROL CIRCUIT

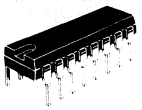
ORDERING INFORMATION

PART NUMBER	PACKAGE	
	DP	SP
UAA4006B	•	•

Example : UAA4006BDP

CASES

CB-79



DP SUFFIX
PLASTIC PACKAGE

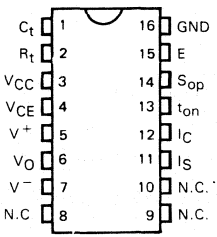
CB-501

SP SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENTS

(Top view)

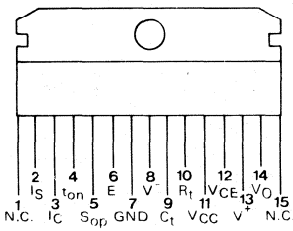
CB-79



C_t	:	Oscillator timing capacitor
R_t	:	Oscillator timing resistor
V_{CC}	:	Supply voltage
V_{CE}	:	$V_{CE(sat)}$ sensing
V^+	:	Power stage positive supply
V_O	:	Power stage output
V^-	:	Power stage negative supply
I_S	:	Secondary current monitoring input
I_C	:	Primary current limit input
t_{on}	:	$t_{on(max)}$ limit access
S_{op}	:	Amplifier output
E	:	Amplifier input
GND	:	Ground

(Front view)

CB-501



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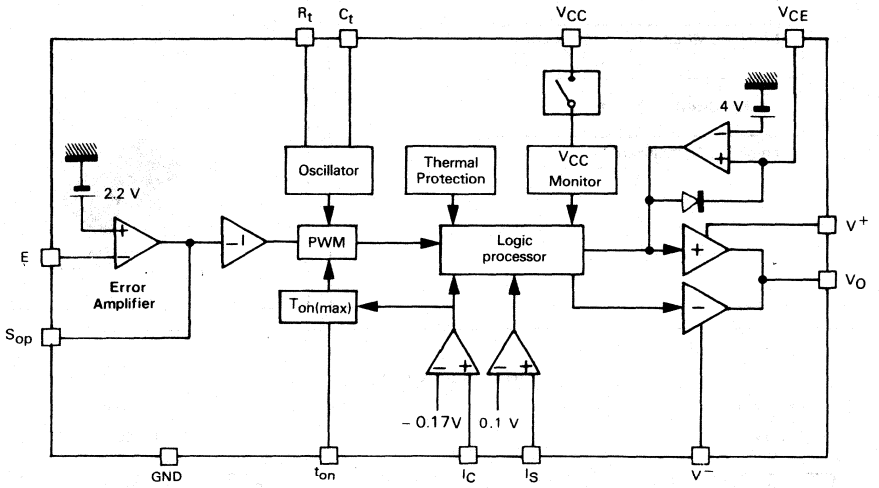
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	+15	V
Supply voltages (Power stage) Positive Negative	V^+ V^-	+15 −6	V V
Voltage between pins 11 and 13	$V^+ - V^-$	+18	V
Output current	I_O	±1.6	A
Current into input I_C (internal protection diodes)	–	±5	mA
Current into input I_S	–	±5	mA
Junction temperature range	T_j	−40 to +150	°C
Storage temperature range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	CB-79	CB-501	Unit
Maximum junction-ambient thermal resistance	$R_{th(j-a)}$	50	40	°C/W
Maximum junction-case thermal resistance	$R_{th(j-c)}$	7	2.5	°C/W

BLOCK DIAGRAM



CASE	C_t	R_t	V_{CC}	V_{CE}	V^+	V_O	V^-	NC	I_S	I_C	t_{on}	S_{op}	E	GND
CB-79	1	2	3	4	5	6	7	8, 9, 10	11	12	13	14	15	16
CB-501	9	10	11	12	13	14	8	1, 15	2	3	4	5	6	7

CIRCUIT DESCRIPTION

OSCILLATOR

The oscillator provides a triangular waveform with a fall time much smaller than the rise time. The voltage swings between +1.5 V and about $V_{CC}/2$. The maximum operating frequency is 60 kHz, the period being given by $T_{osc} = 0.5 R_t C_t$ Resistor R_t adjusts the frequency, but determines also the value of $t_{on(min)}$ (see logic processor).

PULSE WIDTH MODULATOR (PWM)

The variable duty-cycle signal is elaborated by comparing the oscillator voltage (pin C_t) to the inverted error amplifier output voltage. Another comparator determines the maximum value of the duty-cycle by comparing the oscillator signal with the voltage on pin "t_{on}". If $V(t_{on}) = 0$, then the maximum duty-cycle is internally set to 0.67 T_{osc}, otherwise, the maximum duty-cycle is given by :

$$\left(\frac{t_{on}}{T_{osc}}\right) max = 1 - \frac{R_{ton}}{2R_t}$$

(valid only if $R_{ton} > 0.67\ R_t$, where R_{ton} is the resistor inserted between t_{on} pin and ground).

CURRENT LIMITATION

A level lower than I_C threshold on pin I_C involves two actions :

- a direct action through the logic processor which stops the drive until the end of the oscillator period ;
- an indirect action through the t_{on} funtion. The change of state at the output of comparator I_C is applied to pin t_{on} as long as the overload current persists. By inserting capacitor C_B between pin t_{on} and V_{CC} (about 0.1 μF), the voltage at this point rises by a quantity ΔV proportional to the duration and the frequency of the overcurrent.

This will consequently lower the maximum conduction ratio, thus decreasing the frequency of the overcurrent. At the end of an overload condition, capacitor C_B slowly charges up through a 20k internal impedance, in order to return progressively to normal operation.

NOTE : If capacitor C_B is omitted, direct action will only be implemented.

SUPERVISION OF THE SECONDARY CURRENT

In order to avoid the magnetization of the transformer core in case of short-circuits or heavy overloads on the secondary winding, a new cycle of conduction can only begin after the secondary current has completly fallen to zero.
This task is accomplished by comparator I_S which threshold is 0.1 V and detects the zero crossing of the secondary current.

PROTECTION AGAINST DESATURATION

If, because of a too low base current or a too heavy load, the collector to emitter voltage of the switching transistor rises above 4 V approximately, the output of comparator V_{CE} changes state, and the drive is interrupted.

ERROR AMPLIFIED

This is an operational amplifier whose open loop gain is greater than 1000. The input current are less than 3 μA, and the input offset voltage is lower than 5 mV.
The input common-mode voltage range is 0 V to (V_{CC} — 3 V).
Due to an internal limitation the output source current of the amplifier is about 4 mA.

START SWITCH

An internal switch is inserted between pin V_{CC} supply line and internal voltage.
During power-up, this switch closes when V_{CC} reaches + 8.4 V. The leakage current (I_{CC})L is about 0.4 mA before the switch closes. This original feature enables starting the converter by means of a high value resistance directly connected between V_{CC} and the high supply voltage. The smoothing capacitor on V_{CC} supply provides the energy required for the start. The turn-off of the internal switch requires that V_{CC} falls below + 6.2 V.

THERMAL PROTECTION

This protection becomes active when the junction temperature reaches +160°C.

LOGIC PROCESSOR

A logic unit processes the information coming from the fault detectors, and ensures that the output signal fulfils two conditions :

- No double pulsing with a period : the occurrence of a hault detection is memorized until the end of the period.
- To allow the discharge of a snubber network, the minimum width of the output pulse is set at a given value $t_{on(min)}$ by an internal monostable. If this monostable is not triggered, there will be no conduction. The duration $t_{on(min)}$ is programmable by resistor R_t using (see figure 1).

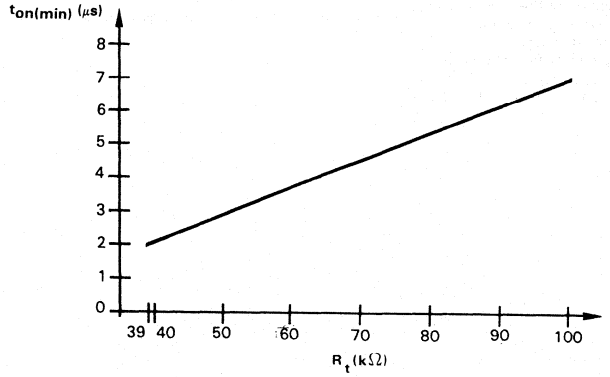
ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = +25°C$, $V_{CC} = +10$ V, $V^- = -5$ V
(Unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	–	–	14	V
Rise supply voltage threshold	V_{CCR}	7.7	8.4	9.1	V
Fall supply voltage threshold	V_{CCF}	5.5	6.2	6.9	V
Hysteresis on V_{CC} threshold	ΔV_{CC}	1.6	2.2	2.5	V
Current I_{CC} (V_{CC} under threshold voltage)	–	–	0.4	1	mA
Supply current ($V_{CC} = +10$ V)	I_{CC}	–	10	–	mA
Positive supply voltage (Power stage)	V^+	4	–	15	V
Negative supply voltage (Power stage)	V^-	−6	–	−1	V
Threshold of input I_C	$I_{C(th)}$	−188	−172	−156	mV
I_C input current ($V_{(I_C)} = 0$ V)	–	–	5	20	μA
Threshold of input I_S	$I_{S(th)}$	0.065	0.1	0.135	V
I_S input current ($V_{(I_S)} = 0$ V)	–	–	5	20	μA
Error amplifier open-loop gain	A_V	60	–	–	dB
Error amplifier offset voltage	V_{IO}	–	5	–	mV
Internal reference voltage	$V_{(ref)}$	2.1	2.2	2.3	V
Oscillator frequency $f_{osc} = \frac{1}{T_{osc}}$	f_{osc}	–	$2/R_tC_t$	60	kHz
Value of resistance R_t (See figure 1)	R_t	39 –	– –	100 –	kΩ
Output current ($V^+ - V_S = 3$ V, $V_S - V^- = 3$ V)	I_O	±1.5	–	–	A
V_{CE} comparator threshold voltage	$V_{CE(th)}$	3.6	4	4.4	V
$t_{on(min)}$ adjustment range $R_t = 39$ kΩ (See figure 1) $R_t = 100$ kΩ	–	– –	2 7	– –	μs
Max duty cycle : $\left(\frac{t_{on}}{T_{osc}}\right)_{max}$ ($R_{ton} > 0.67\ R_t$) - Note 1 ($R_{ton} < 0.67\ R_t$)	– –	– –	$1 - \frac{R_{ton}}{2R_t}$ 0.67	– –	– –
Oscillator frequency drift with temperature ($V_{CC} = 12$ V)	–	–	0.02	0.05	%/°C
Oscillator frequency drift with V_{CC}	–	–	0.2	0.5	%/V

Note 1 : $R_{t_{on}}$ externally connected between pin "t_{on}" and GND
R_t externally connected between pin "R_t" and GND

FIGURE 1 - $t_{on(min)}$ ADJUSTMENT RANGE (V_{CC} = 10 V)



OUTPUT STAGE

ON-state

The positive stage achieves a very efficient drive of the switching transistor.
Its features are essentially :

- Direct drive (neither inductor, nor tranformer) ;
- The transistor stays in a quasi-saturation mode, and thus has a reduced storage time ;
- The drive energy is strictly limited to the required amount ;
- Easy implementation.

K_1 is closed to turn the positive stage on. The maximum value of the positive base current is determined by the external limitation resistor R (between V_{CC} and V^+).
Diode D maintains Q in a quasi-saturation mode : the more Q is saturated, the more diode D will shunt an important part of the drive current I_{B1}, through diode D_1.
Resistor R_B has a low value (about 1 Ω), and is used to stabilize the regulation loop. For a good efficiency of the negative drive, the value of this resistor should be as low as possible.
Integrated Darlington T_1 is able to supply a peak current of 1.5 A with a 2 V saturation voltage.
The voltage V_{CE} on transistor Q is :
$V_{CE} = V_D + R_B I_{B1}$

OFF-state

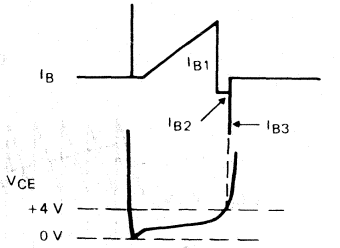
The turn off is accomplished in two steps :

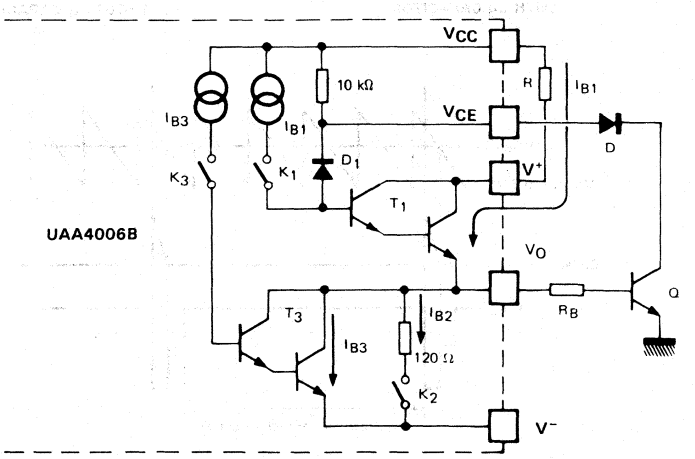
- an immediate action through K_2 which connects the base of the switching transistor to the negative supply through a 120 Ω integrated resistor (current I_{B2}) :
- a detayed action through K_3 which is closed only after the desaturation of the external transistor. This is detected by comparator V_{CE}, when the collector to emitter voltage reaches 4 V.

Darlington T_3 can supply 1.5 A with a 2 V saturation voltage (current I_{B3}).

NOTE : The negative drive I_{B3} for the removal of the stored charges is delayed in order to limit the slope dI_B/dt at the on-off transition. A high dI_B/dt might indeed lead to a destructive overheating of the base-collector junction (see "The power transistor in its environment" published by Thomson-CSF Division Semiconducteurs Discrets).

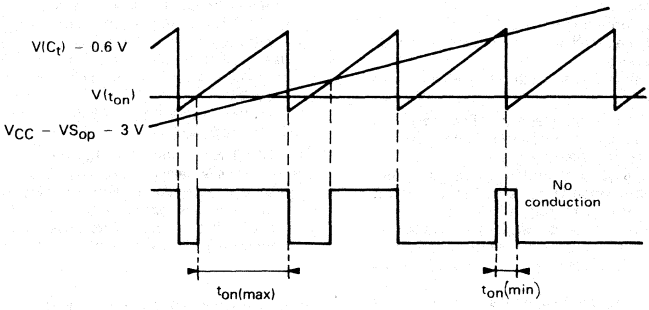
SELF REGULATED BASE CURRENT $I_B = f(V_{CE})$



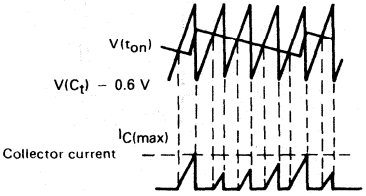


TYPICAL WAVEFORMS

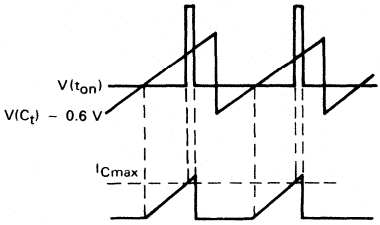
LIMITS OF THE DUTY CYCLE



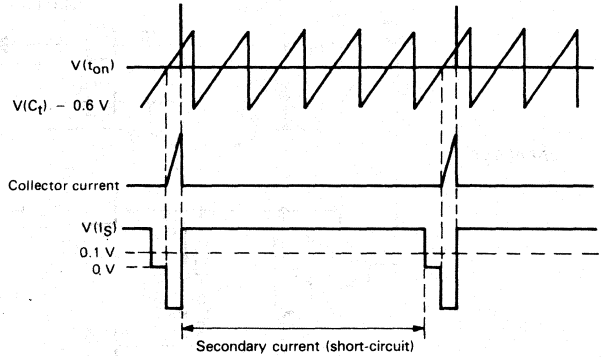
CURRENT LIMITATION



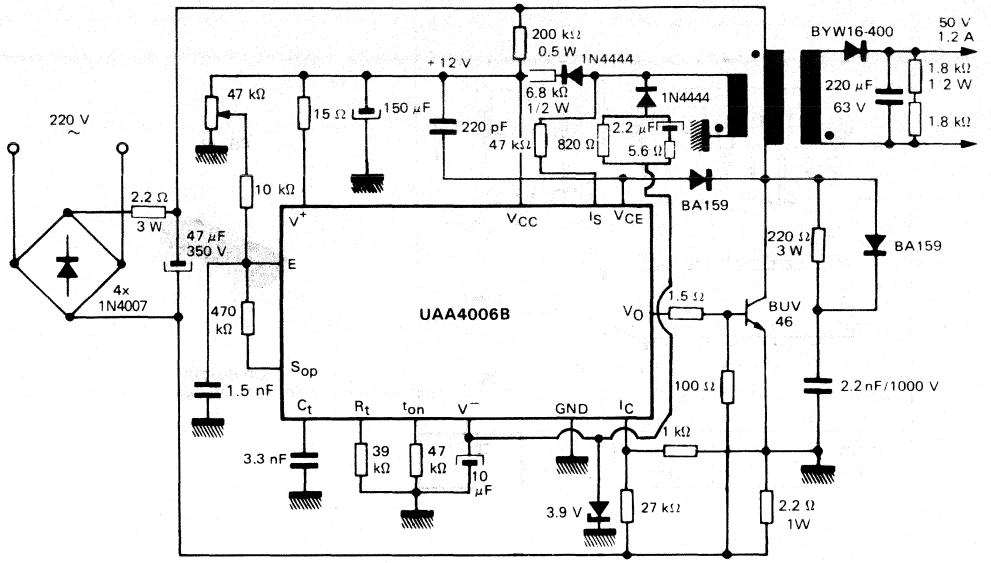
WITH C_B CAPACITOR



WITHOUT C_B CAPACITOR

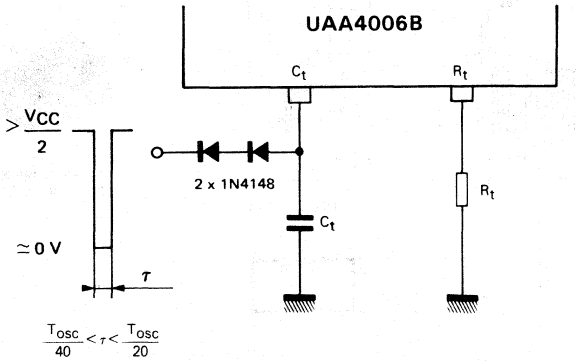


50 W FLY-BACK CONVERTER

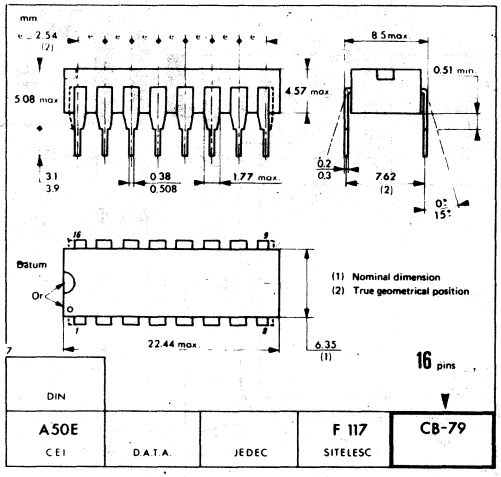


EXTERNAL SYNCHRONIZATION

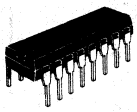
The oscillator may be synchronized to an external frequency f_{ext} so that : $f_{osc} < f_{ext} < 1.2\ f_{osc}$



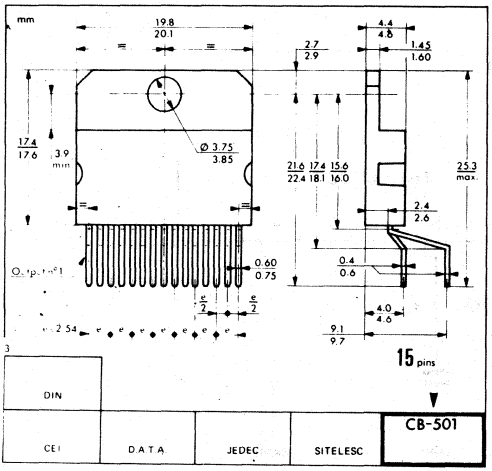
PHYSICAL DIMENSIONS



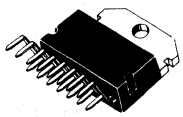
CB-79



DP SUFFIX
PLASTIC PACKAGE



CB-501



SP SUFFIX
PLASTIC PACKAGE

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Please inquire with our sales offices about the availability of the different packages.

Printed in France

TEA5101

RGB HIGH VOLTAGE VIDEO AMPLIFIER

ADVANCE INFORMATION

DESCRIPTION

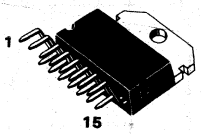
The TEA5101 includes three video amplifiers realised with a high voltage DMOS/bipolar technology. It drives directly the three CRT cathodes. The device is protected against flashovers. Due to its three cathode current outputs, the TEA5101 can be used with both parallel and sequential sampling applications.

Main features

- Bandwidth: 10 MHz typical.
- Rise and fall time: 50 ns typical.
- CRT cathodes current outputs for parallel or sequential cut-off or gain adjustment.
- Flashover protection.
- Power dissipation: 3.5 W.

RGB HIGH VOLTAGE VIDEO AMPLIFIER

CASE CB-501



PLASTIC PACKAGE

PIN ASSIGNMENT

1	Blue input	9	Red feedback
2	V_{CC} low voltage	10	Green output
3	Green input	11	Green cathode current
4	Red input	12	Green feedback
5	V_{DD} high voltage	13	Blue output
6	Red cathode current	14	Blue cathode current
7	Red output	15	Blue feedback
8	Ground		

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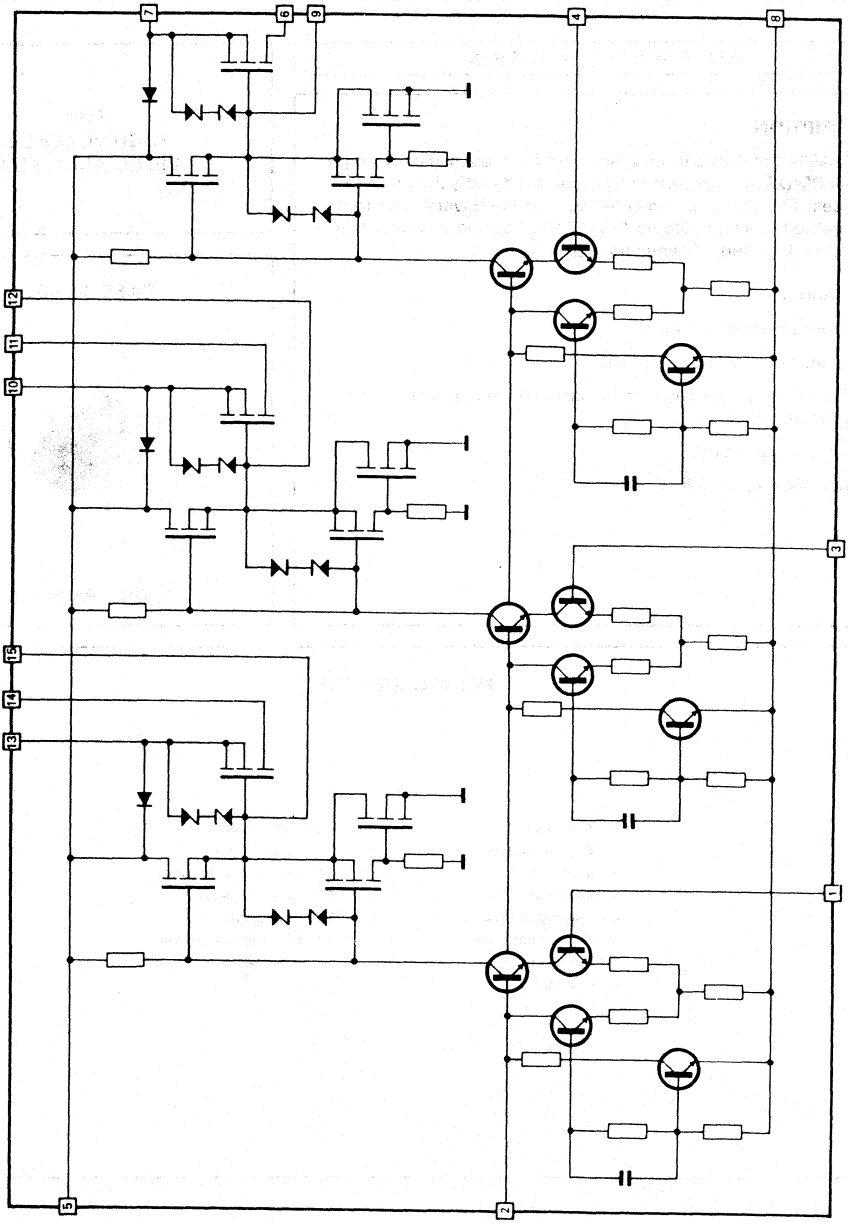
CIRCUIT DESCRIPTION

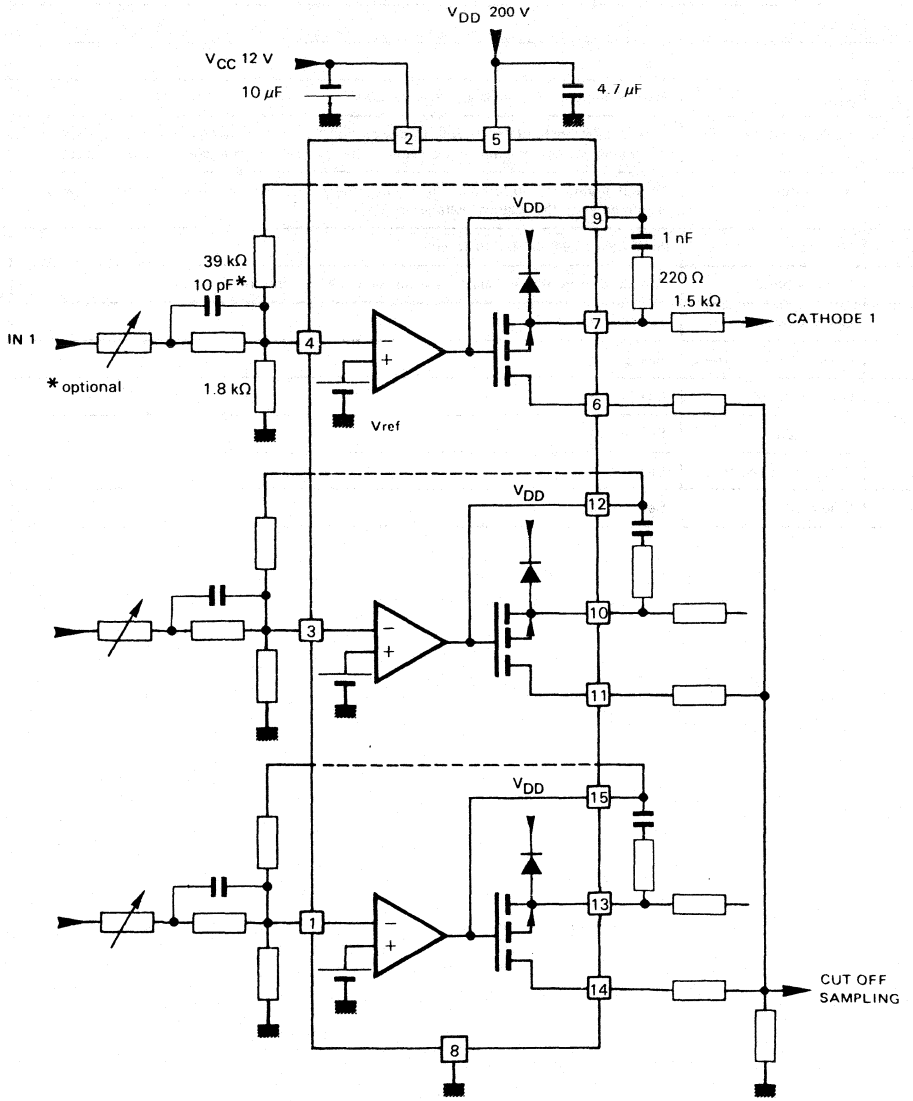
BLOCK DIAGRAM



TYPICAL APPLICATION
(Sequential cut-off sampling)

The TEA5101 consists of three independent amplifiers. Each of them includes:

- a differential amplifier, the gain of which is fixed by external feedback resistors,
- a voltage reference,
- a PMOS transistor providing a copy of the cathode current,
- a protection diode against CRT arc discharges.



PIN DESCRIPTION

No.	Function	Description
1	Blue input	Input of the "blue" amplifier. It is a virtual ground with 3.8 V bias voltage, 15 microamperes input bias current with 14 kohms input resistance.
2	V_{CC}	Low voltage power supply, typically 12 V.
3	Green input	See pin 1.
4	Red input	See pin 1.
5	V_{DD}	High voltage power supply, typically 200 V.
6	Red cathode current	Provides the video processor with a copy of the DC current flowing into the red cathode, for automatic cut-off or gain adjustment. If this control is not used, pin 6 is grounded.
7	Red output	Output driving the red cathode. Pin 7 is internally protected against CRT arc discharges by a diode limiting the output voltage to V_{DD}.
8	Ground	Also connected to the heat sink.
9	Red feedback	Output driving the feedback resistor network for the red amplifier.
10	Green output	See pin 7.
11	Green cathode current	See pin 6.
12	Green feedback	See pin 9.
13	Blue output	See pin 7.
14	Blue cathode current	See pin 6.
15	Blue feedback	See pin 9.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply high voltage	Pin 5	V_{DD}	250	V
Supply low voltage	Pin 2	V_{CC}	35	V
Output current to V_{DD} to ground	Pins 7 - 10 - 13	 I_O I_O	 protected protected	 mA mA
Output current to V_{DD} to ground	Pins 9 - 12 - 15	 I_F I_F	 45 45	 mA mA
Input current	Pins 1 - 3 - 4	I_I	60	mA
Junction temperature		T_j	150	°C
Operating ambient temperature		T_{oper}	0 to 70	°C
Storage temperature		T_{stg}	— 55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Maximum junction-case thermal resistance	$R_{th(j-c)}$	Max. 3	°C/W
Typical junction-ambient thermal resistance	$R_{th(j-a)}$	Typ 35	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 12 V, V_{DD} = 200 V, AV = 50 (unless otherwise specified)

Characteristic		Symbol	Min.	Typ	Max.	Unit
High supply voltage	Pin 5	V_{DD}	—	200	220	V
Low supply voltage	Pin 2	V_{CC}	—	12	—	V
High voltage supply direct current (V_{out} = 100 V)	Pin 5	I_{DD}	—	12	—	mA
Maximum output voltage swing	Pins 7 - 10 - 13	V_{out}	180	—	—	Vpp
Bandwidth (— 3 dB) (C_{load} = 10 pF) ΔV_{out} = 50 Vpp ΔV_{out} = 100 Vpp	Pins 7 - 10 - 13	BW	 — —	 10 8	 — —	 MHz MHz
Rise time and fall time measured between 10% and 90% of output pulse (C_{load} = 10 pF, ΔV_{out} = 100 Vpp)		tr - tf	—	50	—	ns
Open loop gain		G_o	—	50	—	dB
Internal power dissipation (see explanations page 6)		P	—	3.5	—	W
Internal voltage reference	Pins 1 - 3 - 4	V_{ref}	—	3.8	—	V
Input bias current (V_{out} = 100 V)	Pins 1 - 3 - 4	I_{IB}	—	15	—	μA
Input resistance		R_I	—	14	—	kΩ

APPLICATIONS INFORMATIONS

PC BOARD LAYOUT

The best performances of the high voltage video amplifier will be obtained only with a carefully designed PC board. Output to input capacitances are of particular importance.

For a single amplifier, the input-output capacitance, in parallel with the relatively high feedback resistance, creates a pole in the closed-loop transfer function. A low parasitic capacitance (0.3 pF) feedback resistor and HF isolated printed wires are necessary. Furthermore, capacitive coupling from the output of an amplifier toward the input of another one may induce excessive crosstalk.

POWER DISSIPATION

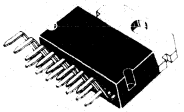
The power dissipation consists of a static part and a dynamic part. The static dissipation varies with the output voltage. With $V_{DD} = 200$ V, $P_{stat} = 2.3$ W at $V_{out} = 100$ V, 1.5 W at 150 V and 3 W at 50 V. First value (2.3 W) will be the reference.

The dynamic dissipation depends on the signal spectrum and the load capacitance. Dynamic power with a UER pattern signal with 150 Vpp modulation is typically 1 W. For a sine wave, dynamic dissipation per amplifier is $Pd = f \times C_L \times V_{opp} \times V_{DD} \times 0.8$. C_L, which includes CRT and board capacitance (about 10 pF) and amplifier output capacitance (7 pF), amounts to 15 to 20 pF. For a 7 MHz 50 Vpp sine wave, and a 20 pF load capacitance, the maximum dynamic power is 3.4 W.

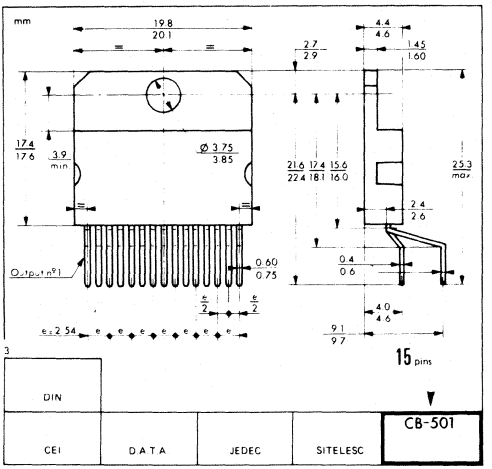
Therefore, the total power dissipation is typically 3.3 W (UER pattern) and 5.7 W at max. sine wave. The junction-case thermal resistance is 3°C/W max. With a 9°C/W external heat sink and a 70°C ambient temperature, the junction temperature will be 110°C typically, and 140°C maximum.

PHYSICAL DIMENSIONS

CB-501



PLASTIC PACKAGE



NOTES

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THOMSON COMPONENTS SEMICONDUCTEURS

TEA5031D

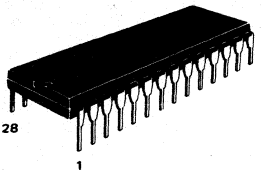
COLOR TV VIDEO PROCESSOR

The TEA5031D is a new video processor I.C. compatible with all standards PAL/SECAM/NTSC and new needs such as teletex, antiope, TV games, remote control etc...

- Matrixing of R, G, B signal from (R-Y) and (B-Y)
- Electronic control of contrast, brightness and saturation.
- Three channels video swtich, for selection of internal signal (broadcast or external R, G, B information.
- Automatic cut-off adjustment.

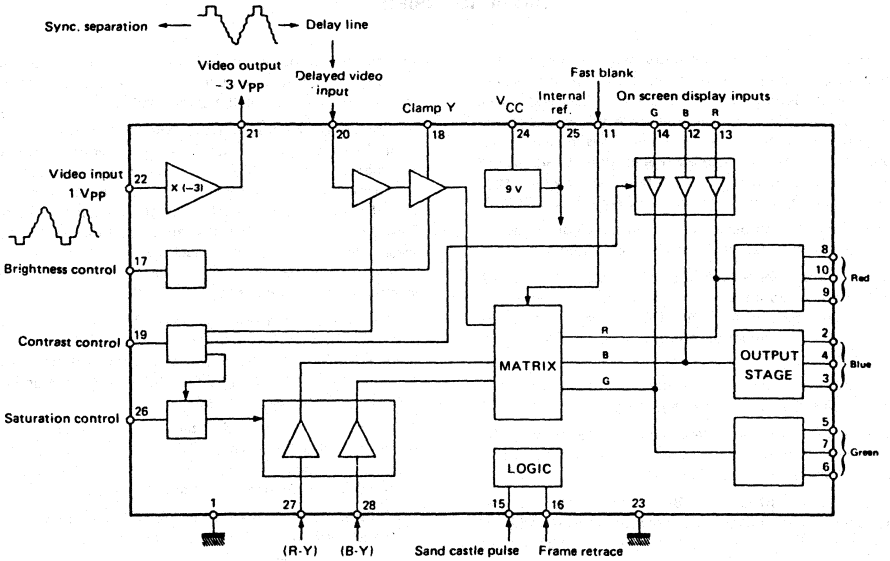
COLOR TV VIDEO PROCESSOR

CASE CB-132



PLASTIC PACKAGE

BLOCK DIAGRAM



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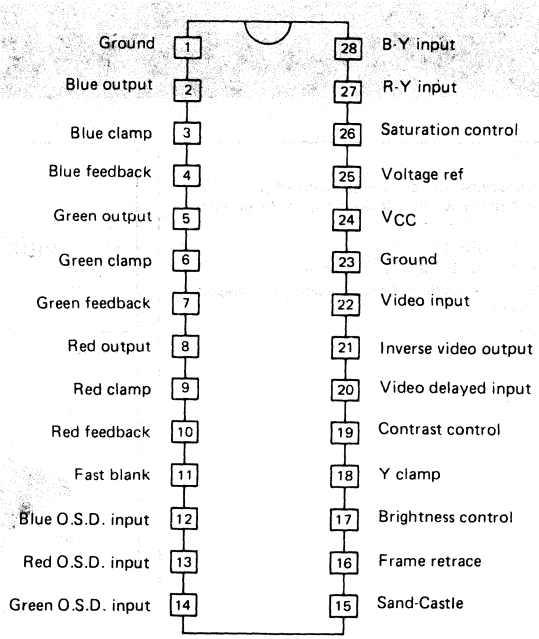
PIN ASSIGNMENT
Top view



CIRCUIT DESCRIPTION

In order to ensure compatibility with standard video transmission systems the luma input is a high impedance, AC coupled, designed to accept a 1 V video signal. After a X3 gain voltage amplifier the inverted luma signal is brought out to the luma delay line. This output is low impedance to match the delay line accurately, and as the signal is inverted, it is highly suitable for driving a synchronization separator such as the TDA2593 or TBA920.

Following the luma delay line the video is controlled by an electronic gain control with a range of 40 dB.

The DC luma level is locked on the black level (cut-off current) with a range of ± 1 V depending of brightness. The DC voltage level is clamped during each line retrace and an external capacitor holds this voltage during the line trace.

After brightness and contrast controls the luminance is fed to the matrix with R-Y and B-Y signals.

The R-Y and B-Y inputs are high impedance with AC coupling, compatible with decoder I'Cs such TEA5630 for SECAM and TEA5620 for PAL.

The voltage gain of R-Y and B-Y is controlled by saturation. The saturation is in tracking with contrast and then the R-Y and B-Y signals are fed to the matrix and summed with on-screen display signals which are controlled in gain by the luma contrast control. Each input is AC coupled and black level clamped using the coupling capacitor as the storage element for the clamp voltage.

All the controls have an active range of 0.5 to 4.5 V making them compatible with D/A converter derived control signals, such as those from remote control systems. The three on-chip output stages are high gain class B amplifiers with the gain set by parallel feedback resistor. This gives a well defined gain and stable output voltage level. The beam current in each cathode of the picture tube is monitored by a high-voltage PNP transistor. A sample of this current is fed back to the IC.

In the luma signal a reference black level is inserted during the line and frame blanking periods. While this reference level is present, and after the frame flyback, the output stage feedback input goes high impedance and an internal comparator is actived.

This circuit compares an internal reference voltage to the voltage developed across an external resistor by the picture tube beam current, and the output voltage is trimmed to get the desired cathode current value.

An internal logic delivers blanking and clampling pulses from the normalized sand castle and frame retrace signals.

MAXIMUM RATINGS

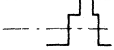
Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	16	V
Operating ambient temperature	T_{amb}	0 to 70	°C
Storage temperature range	T_{stg}	- 65 to + 150	°C

THERMAL CHARACTERISTICS

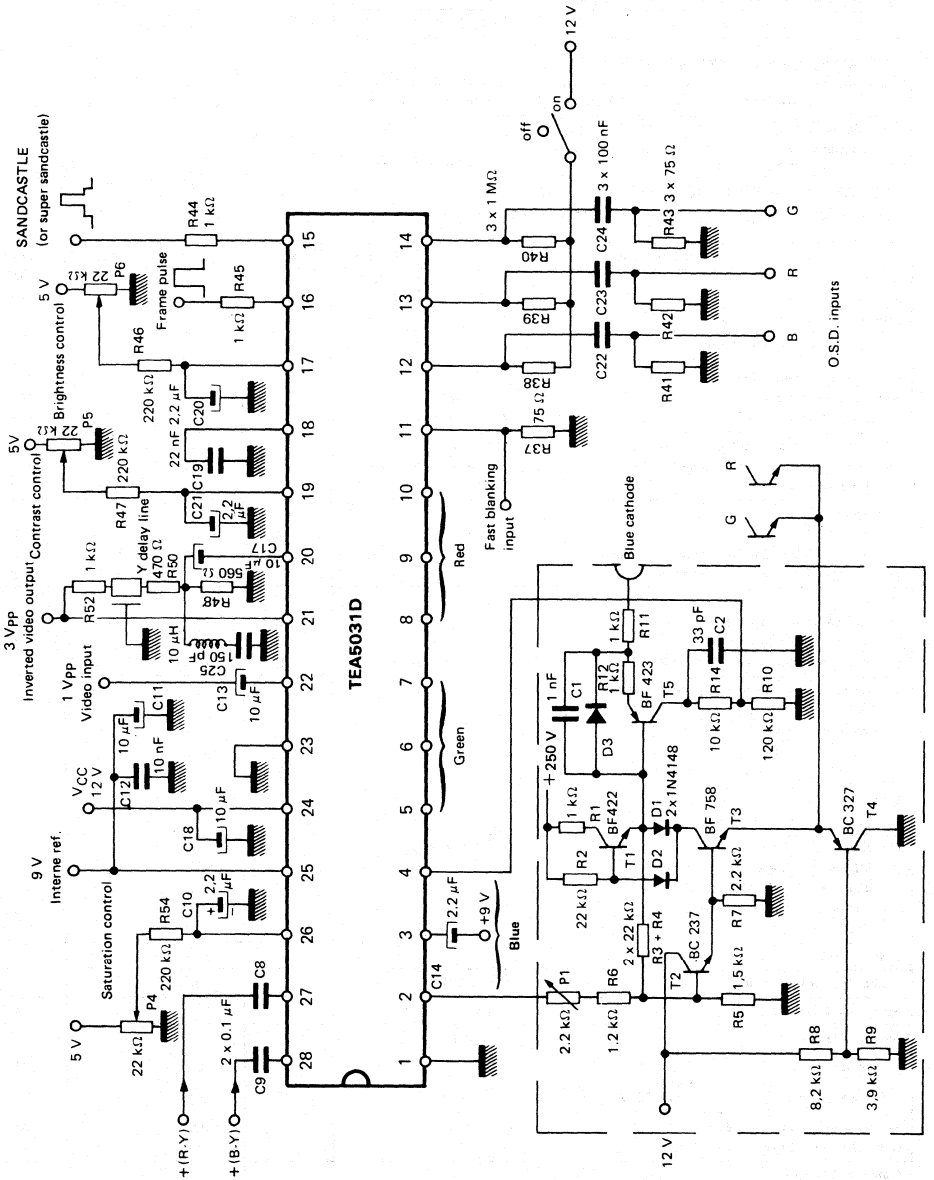
Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	55	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

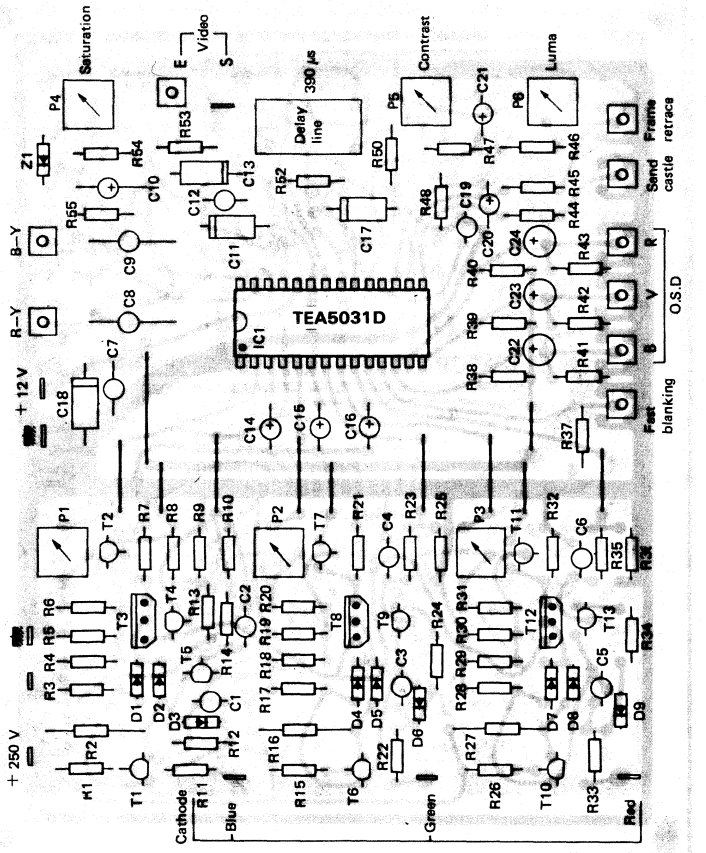
$T_{amb} = + 25°C$; $V_{CC} = 12$ V (unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply voltage	Pin 24	V_{CC}	10.8	12	13.2	V
Supply current	Pin 24	I_{CC}	–	55	–	mA
Internal voltage ref.	Pin 25	V_Z	–	9	–	V
Input-Output characteristics						
Video input	Pin 22	–	–	1	–	Vpp
Output voltage inv. video (V22 = 1 Vpp)	Pin 21	–	–	3	–	Vpp
Max output voltage swing	Pin 21	–	–	7	–	Vpp
– 3 dB bandwidth	Pins 2-5-8	–	4.5	5	–	MHz
(R–Y) input voltage (100 % modulation)	Pin 27	–	–	1.4	2	Vpp
(B–Y) input voltage (100 % modulation)	Pin 28	–	–	1.0	2	Vpp
– 3 dB bandwidth		–	1.5	–	–	MHz
Luma gain						
G21/22	Pin 21	–	8.5	10	11.5	dB
G2/20 ; G5/20 ; G8/20 at max adjustement	Pins 2-5-8	–	13.5	15.5	19.1	dB
Differential gain fault : Luma channel		–	–	–	0.5	dB
Chroma gain						
G8/27 at max adjustment		–	8.8	11.6	14.5	dB
G2/28 at max adjustment		–	12	14.7	17.2	dB
Chroma gain ratio at max adjustment		–	1.28	1.40	1.48	
Voltage control for electronic potentiometers						
Contrast (Pin 19) - Saturation (Pin 26)						
Range of adjustment						
V19 = 5 V ; V26 = 5 V		–	–	G_{max}	–	dB
V19 = 0 V ; V26 = 0 V Attenuation		–	40	46	–	dB
Brightness (Pin 17)						
V_{out} adjustment (V17 varying from 0 to 5 V)		–	–	± 1	–	V
On screen display inputs	Pins 12-13-14					
OSD input voltage (Black to white level)		–	–	1	2	V
OSD gain (V2/12 ; V8/13 ; V5/14)		–	13.5	15	17	dB
OSD generator max impedance		–	–	–	75	Ω
- 3 dB bandwidth		–	5	–	–	MHz
Fast blanking threshold		–	–	0.5	–	V
Max output voltage swing	Pins 2-5-8	–	7	8	–	Vpp
Feed-back threshold	Pins 4-7-10	–	1.7	2	2.4	V
Sand-Castle input	Pin 15					
Clamp Y 8 V			–	8	–	V
Line blanking  2.5 V			–	2.5	–	V
Frame return input voltage	Pin 16	–	–	2.5	–	V
Control current (V15 = V16 = 4 V)			–	0.5	–	mA
Matrix coefficient						
Red output (V5/V8 with V27 = 1 V ; V28 = 0 ; V20 = 0)		–	–	0.51	–	–
Blue output (V5/V2 with V27 = 0 ; V28 = 1 ; V20 = 0)		–	–	0.19	–	–

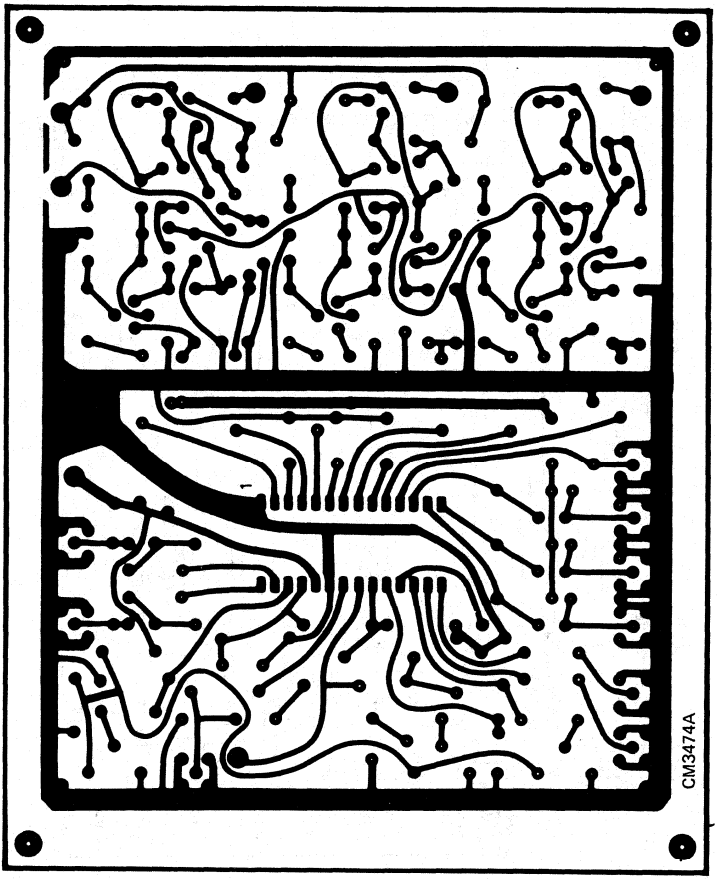
APPLICATION CIRCUIT



COMPONENT SIDE



COPPER SIDE



N°	Value	P
R1	1 kΩ	1/4 W
R2	22 kΩ	1 W
R3	22 kΩ	1/4 W
R4	22 kΩ	"
R5	1.5 kΩ	"
R6	1.2 kΩ	"
R7	2.2 kΩ	"
R8	8.2 kΩ	"
R9	3.9 kΩ	"
R10	120 kΩ	"
R11	1 kΩ	"
R12	1 kΩ	"
R13	220 kΩ	"
R14	10 kΩ	"
R15	1 kΩ	"
R16	22 kΩ	1 W
R17	22 kΩ	1/4 W
R18	22 kΩ	"
R19	1.5 kΩ	"
R20	1.2 kΩ	"
R21	2.2 kΩ	"
R22	1 kΩ	"
R23	10 kΩ	"
R24	1 kΩ	"
R25	120 kΩ	1/4 W
R26	1 kΩ	"
R27	22 kΩ	1 W

N°	Value	P
R28	22 kΩ	1/4 W
R29	22 kΩ	"
R30	1.5 kΩ	"
R31	1.2 kΩ	"
R32	2.2 kΩ	"
R33	1 kΩ	"
R34	1 kΩ	"
R35	10 kΩ	"
R36	120 kΩ	"
R37	75 Ω	"
R38	1 MΩ	"
R39	1 MΩ	"
R40	1 MΩ	"
R41	75 Ω	"
R42	75 Ω	"
R43	75 Ω	"
R44	1 kΩ	"
R45	1 kΩ	"
R46	220 kΩ	"
R47	220 kΩ	"
R48	560 Ω	"
R50	470 Ω	1/4 W
R52	1 kΩ	"
R53	1 kΩ	"
R54	220 kΩ	"
R55	1 kΩ	"

N°	Value	U
C1	1 nF	
C2	33 pF	
C3	1 nF	
C4	33 pF	
C5	1 nF	
C6	33 pF	
C7	10 nF	63 V
C8	100 nF	63 V
C9	100 nF	63 V
C10	2.2 µF	35 V
C11	10 µF	63 V
C12	10 nF	63 V
C13	10 µF	63 V
C14	2.2 µF	35 V
C15	2.2 µF	35 V
C16	2.2 µF	35 V
C17	10 µF	63 V
C18	10 µF	63 V
C19	22 nF	
C20	2.2 µF	35 V
C21	2.2 µF	35 V
C22	4.7 µF	63 V
C23	4.7 µF	63 V
C24	4.7 µF	63 V
C25	150 pF	

N°	Typ
T1	BF 422
T2	BC 237
T3	BF 758
T4	BC 327
T5	BF 423
T6	BF 422
T7	BC 237
T8	BF 758
T9	BF 423
T10	BF 422
T11	BC 237
T12	BF 758
T13	BF 423

N°	Typ
IC1	TEA5031D

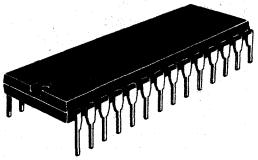
N°	Value
P1	2.2 kΩ
P2	2.2 kΩ
P3	2.2 kΩ
P4	22 kΩ
P5	22 kΩ
P6	22 kΩ

N°	Typ
DL	TDK

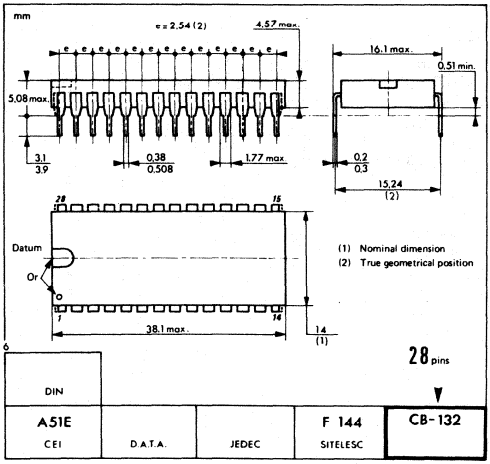
N°	Typ
D1	1N4148
D2	"
D3	"
D4	"
D5	"
D6	"
D7	"
D8	"
D9	"
Z1	5 V

PHYSICAL DIMENSIONS

CB-132



PLASTIC PACKAGE



These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

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THOMSON COMPONENTS SEMICONDUCTEURS

TEA5040

WIDE BAND VIDEO PROCESSOR

PRODUCT PREVIEW

The TEA5040 IC is a serial bus controlled videoprocessing device which integrates a complex architecture fulfilling multiple functions.

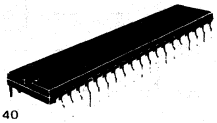
Main features

- Digital control of brightness, saturation and contrast on TV' signals and R, G, B internal or external sources.
- Bus drive of switching functions.
- Dematrixing of R, G, B signals from Y, R-Y, B-Y TV mode inputs.
- Matrixing of R, G, B sources into Y, R-Y, B-Y signals.
- Automatic drive and cut-off controls by digital processing during the frame retrace.
- Peak and average beam current limitation.
- On-chip switching for R, G, B input selection.
- On-chip insertion of internal or external R, G, B sources.

WIDE BAND

VIDEO PROCESSOR

CASE CB-132



PLASTIC PACKAGE

PIN ASSIGNMENT

V_{CC}	1	40	Switchable video output
R int input	2	39	Synchro input
R ext input	3	38	Internal video output
G int input	4	37	Internal video input
G ext input	5	36	Average beam limit. ref.
B int input	6	35	External video input
B ext input	7	34	Average beam current filter
On Screen Display ext	8	33	Leakage currents filter
On Screen Display int	9	32	Cathode currents input
B-Y input	10	31	Switch cut-off resistance
R-Y input	11	30	Super Sand Castle input
Y input	12	29	B output
Clock	13	28	Cut-off memory (B channel)
Data	14	27	Drive memory (B channel)
Enable	15	26	G output
Voltage reference	16	25	Cut-off memory (G channel)
R clamp memory	17	24	Drive memory (G channel)
G clamp memory	18	23	R output
B clamp memory	19	22	Cut-off memory (R channel)
Ground	20	21	Drive memory (R channel)

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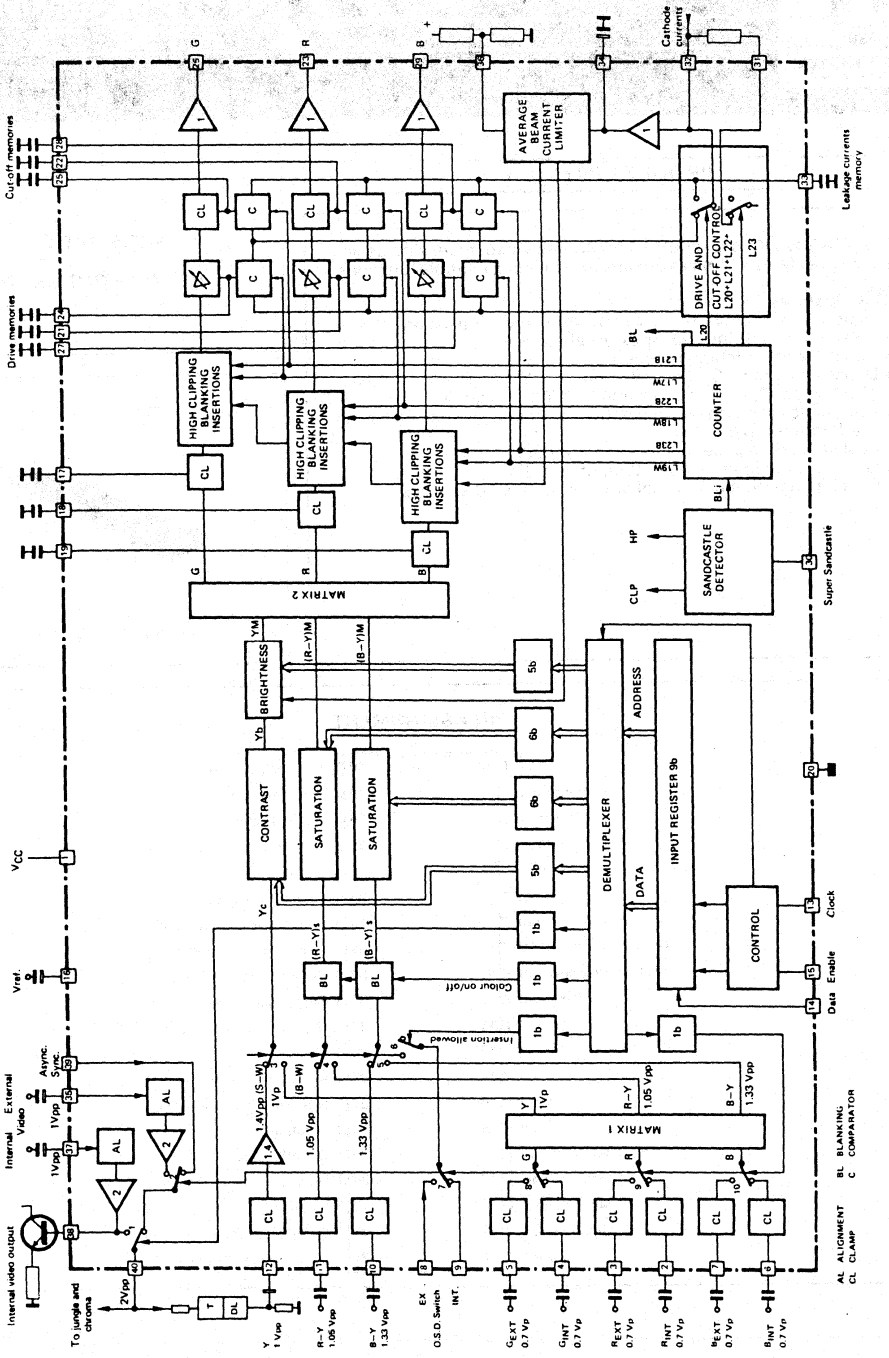
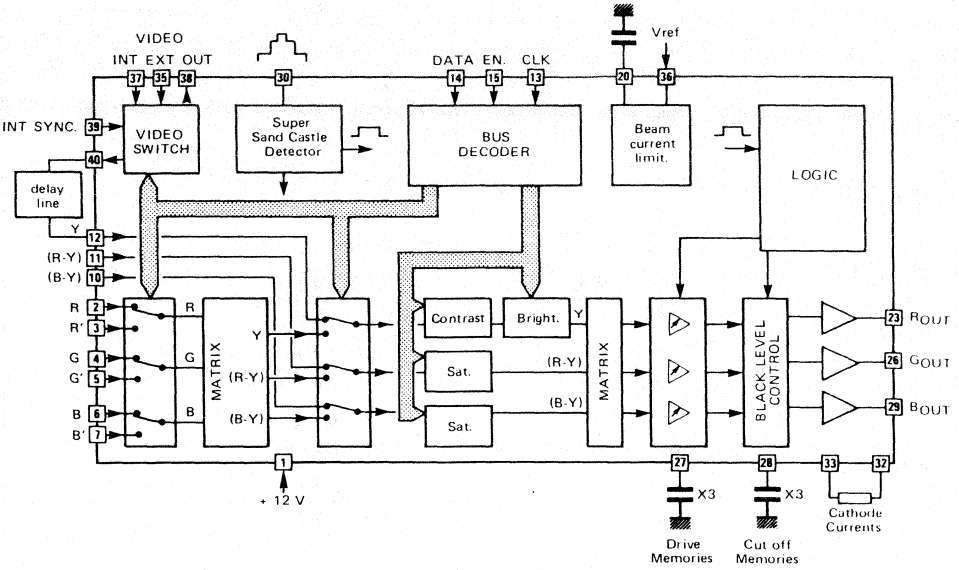
BLOCK DIAGRAM





GENERAL DESCRIPTION

Brief description

This new integrated circuit incorporates the following features:

- a synchro and two video inputs
- a fixed video output
- a switchable video output
- normal Y, R-Y, B-Y TV mode inputs
- double set of R, G, B, inputs
- brightness, contrast and saturation controls as well on a R, G, B picture as on a normal TV picture
- digital control inputs by means of serial bus
- peak beam current limitation
- average beam current limitation
- automatic drive and cut-off controls

Block diagram description

Bus decoder

A 3 lines bus (clock, data, enable) delivered by the microcomputer of the TV-set enters the videoprocessor integrated circuit (pins 13-14-15). A control system acts in such a way that only a 9 bit word is taken into account by the videoprocessor. Six of the bits carry the data, the remaining three carry the address of the subsystem.

Function	Address	Number of bits
Brightness control	0	5
Contrast control	1	5
Colour on/off selection	2	1
Insertion allowed	3	1
Int/Ext RGB switching	4	1
Int/Ext video switching	5	1
B-Y saturation control	6	6
R-Y saturation control	7	6

Hereunder are mentioned the different 9 bit words it is necessary to send to each subsystem in order to make it fulfil all its functions.

Subsystem's configuration		Data bits Lsb ------ Msb	Add. bits Lsb ----- Msb
BRIGHTNESS	MIN.	X 0 0 0 0 0	0 0 0
	MAX.	X 1 1 1 1 1	
CONTRAST	MIN.	X 0 0 0 0 0	1 0 0
	MAX.	X 1 1 1 1 1	
COLOUR ON/OFF	OFF	X X X X X 0	0 1 0
	ON	X X X X X 1	
INSERTION	ALLOWED	X X X X X 0	1 1 0
	NOT ALLOWED	X X X X X 1	
RGB INT/EXT	INT.	X X X X X 0	0 0 1
	EXT.	X X X X X 1	
SYNC/ASYNC MODE	SYNC.	X X X X 0 X	0 0 1
	ASYNC.	X X X X 1 X	
VIDEO INT/EXT	INT.	X X X X X 0	1 0 1
	EXT.	X X X X X 1	
SATURATION B-Y	MIN.	0 0 0 0 0 0	0 1 1
	MAX.	1 1 1 1 1 1	
SATURATION R-Y	MIN.	0 0 0 0 0 0	1 1 1
	MAX.	1 1 1 1 1 1	

A demultiplexer directs the data towards latches which drive the appropriate control. More detailed informations about serial bus functioning are given in the following chapter.

Video switch

The video switch has three inputs:

- an internal video input (pin 37),
- an external video input (pin 35),
- a synchro input (pin 39),

and two outputs:

- an external video output (pin 38),
- a switchable video output (pin 40).

The 1 Vpp composite video signal applied on the internal video input is multiplied by two and then appears as a 2 Vpp low impedance composite video output. This signal is used to deliver a 1 Vpp/75 Ohm composite video signal to the peri-TV plug.

The switchable video output can be any of the three inputs. When the Int/Ext one bit word is high (address number 5), the internal video input is selected. If not, either a regenerated synchro pulse or the external video signal is directed towards this output depending on the level of the Int/Ext RGB one bit word (address number 4). As this output is to be connected to the jungle integrated circuit, RGB information derived from an external source via the TV plug can be displayed on the screen, the synchronisation of the TV-set being then made with an external video signal.

When RGB information is derived from a source integrated in the TV-set, a teletext decoder for example, the synchronization can be made either on the internal video input (in case of synchronous data) or on the synchro input (in case of asynchronous data).

R, G, B inputs

There are two sets of R, G, B inputs: one is to be connected to the peri-TV plug (Ext R, G, B), the second one receives the information derived from the TV-set itself (Int R, G, B).

In order to have a saturation control on a picture coming from the R, G, B inputs too, it is necessary to get R-Y, B-Y and Y signals from R, G, B informations : this is performed on the first matrix that receives the three 0.9 Vp (100% white) R, G, B signals and delivers the corresponding Y, R-Y, B-Y signals. These ones are multiplied by 1.4 in order to make the R-Y and B-Y signals compatible with the R-Y and B-Y TV mode inputs. The desired R, G, B inputs are selected by means of 3 switches controlled by the Int/Ext RGB one bit word (address number 4). The three selected inputs are clamped in order to give the required DC level at the output of this first matrix. The three not selected inputs are clamped on a fixed DC level.

Y, R-Y, B-Y inputs

The 2 Vpp composite video signal appearing at the switchable output of the video switch (pin 40) is driven through the subcarrier trap and the luminance delay line with a 6 dB attenuation to the Y input (1 Vpp; pin 12). In order to make this 1 Vpp (synchro to white) Y signal compatible with the 1 Vpp (black to white) Y signal delivered by the first matrix, it is necessary to multiply it by a 1.4 coefficient.

R, G, B insertion

A R, G, B source has also to provide an insertion pulse. Since this integrated circuit is able to be directly connected to two different sources, it is necessary then to have two separated insertion pulse inputs. These two inputs (pins 8-9) are selected exactly in the same way as the internal or external R, G, B inputs by the corresponding one bit control. Furthermore, the insertion will be only valid for the appropriate level of the only TV/allowed insertion one bit word (address number 3); in this case, three switches will select the Y, R-Y, B-Y signals coming from the first matrix instead of the ones coming from the direct inputs during the insertion pulse time.

Controls

The three brightness, contrast and saturation control functions are directly made in a digital way without using digital to analog converters.

The contrast control of the Y chanel is obtained by means of a digital potentiometer which is an attenuator including several switchable cells directly controlled by a 5 bit word (address number 1). The brightness control is also made by a digital potentiometer (5 bit word, address number 0). Since a + 3 dB contrast possibility is required, the Y signal output 0.7 Vpp nominal. For both functions, the control characteristics are quasi-linear.

In each R-Y and B-Y channel, a six cell digital attenuator is directly controlled by a 6 bit word (address number 6 and 7). The tracking which is necessary to keep the saturation constant when changing the contrast has to be done externally by the microcomputer. Furthermore, the colour can be completely cancelled, blanking the R-Y and B-Y signals by means of a switch controlled by the colour on/off one bit word (address number 2).

Second matrix, clamp, peak clippings, blanking

The second matrix receives the Y, R-Y and B-Y signals and delivers the corresponding R, G, B signals. As it is required to have the possibility of a + 6 dB saturation, an internal gain of 2 is applied on both R-Y and B-Y signals.

A low clipping level is included in order to ensure a correct blanking during the line and frame retraces. A high clipping level ensures the peak beam current limitation. These limitations are correct only if the DC bias of the three R, G, B signals are precised enough. Therefore, a clamp is necessary in each channel because this bias is not kept with enough accuracy in the matrix.

Sandcastle detector and counter

The three level supersandcastle is used in the integrated circuit to deliver the burst pulse (CLP), the horizontal pulse (HP), and the composite vertical and horizontal blanking pulse (BLI). This last one is regenerated in the counter which delivers a new composite pulse (BL) in which the vertical part lasts 23 lines since the vertical part of the supersandcastle lasts more than 11 lines.

The TEA5040 cannot work properly if this minimum duration of 11 lines is not ensured.

The counter delivers different pulses needed in the integrated circuit and especially the line pulses 17 to 23 used in the automatic drive and cut-off control system.

Automatic drive and cut-off control system

Cut-off and drive adjustments are no longer necessary with this integrated circuit as it has a sample and hold feedback loop incorporating the final stages of the TV-set. This system works in a sequential mode. For this purpose, special pulses are inserted in G, R and B channels. During the lines 17, 18 and 19, a "drive pulse" is inserted respectively in the green, red and blue channels. The line 20 is blanked on the three channels. During the lines 21, 22 and 23, a "quasi cut-off pulse" is inserted respectively in the green, red and blue guns.

The resulting signal is then applied to the input of a voltage controlled amplifier. In the final stages of the TV-set, the current flowing in each green, red and blue cathode is measured and sent to the videoprocessor with a current source.

The three currents are added together in a matrix comprised of resistors. By means of this matrix, it is possible to program the ratio between the three currents in order to get the appropriate colour temperature. The output of the matrix forms a high impedance voltage source which is connected to the integrated circuit (pin 32), a lower impedance is grounded by the IC on this pin during the drive pulses (lines 17, 18, 19) to keep the measured voltages in the same range.

This is due to the fact that the drive currents are about one hundred times as high as the cut-off and leakage ones.

Each voltage appearing sequentially on the wire pin 32 is then a function of specific cathode current:

- When a current due to a drive pulse occurs, the voltage appearing on the pin 32 is compared within the IC with an internal reference, and the result of the comparison charges or discharges an external appropriate drive capacitor which memories the value during the frame. This voltage is applied to a voltage controlled amplifier and the system works in such a way that the pulse current drive derived from the cathode is kept constant.
- During the line 20, the three guns of the picture tube are blanked. The leakage current flowing out of the final stages is transformed into a voltage which is stored by an external leakage capacitor to be used later as a reference for the cut-off current measurement.
- When a current due to a cut-off pulse occurs, the voltage appearing on the pin 32 is compared within the IC to the voltage present on the leakage memory. An appropriate external capacitor is then charged or discharged in such a way that the difference between each measured current and the leakage current is kept constant, that means the quasi cut-off current is kept constant.

Average beam current limitation

The total current of the three guns is integrated by means of an internal resistor and an external capacitor (pin 34) and then compared with a programmable voltage reference (pin 36). When 70% of the maximum permitted beam current is reached, the drive gain begins to be reduced; for that purpose, the amplitude of the inserted pulse is increased.

In order to keep enough contrast, the maximum drive reduction is 6 dB limited. If it is not sufficient, the brightness is suppressed.

SPECIFICATION for the THOMSON BIDIRECTIONAL DATA BUS

The bidirectional data bus has three lines (ENABLE, CLOCK, DATA) and is working in series. Transmission on the DATA line is effected bidirectionally. The ENABLE and CLOCK lines are only driven by the microcomputer.

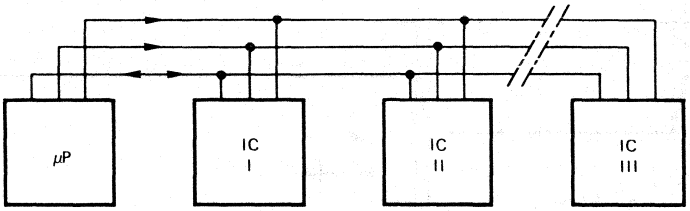


Figure 1 - Peripherals connections on bus

It is possible to select several IC's from the microprocessor via the bus. The identification of each particular IC is achieved by the length of the word (number of data bits/clock impulses), meaning that each IC is responding with its own particular word length.

The number is determined while ENABLE is low and by counting the negative clock edges. As soon as the high edge of the ENABLE signal is applied, the number is fixed (see Figure 2).

The reply word lenght from any of the IC's on the bi-directional line is four bits. If it is found insufficient then the reply word can be expanded to include two repetitive reply sequences one after the other.

The bi-directional transmission is present:

- If the IC has been previously addressed then at the positive going edge of the enable pulse, the bi-directional function is enabled.
- If ENABLE remains high.
- And DATA is available only during the period when the clock remains low.

number of identification bits: n
number of bi-directional clocks: 4

1. . . n: data from the microcomputer
1. . . M: data to the microcomputer

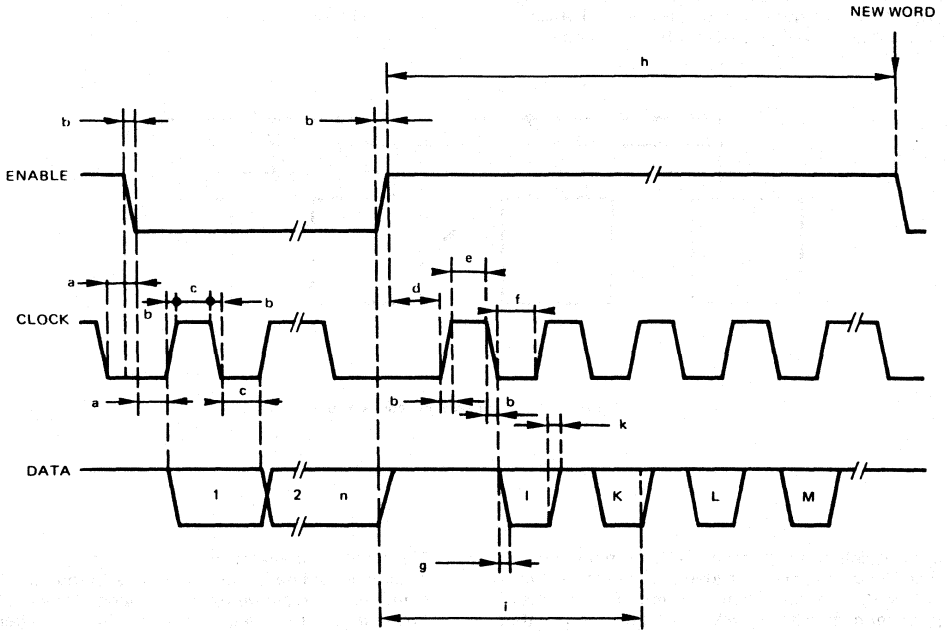


Figure 2

The four bit reply word (synchronized with the clock coming from the microcomputer) from the addressed IC to the microcomputer is sent only once. Subsequent clock pulses present on the clock line will be ignored by the IC in question. The data sent to the microcomputer can generally be suppressed completely or partially, but in the case of the videoprocessor it is necessary to maintain a minimum reply word lenght of 1 (see Figure 3).

This implies that a bi-directional bus that incorporates other IC's together with a videoprocessor IC is then also limited by the minimum reply word restriction of 1.

The data word from the microcomputer is divided into:
- addresses within the IC,
- data.

The data word to the microcomputer is divided into:
- two data bits,
- two address bits.

After the operating voltage is applied, the first transmission will be used as a reset command, that means that the data word will not be detected.

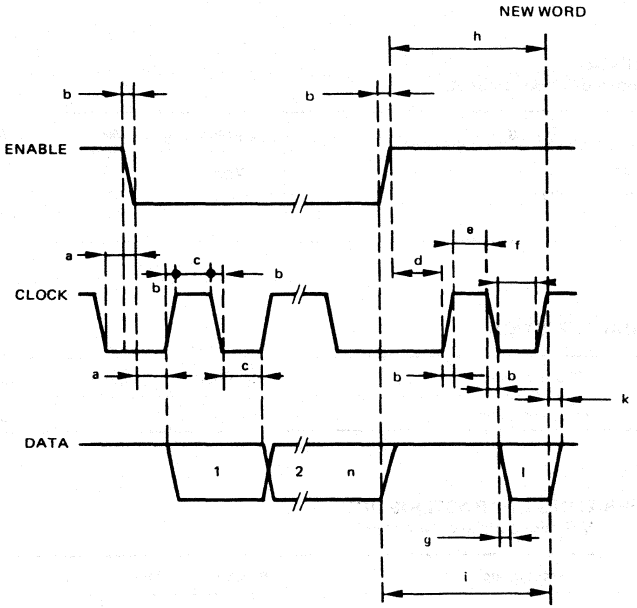


Figure 3

number of identification bits: n
number of bi-directional clocks: 1 (which is the minimum number for the videoprocessor)

1. . . n: data from the microcomputer
1: data to the microcomputer

BIDIRECTIONAL DATA BUS

Characteristic	Symbol	Min	Typ	Max	Unit
TIMING Identification nr = 9 (9: video processor address) (see Figures 2-3)					
	a	5	—	—	µs
	b	0	—	—	µs
	c	5	—	—	µs
	d	70	—	—	µs
	e	—	—	—	—
	f	—	—	—	—
	g	—	—	—	—
(new word to same IC)	h	24	—	—	ms
(new word to other IC)	h	70	—	—	µs
	i	—	—	—	—

MAXIMUM RATINGS

T_{amb} = 25°C (Unless otherwise noted)

Rating	Symbol	Min	Max	Unit
Supply voltage pin 1	V_{CC}	14	—	V
Operating temperature range	T_{oper}	0	+ 60	°C
Storage temperature range	T_{stg}	— 25	+ 125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Junction - ambiant thermal resistance	R_{th} (j-a)	—	55	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} 25°C, V_{cc} = 12 V (Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage pin 1	V_{CC}	10.8	12	12.5	V
Supply current pin 1	I_{CC}	—	80	104	mA
Video switch External video input (75 Ω source impedance)					
Signal amplitude pin 35	V_{35}	—	1	1.4	Vpp
Input current pin 35	I_{35}	—	10	30	µA

ELECTRICAL OPERATING CHARACTERISTICS(Cont'd)

Characteristic	Symbol	Min	Typ	Max	Unit
Internal video input (300 Ω source impedance)					
Signal amplitude pin 37	V_{37}	—	1	1.4	Vpp
Input current pin 37	I_{37}	—	10	30	μA
Synchro input					
Output signal amplitude pin 39 (for a 0.5 V to 2.5 V input signal on pin 39)		0.5	0.6	—	V
Internal video output pin 38					
dynamic		2.7	—	—	Vpp
DC Level (bottom of synchro pulse)		1	—	2.0	V
Gain between pin 38 and pin 37 (for 1 Vpp on pin 37)		5	6	7	dB
Crosstalk between pin 35 and pin 38		—	—	− 50	dB
Bandwidth (— 1 dB)		6	—	—	MHz
Switchable video output pin 40					
Dynamic (pin 35 or pin 37 selected)		2.7	—	—	Vpp
Gain between pins 35-40 (for 1 Vpp on pin 35)		5	—	7	dB
Gain between pins 37-40 (for 1 Vpp on pin 37)		5	—	7	dB
Crosstalk between pins 35-40		—	—	− 50	dB
Crosstalk between pins 37-40		—	—	− 50	dB
Bandwidth (— 1 dB)		6	—	—	MHz
TV mode inputs					
Luminance input pin 12					
Signal amplitude (100% white)	Y	—	1	1.5	Vpp
DC level (on black level)	V_{12}	—	4	—	V
Input current	I_{12}	—	—	10	μA
R-Y input pin 11					
Signal amplitude (75% saturation)	R-Y	—	1.05	1.47	Vpp
DC level (on black level)	V_{11}	—	4.7	—	V
Input current	I_{11}	—	—	2	μA
B-Y input pin 10					
Signal amplitude (75% saturation)	B-Y	—	1.33	1.86	Vpp
DC level (on black level)	V_{10}	—	4.7	—	V
Input current	I_{10}	—	—	2	μA
RGB inputs pins 2-3-4-5-6-7					
Signal amplitude (100% saturation without synchro pulse)		—	0.9	1.2	Vpp
DC level (on black level)		—	3.2	—	V
Input current		—	—	3	μA
On screen display control inputs pins 8-9					
TV/RGB mode threshold		0.5	—	0.9	V
Switching time		—	70	—	ns
Switching time delay		—	70	—	ns
Clamp memory output pins 17-18-19					
Voltage range		8	10	11	V
Input current		—	—	2	μA

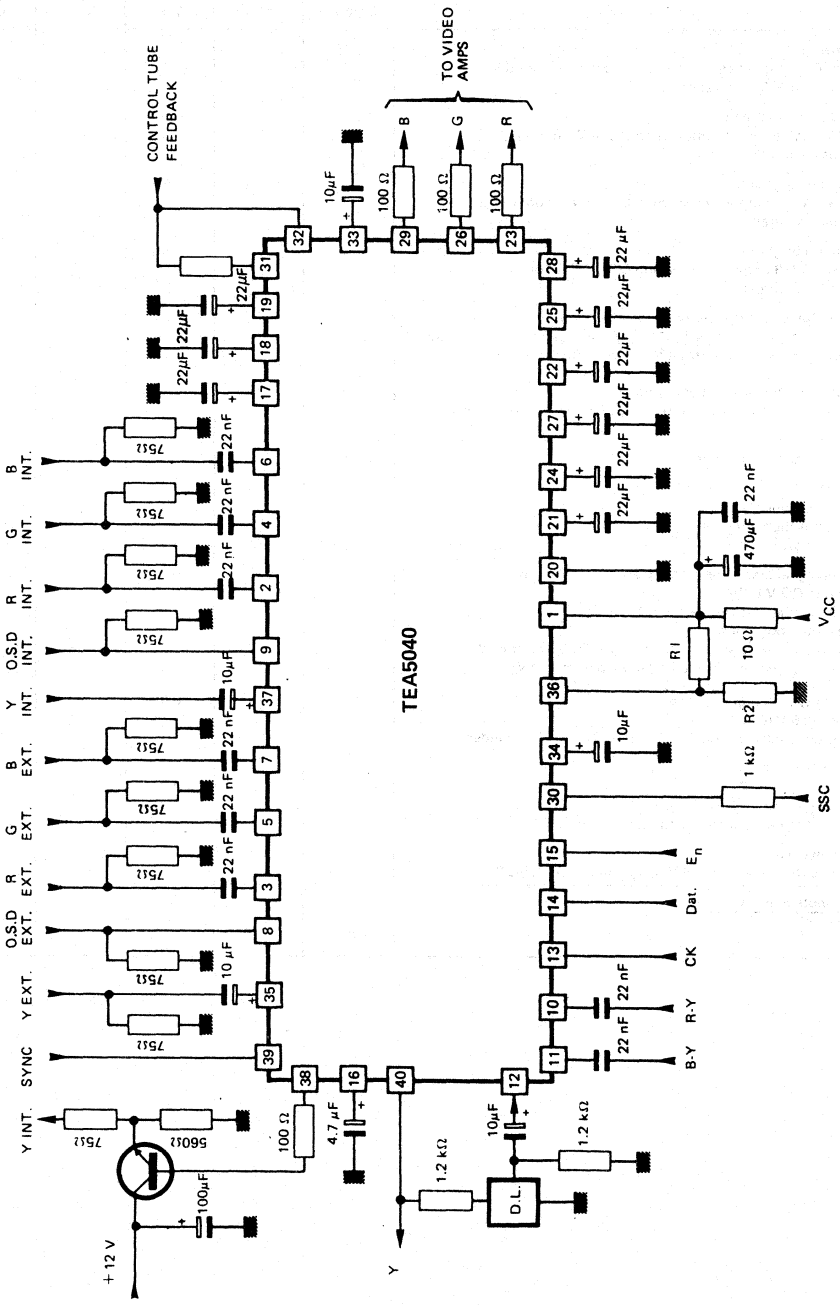
ELECTRICAL OPERATING CHARACTERISTICS (Cont'd)

Characteristic	Symbol	Min	Typ	Max	Unit
Reference voltage pin 16	V_{ref}	—	4	—	V
Sandcastle input pin 30					
Blanking threshold		1	1.4	1.8	V
Burst gate threshold		6.4	6.9	7.6	V
Line retrace threshold		3.1	3.4	3.8	V
Input current pin 30 grounded		—	—	100	μA
Drive and cut-off memory output pins 21-22-24-25-27-28					
Drive leakage current pins 21-24-27		—	—	1	μA
Cut-off leakage current pins 22-25-28		—	—	1	μA
Minimum active level pins 22-25-28		—	4	—	V
Leakage current memory output pin 33					
Voltage range		3	—	—	V
Input current (during picture pin 33 = 5 V)		—	—	0.5	μA
Charging output impedance		—	—	500	Ω
Minimum voltage (pin 32 grounded)		—	3	—	V
Cathode currents input pin 32					
output current during the line trace (pin 32 grounded)		—	—	10	μA
Voltage during lines 17, 18, 19		—	0.4	—	V
Voltage difference during lines 21, 22, 23 and during line 20		—	0.4	—	V
Voltage amplitude on cathode currents input for drive decrease threshold 10% on drive/cut-off					
1 V on pin 36	V_{32}	—	0.7	—	V
2 V on pin 36	V_{32}	—	1.4	—	V
Voltage amplitude on cathode currents input for brightness decrease threshold					
1 V on pin 36	V_{32}	—	1	—	V
2 V on pin 36	V_{32}	—	2	—	V
Impedance SWITCH pin 31					
saturation impedance (for 5 mA) (open during lines 20, 21, 22, 23)		—	250	—	Ω
Reference voltage input for the average beam current limiter pin 36					
reference voltage	V_{36}	0	—	5	V
Input current (V_{36} = 1 V)	I_{36}	—	—	— 20	μA
Average beam current FILTER pin 34 voltage range $0 < V_{32} \leq 7$ V		6	—	—	V
RGB outputs R (pin 23), G (pin 26), B (pin 29)					
Inserted levels					
Low clipping level referred to quasi cut-off inserted level (100% = B/W output signal at maximum contrast with 0.5 V (B/W) input Y signal)		—	45	—	%
High clipping level referred to quasi cut-off inserted level (100% = B/W output signal at maximum contrast with 0.5 V (B/W) input Y signal)		—	115	—	%
Drive inserted level referred to quasi cut-off inserted level (without beam limitation, V_{36} = 6 V, V_{32} grounded)		—	35	—	%
Bandwidth (— 3 dB) (TV mode and R, G, B mode)		—	10	—	MHz
Crosstalk for any of the 11 inputs pins 2-3-4-5-6-7-10-11-12-35-37 on any of the 5 outputs pins 23-26-29-38-40 (range: DC to 3 MHz)		—	—	— 50	dB

ELECTRICAL OPERATING CHARACTERISTICS (Cont'd)

Characteristic	Symbol	Min	Typ	Max	Unit
Brightness Nominal brightness referred to quasi cut-off inserted level (bit word » 10000, address = 0)		—	− 25	—	%
Total brightness range (100% = W/B output signal when 0.5 V (W/B) on pin 12 and max. contrast)		—	78	—	%
Maximum brightness (100% = W/B output signal when 0.5 V (W/B) on pin 12 and max. contrast)		—	38	—	%
Minimum brightness (100% = W/B output signal when 0.5 V (W/B) on pin 12 and max. contrast)		—	− 40	—	%
Differential brightness between any two channels (TV mode, colour off, pins 10-11-12 AC grounded, 0.5 (W/B) signal on pin 12, maximum contrast = 100% on RGB outputs)		—	—	2	%
Variation of the differential brightness (in the whole saturation control range (including colour off))		—	—	0.5	%
Contrast max. contrast attenuation		11	—	—	dB
Saturation max. saturation max. saturation attenuation colour off attenuation		— 20 40	6 — —	— — —	dB dB dB
Output signal amplitude pins 23-26-29 (blanking to high clipping) • Y input: 0.7 V B/W • 0 dB contrast, bit word = 010110, address = 1 • Maximum brightness • Maximum drive efficiency (pins 21-24-26-27 grounded) • No average beam current limitation (pin 36 to 6 V)		—	6.2	—	V
Black to white output voltage Y input: 0.5 V (B/W) Maximum contrast (pin 36 to 6 V, pins 21-24-27 grounded)		—	3.6	—	V
Drive efficiency ratio: $\frac{V_{OUT} \text{ (pins 21-24-27 grounded)}}{V_{OUT} \text{ (pins 21-24-27 to } V_{CC})}$ (No average beam current limitation pin 36 to 6 V)		—	3.4	—	V
Black level control (variable DC voltage from 4 V to V_{CC} on pins 22-25-28)		4.3	—	—	V
Bus inputs pins 13-14-15 High level Low level	 V_{HL} V_{LL}	 3.5 —	 — —	 — 1	 V V

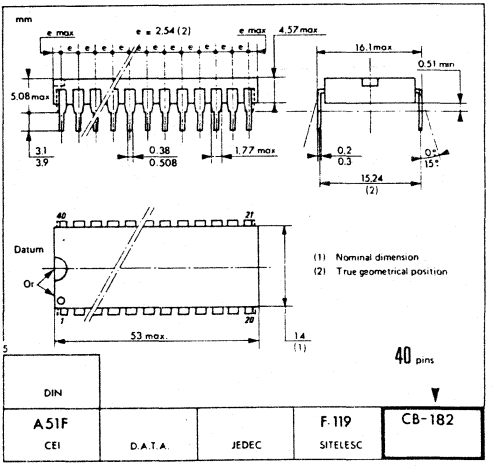
TYPICAL APPLICATION



PHYSICAL DIMENSIONS

CB-132

PLASTIC PACKAGE



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NOTES

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THOMSON COMPONENTS SEMICONDUCTEURS

TEA5620

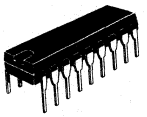
COLOR TV PAL DECODER

MAIN FEATURES

- Phase locked reference oscillator
- U and V axis decoders
- ACC and identification detectors
- Killer
- Use of a standard 4.43 MHz Xtal
- Compatibility with the SECAM decoder TEA 5630 for PAL-SECAM application.

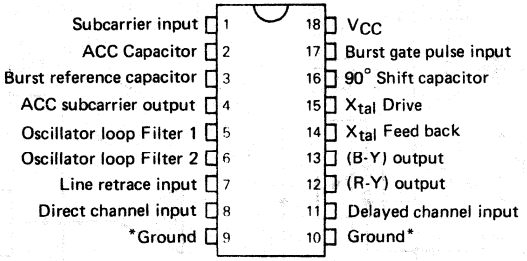
COLOR TV PAL DECODER

CASE CB-181



PLASTIC PACKAGE

PIN ASSIGNMENT



*Pins 9 and 10 have to be both grounded.

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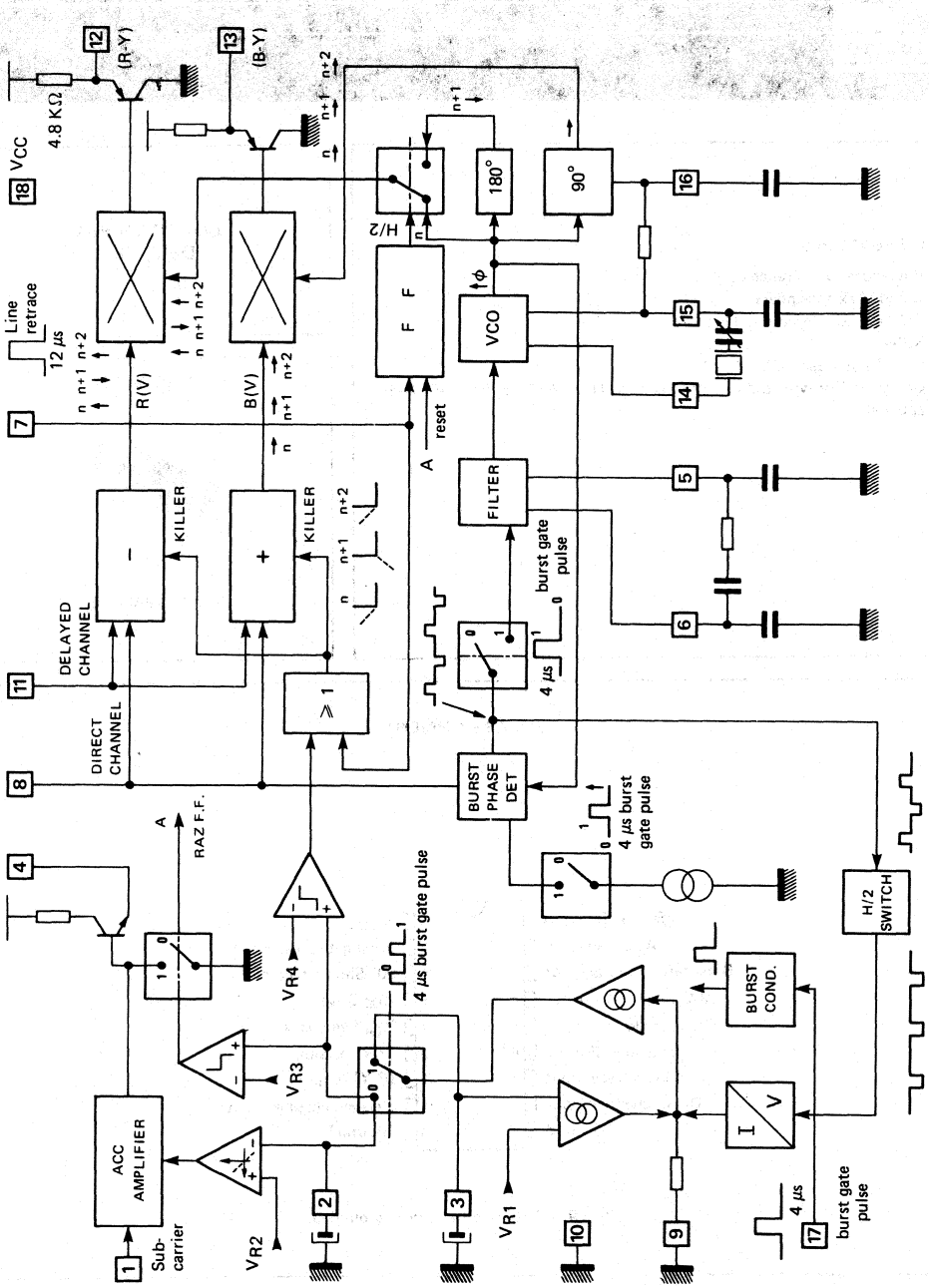
BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	14.4	V
Power dissipation	P_D	800	mW
Operating ambient temperature	T_{amb}	−20 + 70	°C
Storage temperature	T_{stg}	−55 + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal resistance Junction-ambient	$R_{th\ amb}$	70	°C/W

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = +25°C$ $V_{CC} = 12$ V (unless otherwise specified)

Test circuit 1

Characteristics		Switch state S1	Switch state S2	Min	Typ	Max	Unit
Operating Supply Voltage	Pin 18	1	1	10	12	14.4	V
Supply current	Pin 18	1	1	—	40	52	mA
DC voltage at:							
	Pin 1	1	1	5.1	5.7	6.3	V
	Pin 4	0	1	7.6	8.5	9.4	V
	Pin 5	1	2	6.2	7.7	9.2	V
	Pin 6	1	2	6.2	7.7	9.2	V
	Pin 8 - Pin 11	1	1	2.2	2.5	2.8	V
	Pin 12 - Pin 13	1	1	9.5	10.3	11.1	V
	Pin 14	1	2	8.7	9.5	10.7	V
	Pin 15 - Pin 16	1	1	2.7	3.3	3.9	V
DC voltage, with sample pulse to pin 17, at:							
	Pin 2 - Pin 3	0	3	4.3	4.7	5.3	V

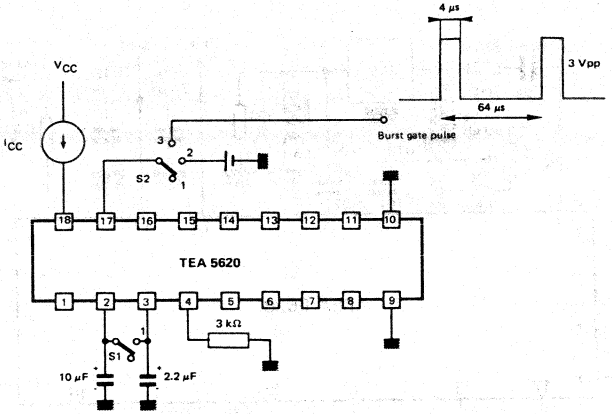
AC ELECTRICAL CHARACTERISTICS

$T_{amb} = +25°C$ $V_{CC} = 12$ V (unless otherwise specified)

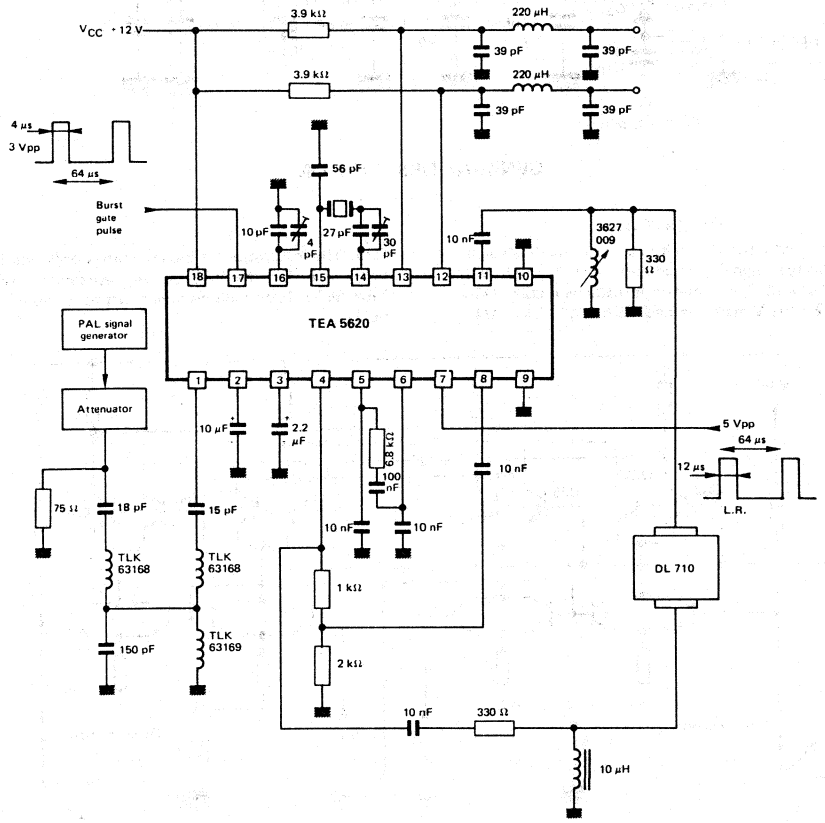
Test circuit 2

Characteristics		Symbol	Min	Typ	Max	Unit
ACC amplifier output voltage (Burst input: 0.1 V_{PP})	Pin 4	BoV	0.45	0.6	0.76	V_{PP}
ACC amplifier output voltage variation (Burst input: + 6 dB = 0.2 V_{PP})	Pin 4	Δ BoV_1	- 1	0	+ 1	dB
ACC amplifier output voltage variation (Burst input: - 20 dB = 10 mV_{PP})	Pin 4	Δ BoV_2	- 5	- 2	+ 1	dB
R-Y output voltage (Colour bar input signal: 0.1 V_{PP})	Pin 12	$ED1_{RY}$	0.7	1.4	1.95	V_{PP}
B-Y output voltage (colour bar input signal: 0.1 V_{PP})	Pin 13	$ED1_{BY}$	0.9	1.5	1.95	V_{PP}
Output voltage ratio: B-Y/R-Y		$\frac{ED1_{BY}}{ED1_{RY}}$	0.9	1.05	1.15	—
R-Y output voltage variation (V_{CC}: 12 V to 14.4 V V_{CC}: 12 V to 9.6 V)	Pin 12	Δ $ED1_{RY}$	0.15	—	0.55	V_{PP}
B-Y output voltage variation (V_{CC}: 12 V to 14.4 V V_{CC}: 12 V to 9.6 V)	Pin 13	Δ $ED1_{BY}$	0.15	—	0.55	V_{PP}
HF residual voltage (colour bar input signal: 0.1 V_{PP})	Pins 12 - 13	EL	—	100	120	mV_{PP}
Colour killer level (Reference input signal: 0.1 V_{PP})		EK	- 40	- 35	- 30	dB
Colour killer leakage (Colour killer on)	Pins 12 - 13	ELK	—	—	20	mV_{PP}
Minimum supply voltage for internal oscillator operation		V_{CC}	—	6	8	V
Input impedance (Input signal: F = 4.43 MHz Vi = 100 mV_{PP})	Pin 1	Ri_1 Ci_1	— —	2.8 10	— —	KΩ pF
Delay time between line retrace pulse and first colour response	Pin 12	To	0.4	1.3	2	μs
VCO control sensitivity: variation of frequency oscillator versus pin 5 to 6 difference voltage (Burst input 0.7 V_{PP} on pin 8)			—	1.8	—	Hz/mV
Pull-in frequency range (Variation of burst frequency)	Pin 15	Fp	—	± 800	—	Hz
Phase hold characteristics (Phase deviation for ΔF burst = 100 Hz)		∅	—	0.03	—	°/Hz
Line retrace threshold	Pin 7	V_{dlr}	—	2.5	—	V
Sampling pulse threshold	Pin 17	V_{dl}	0.6	0.8	1	V

Test circuit 1

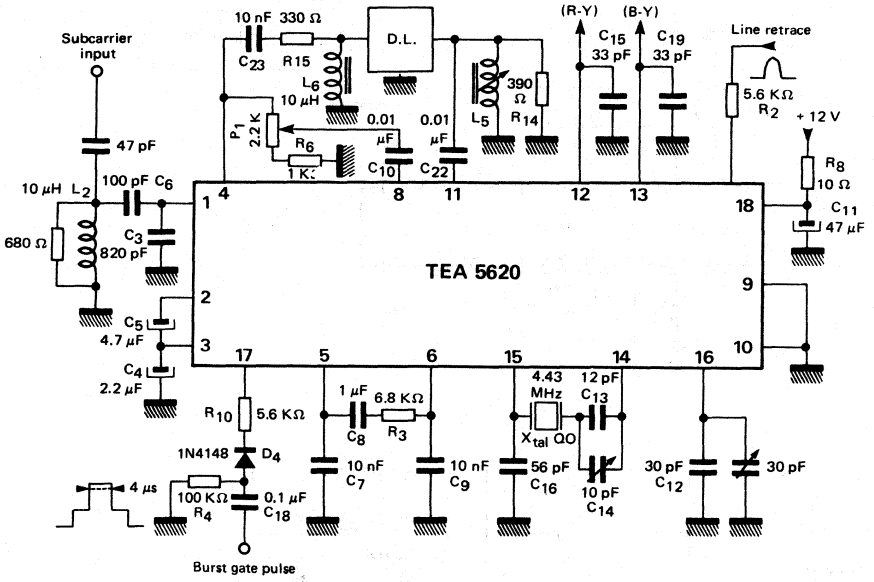


Test circuit 2



Chroma input **0 dB** **Burst 100 mVpp** **10 ops**

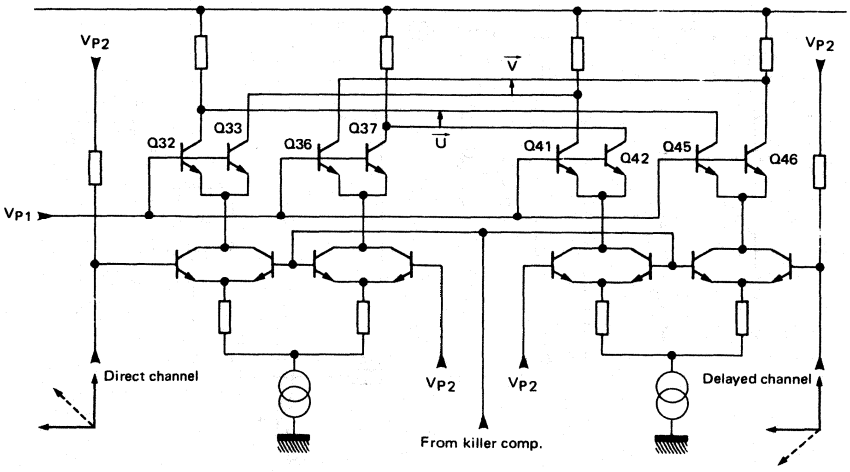
TYPICAL PAL APPLICATION



GENERAL DESCRIPTION

DL MATRIX

The adding and substraction function for the direct signal and the delayed signal are also performed by the IC with the under circuit. The U matrix is made with Q32 - Q45 - Q37 - Q42 ; the V matrix is made with Q33 - Q41 - Q46 - Q36. The integration of the DL matrix only requires one delay line for the PAL/SECAM application with the TEA 5630. It also allows lower cost for external components.



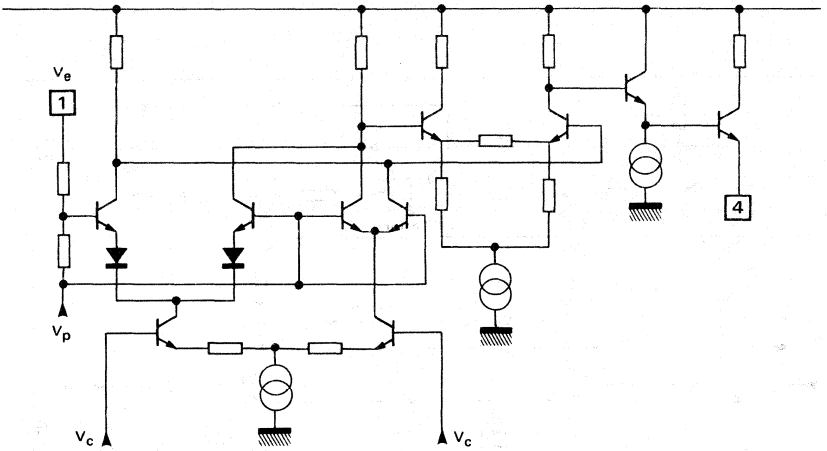
ACC AMPLIFIER

This ACC amplifier is performed with a double differential stage. The subcarrier is sent to the input of the first pair, while the second is connected to a reference voltage. The gain of the amplifier is controlled by the ACC voltage, by switching the bias current through a third differential pair.
The dynamic range obtained by this device is 32 dB. The bias voltage on the pin 1 is 5.6 V. The burst signal delivered by the pin 4 is about 0.6 Vpp for an input signal on pin 1 variable from 5 to 200 mV.

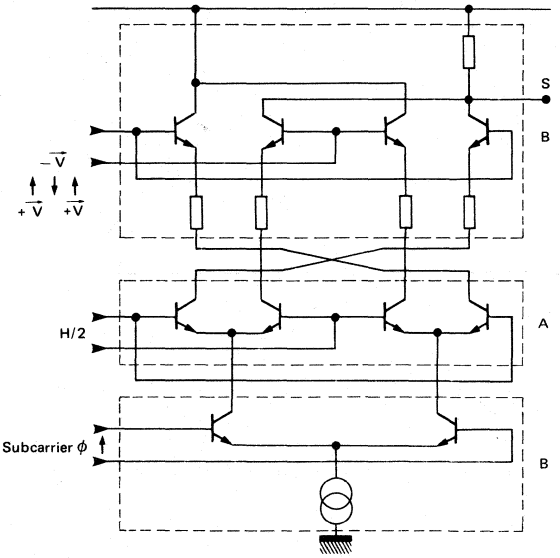
U AND V AXIS DECODERS

They consist on two phase detector stages (B). They provide output signals proportionnal to the magnitude of the chroma signal phased with the regenerated subcarrier feeding the stage.
The subcarrier is fed to the Vaxis decoder through an H/2 switch (A). This switch is required to make the phase of this signal the same than the burst.

ACC AMPLIFIER



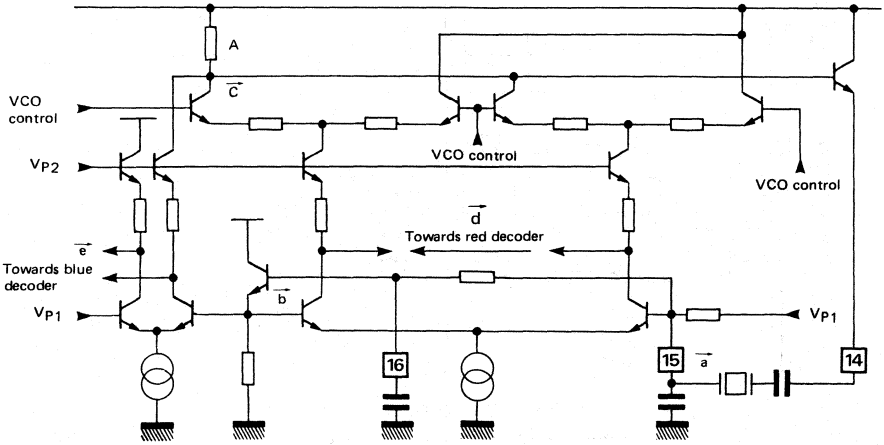
U AND V AXIS DECODERS

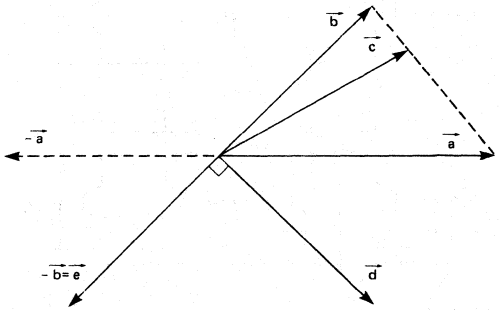


VOLTAGE CONTROL OSCILLATOR

The frequency of the VCO is depending on the vector adding performed at point A between $\vec{b}$ and $\vec{d}$ (see graphe). This adding is controlled by the voltage coming from the burst phase detector. This VCO is attractive because it uses a standard low cost Xtal. The 90° phase shift is made by vector addition and by a 45° phase shifter connected to the pin 16.

VOLTAGE CONTROL OSCILLATOR

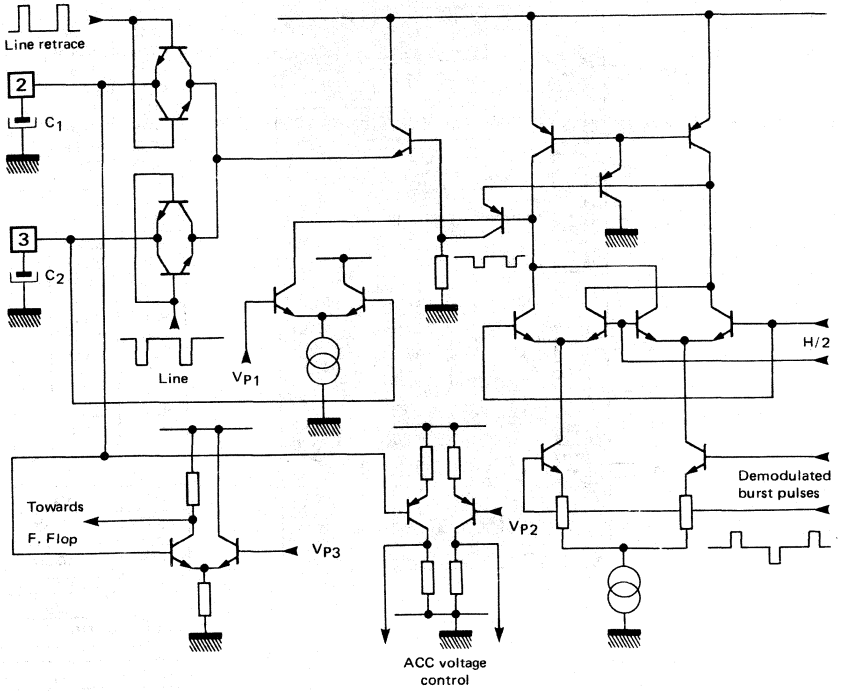




SAMPLING AND HOLD STAGE

This stage performs the identification and provides the ACC control voltage. A bias voltage is stored in C_2 capacitor during the line trace. The C_1 capacitor stores this bias voltage decreased by the demodulated burst peak value. So the differential voltage between C_1 and C_2 is not depending of a bias voltage, out of any drift, and therefore suitable to control the ACC amplifier.

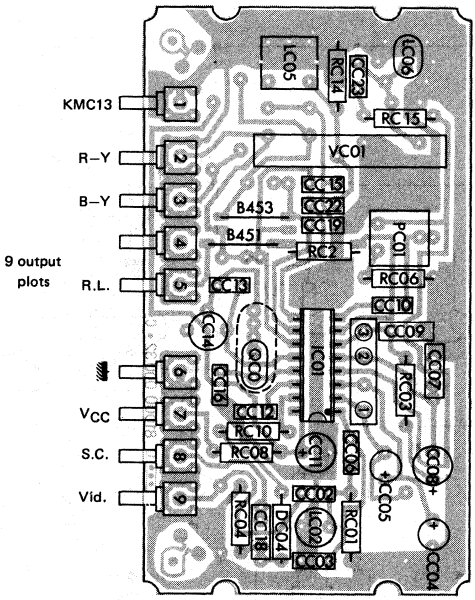
SAMPLING AND HOLD STAGE



TYPICAL APPLICATION

See electric diagram page 6

COMPONENT SIDE



N°	Capa.	U	%
CC02	47 pF		
CC03	820 pF		
CC04	2.2 µF	63	
CC05	4.7 µF	35	
CC06	100 pF		
CC07	0.01 µF	250	
CC08	1 µF	63	
CC09	0.01 µF	250	
CC10	10 nF		
CC11	47 µF	16	
CC12	56 pF		
CC13	12 pF		
CC14	10-30 pF		
CC15	33 pF		
CC16	56 pF		
CC18	0.1 µF	100	
CC19	33 pF		
CC22	10 nF		
CC23	10 nF		

N°	Value	P	%
RC01	820 Ω		5
RC02	5.6 k		5
RC03	6.8 kΩ		5
RC04	100 kΩ		5
RC06	1 kΩ		5
RC08	27 Ω		
RC10	5.6 kΩ		5
			5
			5
RC14	390 Ω		5
RC15	330 Ω		5

N°	Value
LC02	10 µH
LC05	7 - 13 µH
LC06	10 µH

N°	Value
VC01	DL710

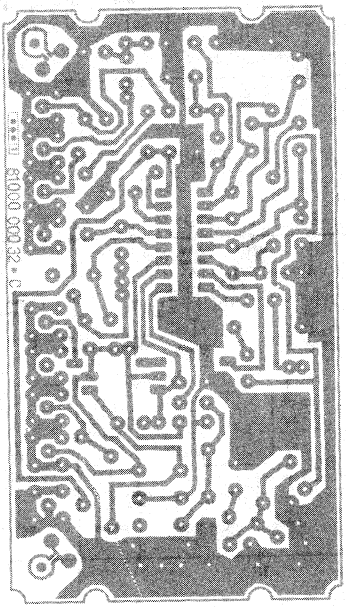
N°	Value
PC01	2.2 kΩ

N°	Value
QC0	4433.619 KHz

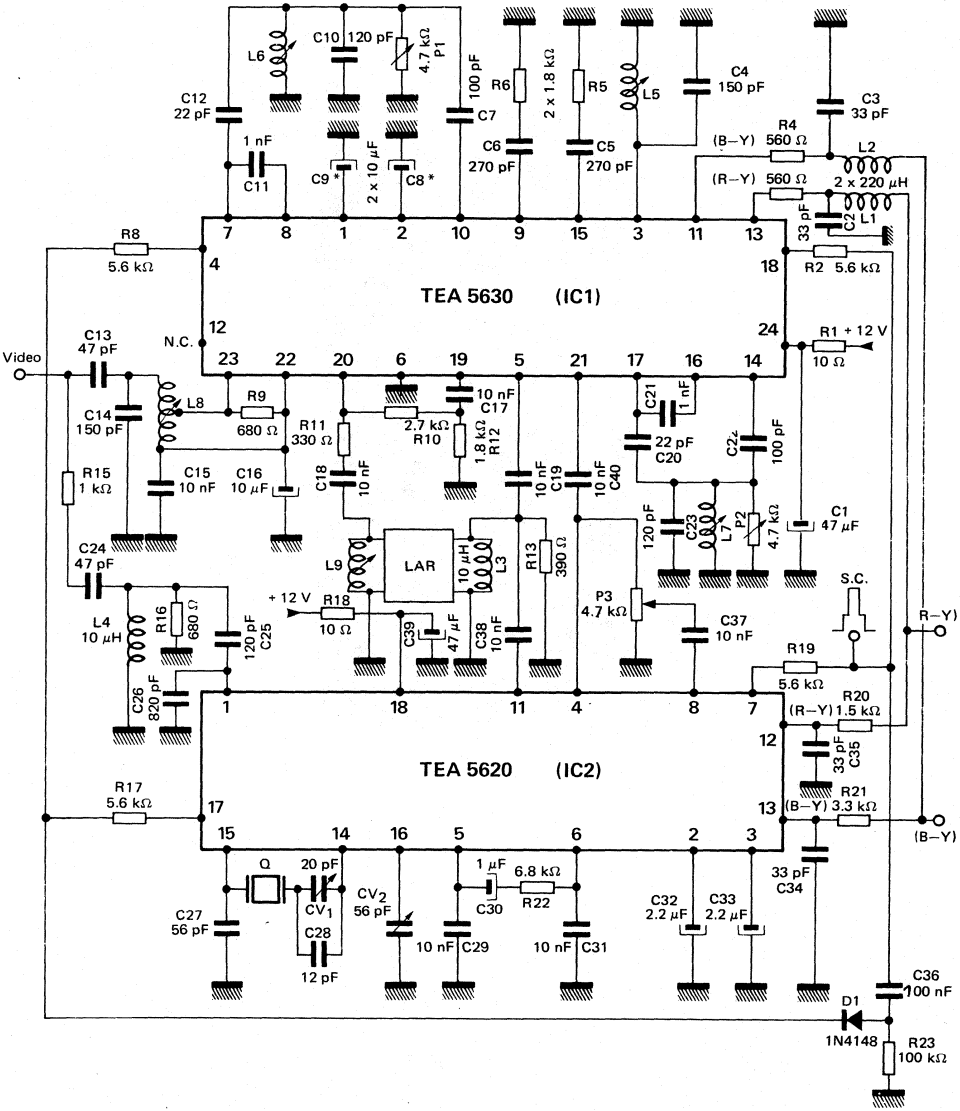
N°	Type
DC04	1N4148

N°	Type
IC01	TEA 5620

COPPER SIDE

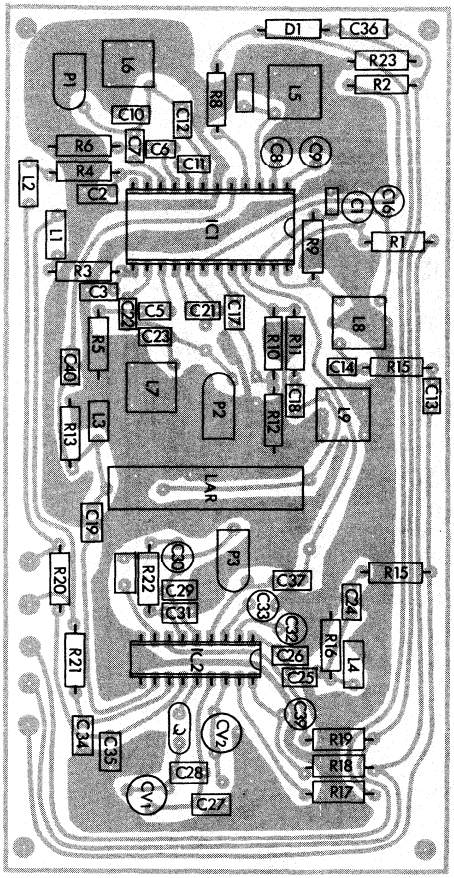


PAL-SECAM APPLICATION
TEA5620-TEA5630



* C8, C9 values can be reduced to 1 µF (polypropylène capacitors) if line identification only.

COMPONENT SIDE



N°	Value
C1	47 µF
C2	33 pF
C3	33 pF
C4	150 pF
C5	270 pF
C6	270 pF
C7	100 pF
C8-C9	10 µF/16 V
C10	120 pF
C11	1 nF
C12	22 pF
C13	47 pF
C14	150 pF
C15	10 nF
C16	10 µF/16 V
C17	10 nF
C18	10 nF
C19	10 nF
C20	22 pF
C21	1 nF
C22	100 pF
C23	120 pF
C24	47 pF
C25	120 pF
C26	820 pF
C27	56 pF
C28	12 pF
C29	10 nF
C30	1 µF/16 V
C31	10 nF
C32	2.2 µF/16 V
C33	2.2 µF/16 V
C34	33 pF
C35	33 pF
C36	100 nF
C37	10 nF
C38	10 nF
C39	47 µF/25 V
C40	10 nF

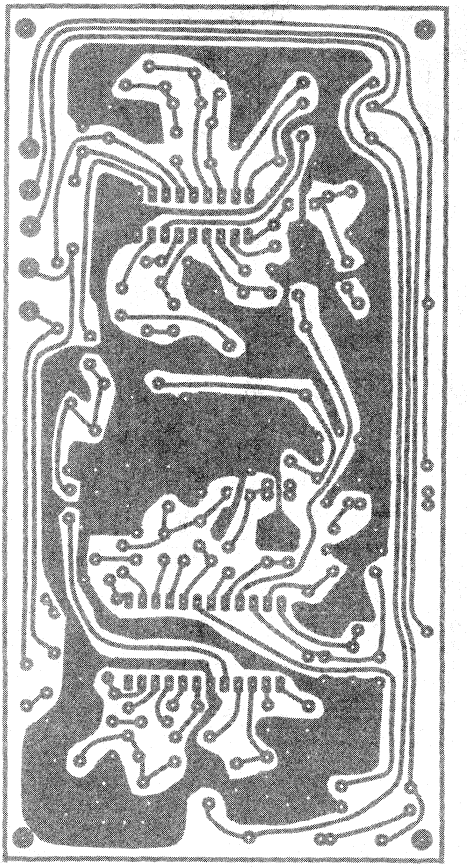
N°	Value
R1	10 Ω
R2	5.6 kΩ
R3	560 Ω
R4	560 Ω
R5	1.8 kΩ
R6	1.8 kΩ
R8	5.6 kΩ
R9	680 Ω
R10	2.7 kΩ
R11	330 Ω
R12	1.8 kΩ
R13	390 Ω
R15	1 kΩ
R16	680 Ω
R17	5.6 kΩ
R18	10 Ω
R19	5.6 kΩ
R20	1.5 kΩ
R21	3.3 kΩ
R22	6.8 kΩ
R23	100 kΩ

N°	Type	Value
L5	TOKO RCL 36270 - 14	10-15 µH
L6	TOKO RCL 36270 - 13	7 µH
L7	TOKO RCL 36270 - 13	7 µH
L9	TOKO RCL 36270 - 09	10 µH

N°	Value
P1	4.7 kΩ
P2	4.7 kΩ
P3	4.7 kΩ
Q quartz	4.433 MHz
CV_1	3 - 30 pF
CV_2	6 - 60 pF

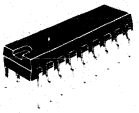
N°	Type or value
D1	1N4148
LAR:	LAA64 µs
IC_1	TEA 5630
IC_2	TEA 5620
L1	220 µH
L2	220 µH
L3	10 µH
L4	10 µH
L8	0.7 - 1.3 µH

COPPER SIDE

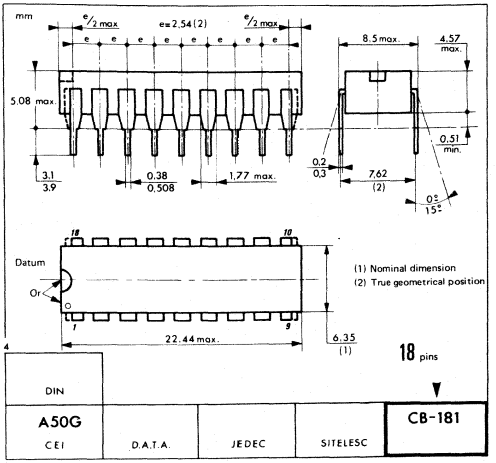


PHYSICAL DIMENSIONS

CB-181



PLASTIC PACKAGE



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NOTES

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TEA5630

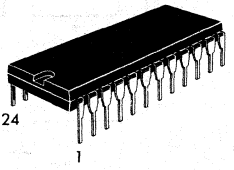
COLOR TV SECAM DECODER FOR LOW-COST TV SETS

MAIN FEATURES

- Subcarrier limiter
- R–Y, B–Y } demodulators
- Identification and killer
- PAL-SECAM switches for multistandard application.

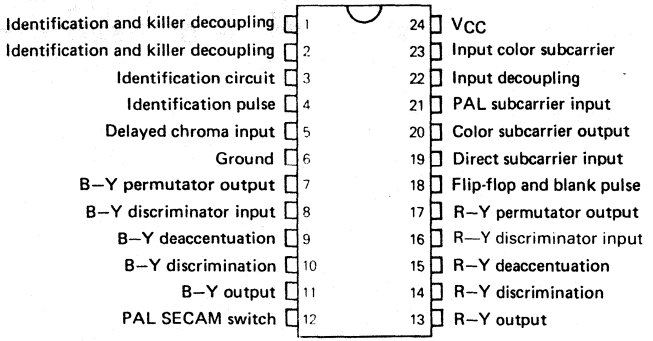
COLOR TV SECAM DECODER FOR LOW-COST TV SETS

CASE CB-68



PLASTIC PACKAGE

PIN ASSIGNMENT



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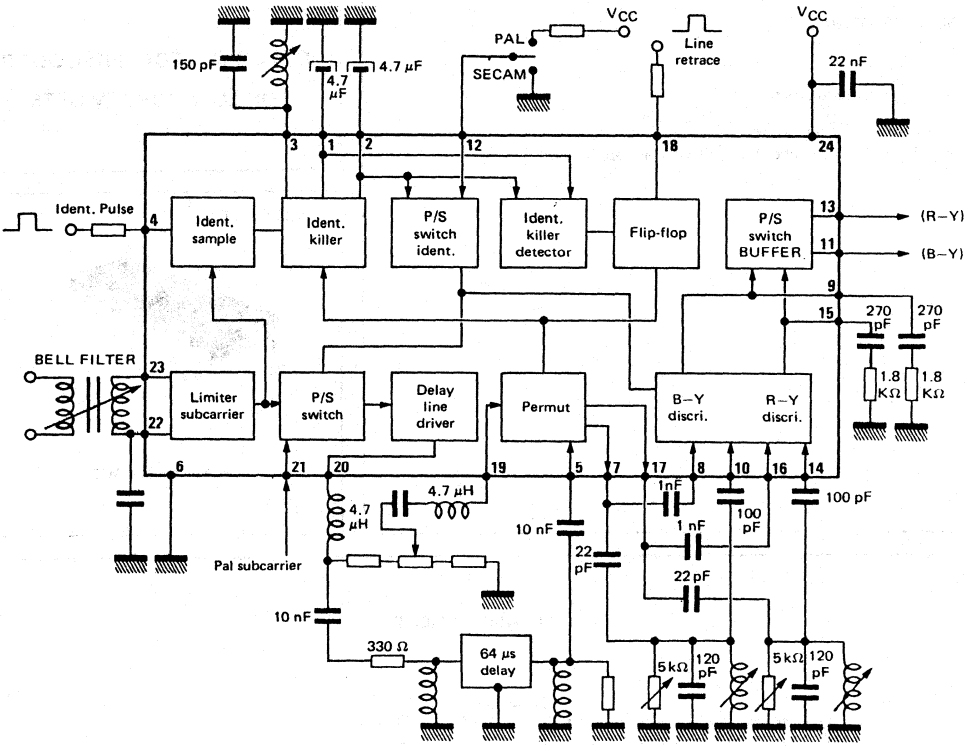
BLOCK DIAGRAM



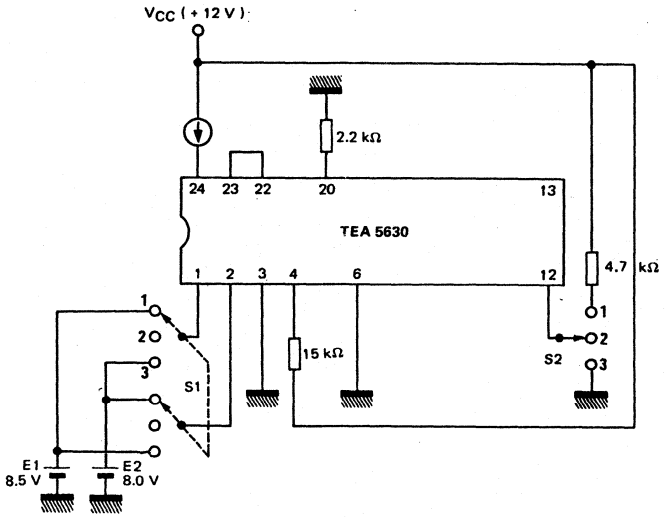
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	14.4	V
Power dissipation	P_{tot}	760	mW
Operating ambient temperature	T_{oper}	- 20 + 70	°C
Storage temperature	T_{stg}	- 55 + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal resistance Junction-ambient	$R_{th(j-a)}$	60	°C/W

TEST CIRCUIT 1



DC ELECTRICAL CHARACTERISTICS

$T_{amb} = +25°C$ $V_{CC} = 12$ V (unless otherwise specified)

Test circuit 1

Characteristics		Switch state		Min	Typ	Max	Unit
		S1	S2				
Operating Supply Voltage	Pin 24	2	2	9.6	12	13	V
Supply current	Pin 24	2	2	20	30	40	mA
DC voltage at:							
	Pin 1, pin 2	2	3	4.8	5.7	6.4	V
	Pin 5, pin 19	2	3	1.8	2.4	3	V
	Pin 7, pin 17	2	3	10.6	11.2	11.8	V
	Pin 8, pin 16	2	3	4.7	5.4	6.1	V
	Pin 9, pin 15	2	3	6.3	7.2	8	V
	Pin 10, pin 14	2	3	2.5	3.3	4	V
	Pin 11, pin 13	2	3	6.8	8	9	V
	Pin 20	2	3	6.8	7.9	9	V
	Pin 21	2	3	2.6	3.3	4	V
	Pin 22	2	3	2.3	3	3.7	V
	Pin 9, pin 15	2	1	11.7	11.9	—	V
	Pin 11, pin 13	2	1	11.7	11.9	—	V
	Pin 12	2	2	0.85	1.1	1.3	V
	Pin 12	1	2	0	0.1	0.2	V
	Pin 12	3	2	0	0.1	0.2	V

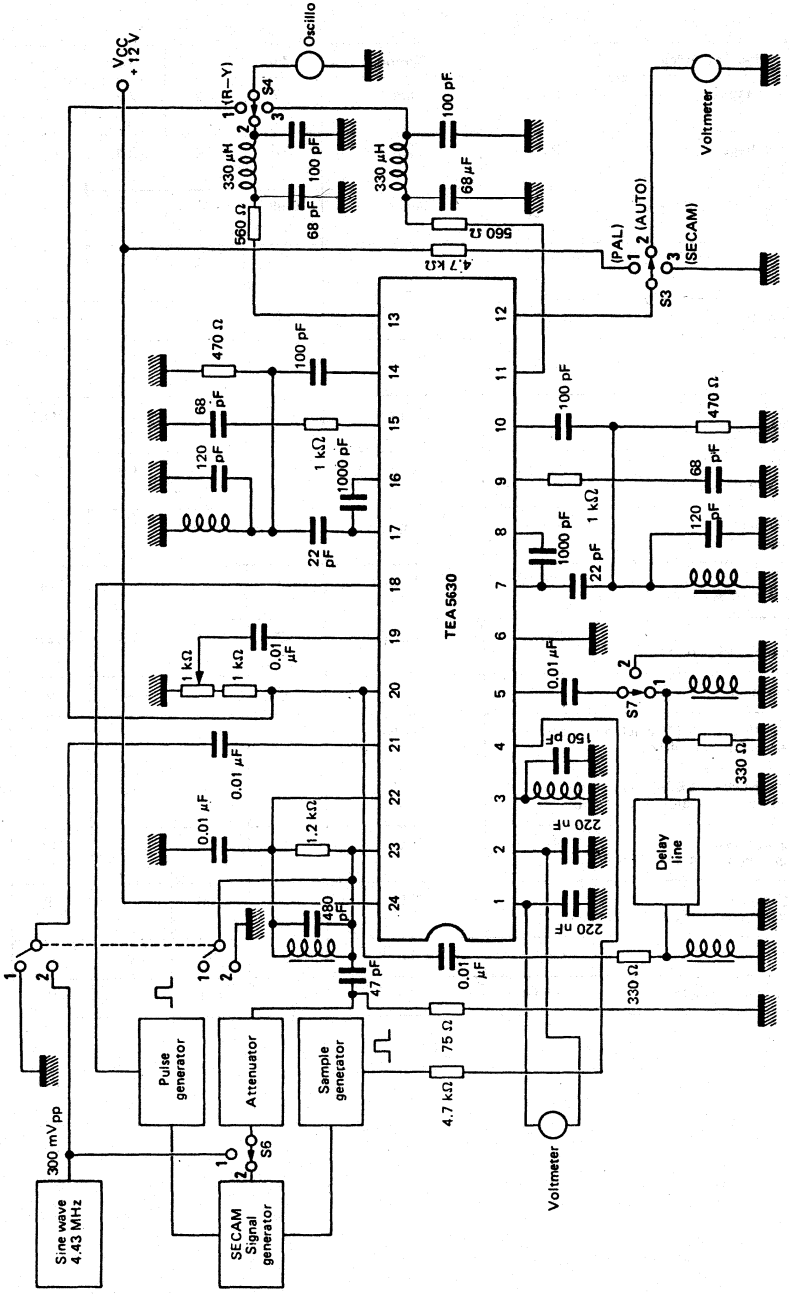
AC ELECTRICAL CHARACTERISTICS

$T_{amb} = +25°C$ $V_{CC} = 12$ V (unless otherwise specified)

Test circuit 2

Characteristics		Symbol	Min	Typ	Max	Unit
Limiter amplifier output voltage (V_I = 100 mVpp)	Pin 20	Elim-1	1.7	2.2	2.7	Vpp
Limiter amplifier output voltage (V_I = -30 dB = 3.2 mVpp)	Pin 20	Elim-2	0.6	1.4	2.4	Vpp
PAL amplifier gain: VO (pin 20)/V_I (pin 21) (V_I = 300 mVpp)		Av PAL	0.95	1.1	1.3	—
Permutator output (V_{pin} 19-5: 400 mVpp)	Pins 7 - 17		—	1.4	—	Vpp
Permutator input impedance	Pins 19 - 5		—	2.5	—	KΩ
Permutator crosstalk (S7 = 2)		CT1	—	- 60	—	dB
B-Y output voltage (Colour bar signal generator 75%)	Pin 11	$ED1_{BY}$	0.6	1	1.3	Vpp
R-Y output voltage (Colour bar signal generator 75%)	Pin 13	$ED1_{RY}$	0.7	1.2	1.6	Vpp
Output voltage ratio R-Y/B-Y (Colour bar signal generator 75%)		R_O	0.95	1.25	1.5	—
B-Y output voltage (Colour bar signal generator 75% - 16 dB)	Pin 11	$ED2_{BY}$	0.6	1	1.3	Vpp
R-Y output voltage (Colour bar signal generator 75% - 16 dB)	Pin 13	$ED2_{RY}$	0.7	1.2	1.6	Vpp
PAL/SECAM switch threshold	Pin 12		—	1.1	—	V
Input level attenuation for PAL/SECAM switching - measure on pin 12 (colour bar generator 75% - 40 dB)		V12 R1	0.9	1.05	1.2	V
Input level attenuation for NO PAL/SECAM switching - measure on pin 12 (colour bar generator 75% - 18 dB)		V12 R2	—	—	0.2	V
PAL/SECAM switching crosstalk (SECAM mode - PAL input signal pin 21: 300 mVpp)		PRS1	—	- 33	—	dB
PAL/SECAM switching crosstalk (PAL mode - SECAM input signal pins 23 - 22: 5 mVpp)		PRS2	—	- 50	—	dB
Line retrace threshold	Pin 18	FF	0.85	1	1.07	V
Identification sampling pulse threshold	Pin 4		—	0.8	—	V

TEST CIRCUIT 2



	V_O (1)	V_O (2)	Av	e_o (1) B–Y	e_o (1) R–Y	e_k	C_{T1}	C_{T2}
S_3	2	3	1	2	2	.3	2	3
S_4	1	1	1	3	3	3	3	1
S_5	1	1	2	1	1	1	1	2
S_6	2	2	2	2	2	2	2	2

GENERAL DESCRIPTION

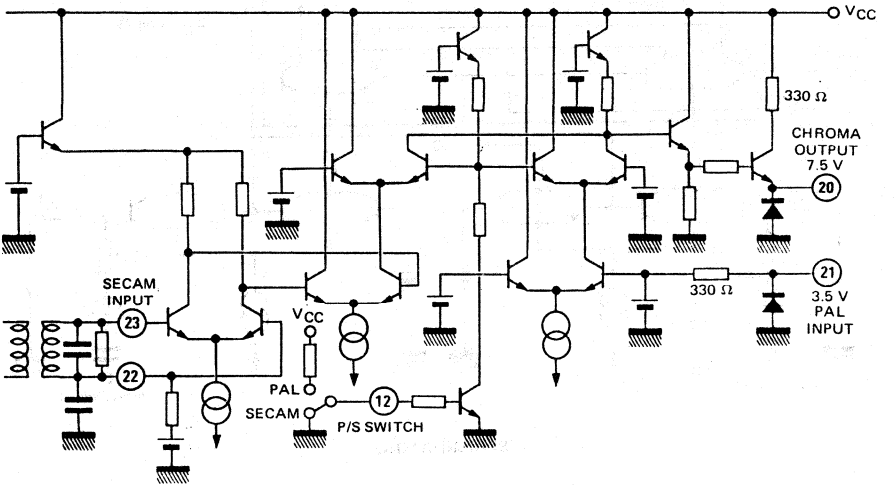
LIMITER AND CHROMA PAL/SECAM SWITCHING

The chroma signal is applied to the input of a limiter stage. After limitation the output signal is sent to an electronical switch which selects the signal coming from the limiter (for SECAM) or from the PAL input (Pin 21). The high output voltage of chrominance signal, 2.2 V_{pp} in SECAM operation, permits to obtain a minimum of crosstalk in the permutation and discrimination. The DC output voltage of the PAL IC connected in parallel for PAL/SECAM must be higher than $V_{CC} - 5$ V.

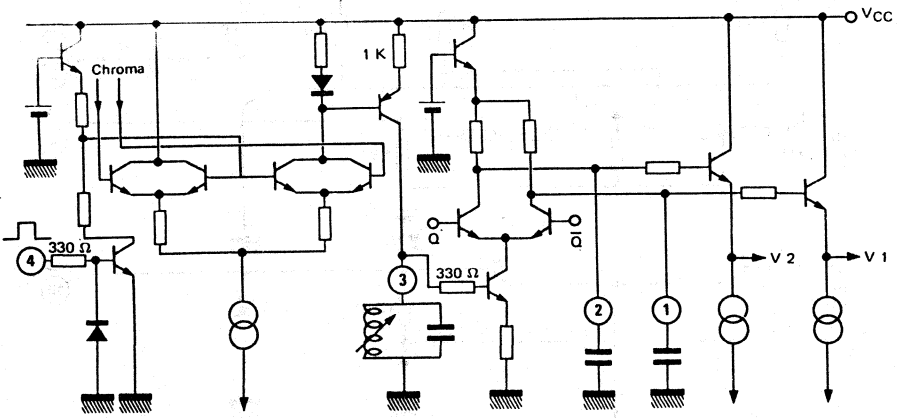
IDENTIFICATION AND KILLER

The identification information is sampled during the identification pulse (PIN 4). The burst differential amplitude voltage on the according circuit pin 3 is amplified and held by capacitors pin 2 and pin 1 to give the right flip-flop phase and killer information.
The circuit is able to identify line by line or line and frame. The choice of identification mode is programmable by the user depending on the identification pulse pin 4.

LIMITER AND CHROMA PAL/SECAM SWITCH



IDENTIFICATION AND KILLER



PERMUTATOR

Two inputs on the permutator :

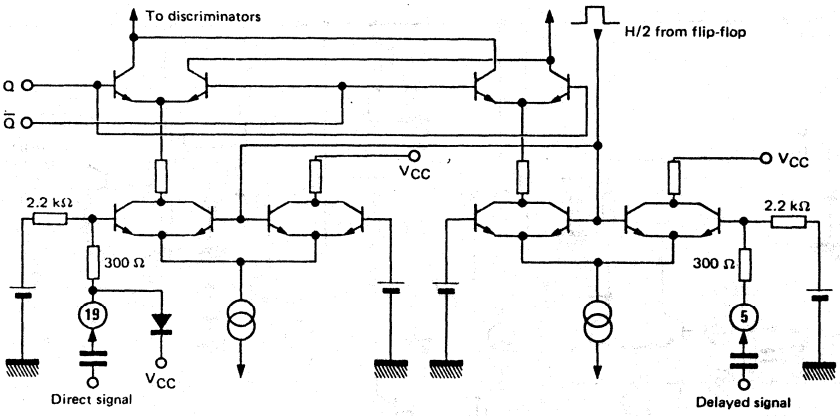
- the direct signal is sent on pin 19,
- the delayed signal is sent on pin 5.

The permutator is controled by a flip-flop at H/2 frequency in order to have (R−Y) signal on pin 17 and (B−Y) signal on pin 7. The output chroma signal typical value is 1.4 V.

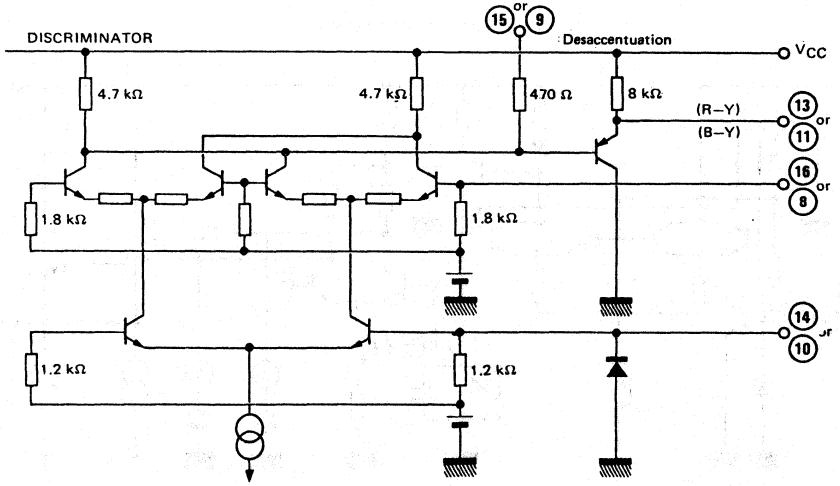
DISCRIMINATORS

They use coïncidence detectors with external according circuit L-C. The (R−Y) and (B−Y) demodulated signal amplitude and linearity can be adjusted by the choice of the damping resistor value in parallel with the L-C circuit. The desaccentuation circuit is connected on the load of the coïncidence detection.
Two PNP emitter followers provide the (R−Y) and (B−Y) signals at low impedance output.
In PAL operating the output impedance is equivalent to a 8 KΩ resistance between output and V_{CC}.

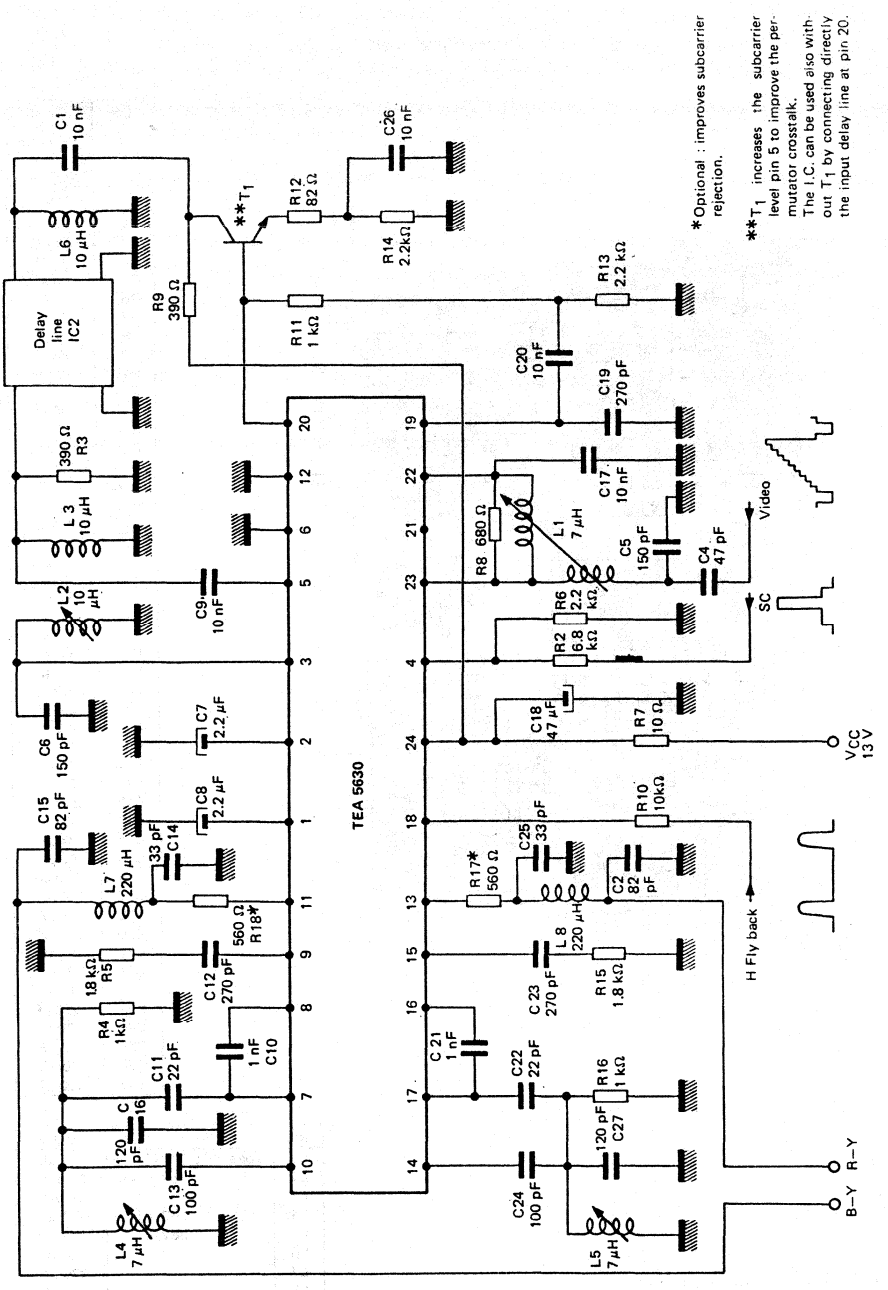
PERMUTATOR



DISCRIMINATORS

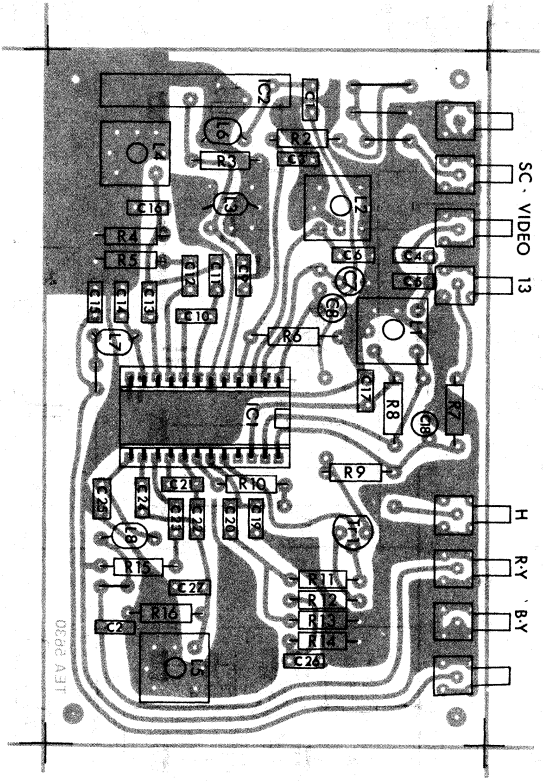


TYPICAL APPLICATION



P.C BOARD AND COMPONENT LAYOUT (FOR SECAM DECODER)

COMPONENT SIDE



N°	Type
Tr1	BC548 B

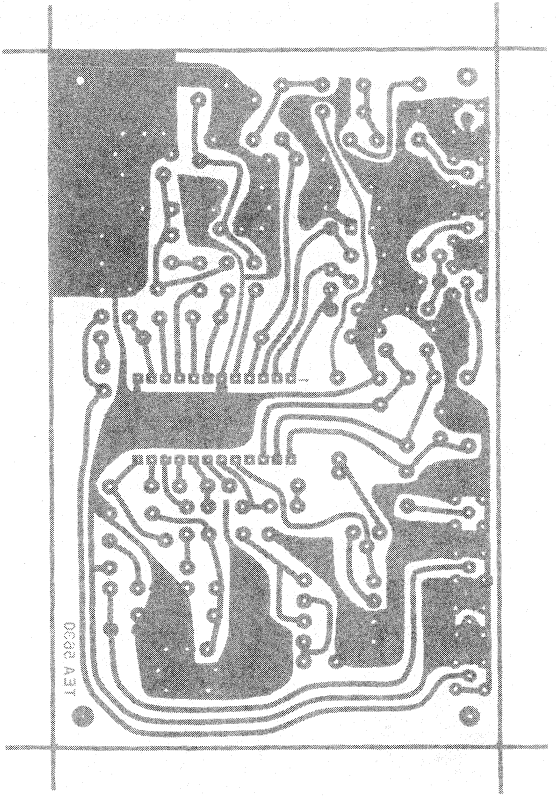
N°	Value
R2	6.8 kΩ
R3	390 Ω
R4	1 kΩ
R5	1.8 kΩ
R6	2.2 kΩ
R7	10 Ω
R8	680 Ω
R9	390 Ω
R10	10 kΩ
R11	1 kΩ
R12	82 Ω
R13	2.2 kΩ
R14	2.2 kΩ
R15	1.8 kΩ
R16	1 kΩ
R17*	560 Ω
R18*	560 Ω

N°	Caps.
C1	10 nF
C2	82 pF
C3	100 pF
C4	47 pF
C5	150 pF
C6	150 pF
C7	2.2 µF
C8	2.2 µF
C9	10 nF
C10	1 nF
C11	22 pF
C12	270 pF
C13	100 pF
C14	33 pF
C15	82 pF
C16	120 pF
C17	10 nF
C18	47 µF
C19	270 pF
C20	10 nF
C21	1 nF
C22	22 pF
C23	270 pF
C24	100 pF
C25	33 pF
C26	10 nF
C27	120 pF

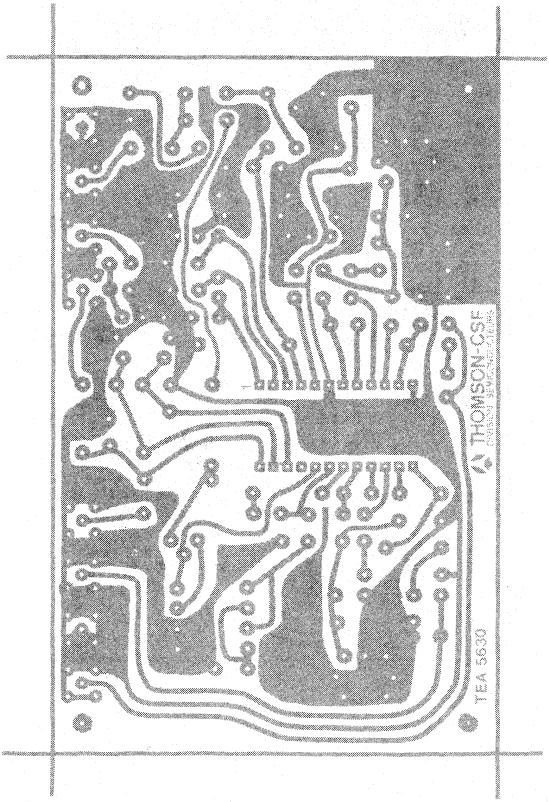
N°	Type	Val.
L1	Toko RCL 3627010	~7 µH
L2	" " 3627014	10-15 µH
L3		10 µH
L4	" " 3627013	~7 µH
L5	" " 3627013	~7 µH
L6		10 µH
L7		220 µH
L8		220 µH

*Optional : improves subcarrier rejection.

COMPONENT SIDE

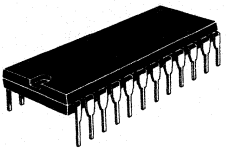


COPPER SIDE

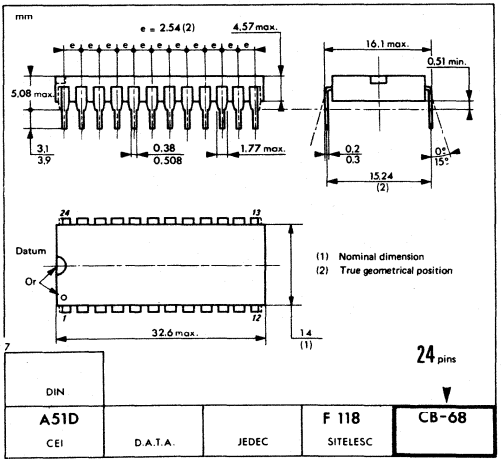


PHYSICAL DIMENSIONS

CB-68



PLASTIC PACKAGE



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Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TEA5640

MULTISTANDARD COLOR TV DECODER

ADVANCE INFORMATION

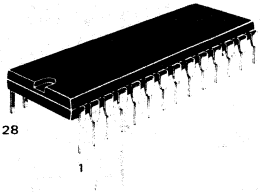
The TEA5640 is a multistandard TV decoder for PAL-SECAM-NTSC1 (3.58 MHz) and NTSC2 (4.43 MHz). The circuit automatically selects the standard corresponding to the input signal. It produces all the reference frequencies required for decoding, which is achieved by a digital frequency synthesizer. Included on the chip are, four numerical frequency locked loops that allow the elimination of PAL and NTSC crystals. The circuit uses an external reference frequency of 62.5 kHz generally provided by the frequency synthesis tuner of the TV set.

Main features:

- Fully automatic multistandard switching: the circuit includes a scanning control system used for the automatic standard recognition
- No crystals required: all the frequencies are synthesized from the external reference frequency of 62.5 kHz, and from specified data stored in an internal ROM
- Automatic bell filter adjustment
- Automatic delay line compensation adjustment
- Automatic internal PAL and NTSC oscillator adjustment
- Automatic adjustment for FOB and FOR in SECAM.

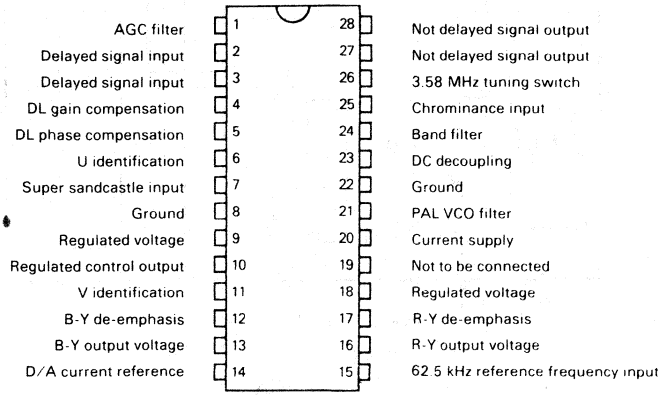
MULTISTANDARD COLOR TV DECODER

CASE CB-132



PLASTIC PACKAGE

PIN ASSIGNMENT



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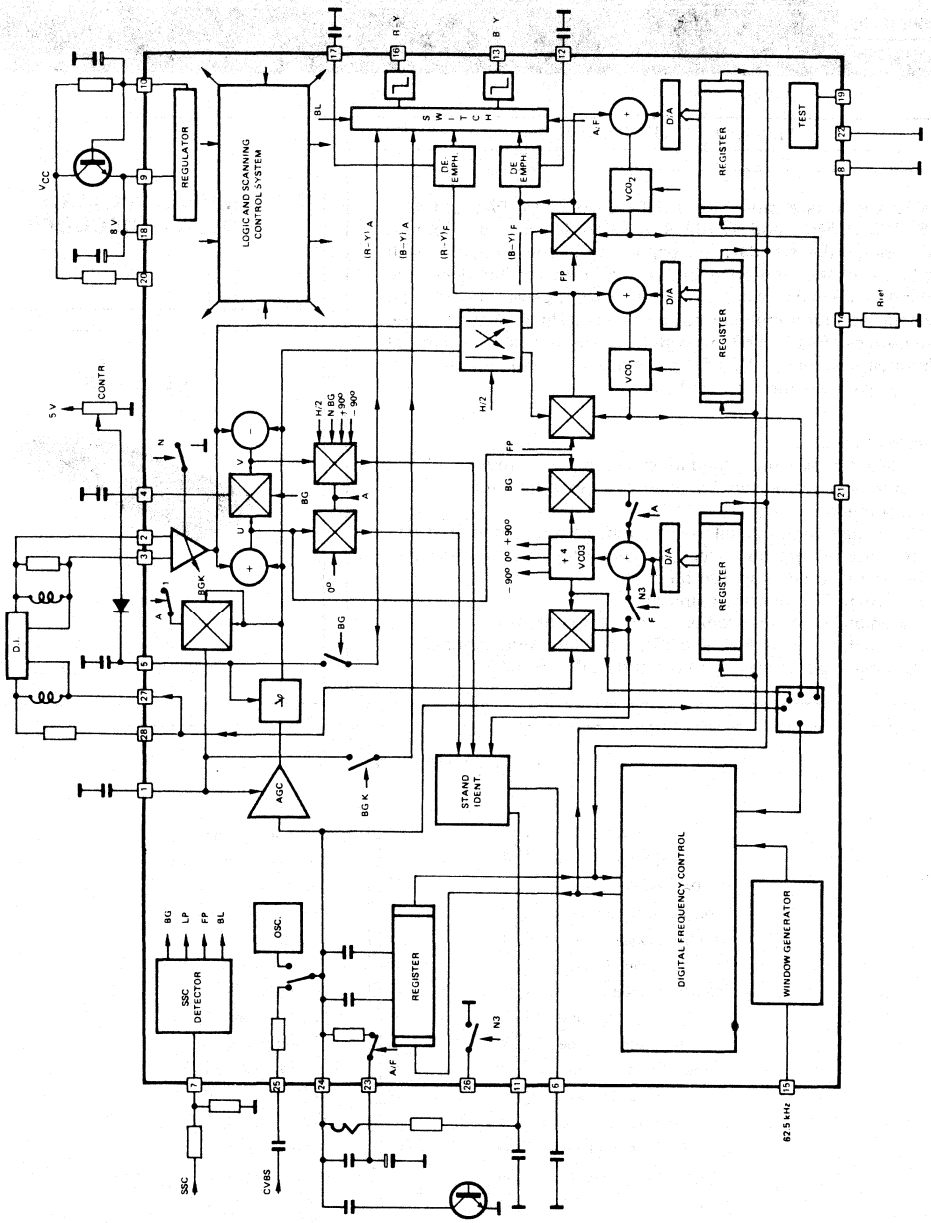
BLOCK DIAGRAM



S: Secam; BP: Bandfilter adjustment; P: Pal; BG: Burstgate
N4: NTSC 4.43; N3: NTSC 3.58; LP: Line Pulse; FP: Frame Pulse
A: Amplit. Modul.; F: Freq. Modul; K: Identification, BL: Blanking

GENERAL DESCRIPTION

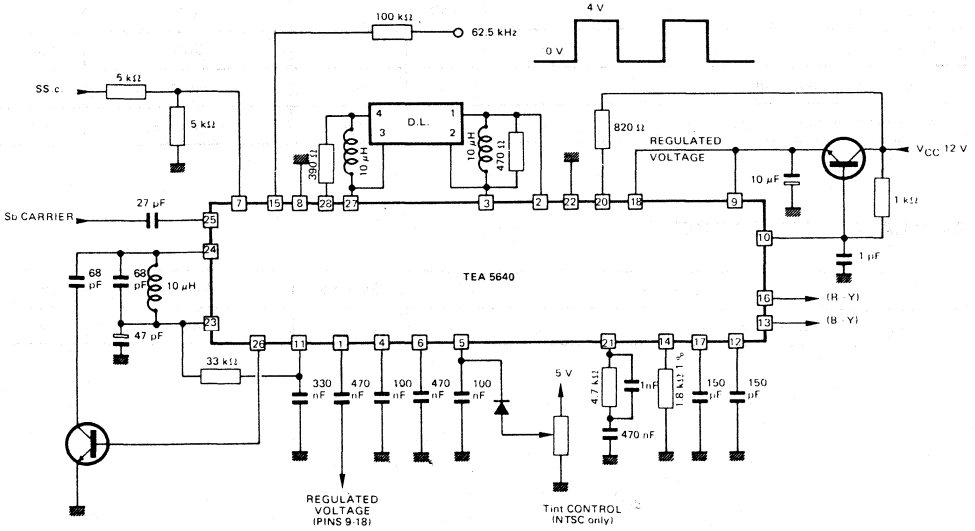
The TEA5640 is a multistandard TV decoder for PAL-SECAM, NTSC 4.43 and NTSC 3.58 signals. The circuit automatically locks itself on the standard of the input signal and produces all the reference frequencies it needs for decoding. This is provided by digital frequency synthesis.

Included on the chip are four numerical locked loops that allow the removal of PAL and NTSC crystals. It works with an external reference frequency of 62.5 kHz which is generally provided by the frequency synthesis tuner of the TV set.

FEATURES

- Full automatic multistandard switching:
  the circuit includes a scanning control system that provides all the switchings required for the automatic standard recognition. This system is synchronized by the frame pulse.
- No crystal requirement:
  the PAL and NTSC frequencies are synthesized originally by the external reference frequency of 62.5 kHz and data stored in the ROM.
- Automatic adjustment of the bell filter:
  by switching an internal capacitor network included in a digital loop.
- Automatic adjustment of the delay line compensations:
  these adjustments are made on the burst and are refreshed every line retrace.
- Automatic adjustment for PAL and NTSC oscillator:
  this oscillator has a digital and an analogic loop. The PAL and NTSC frequencies are memorized in a ROM connected to the digital loop. The digital loop gives the right frequency and the analogic one holds the phase.
- Automatic adjustment of FoR and FoB in SECAM:
  these frequencies are programmed in the ROM and are sent to two other digital loops when SECAM standard is selected.

TYPICAL APPLICATION

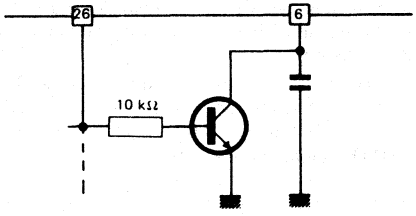


STANDARD SWITCHING AND INHIBITION

NTSC inhibition:
NTSC 1 and 2 standards can be inhibited by connecting pin 6 to the ground.

3.58 MHz filter switching:
Pin 26 can be used to switch external filters when NTSC 1 is selected. (For example luma filter).

3.58 NTSC inhibition:
Pin 26 can be used to inhibit the NTSC 1 standard by connecting the circuit as follows:



SECAM recognition:
- When SECAM on, pin 12 and pin 17 DC voltage is lower than 5 V.
- For other standards, pin 12 and pin 17 DC voltage is regulated V_{CC} (typical 8 V).

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply voltage	Pins 9 - 18	V	9.5	V
Current	Pin 20		200	mA
Operating temperature range		T_{oper}	0 to 70	°C
Storage temperature		T_{stg}	— 40 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	55	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$, $V_{CC} = 12$ V,
Color bar pattern generator on pin 25: $V_I = 250$ mVpp
Refer to application diagram page (unless otherwise specified)

Characteristic		Symbol	Min.	Typ	Max.	Unit
Supplies						
Regulated voltage ($I_{10} = 4$ mA)	Pins 9 - 18	V_{reg}	7.5	8	8.5	V
Supply current	Pin 9 + Pin 18	I_{CC}	—	90	110	mA
Supply current	Pin 9	I_9	—	—	90	mA
Supply current	Pin 18	I_{18}	—	—	20	mA
DC voltage at $I_{20} = 15$ mA	Pin 20	V_{I2L}	—	0.8	—	V
Input current	Pin 10	I_{10}	2	—	20	mA
Transfer characteristic: ($I_{10} = 4.0$ mA)			—	250	—	mA/V
Current reference	Pin 14					
DC voltage ($I_{14} = 0.77$ µA)		V_{14}	1.2	1.4	1.6	V
Internal bias	Pin 23					
DC voltage		V_{23}	3.5	4	4.5	V
Impedance ($I_{out} = 2$ mA)			—	90	110	Ω
Reference clock input F = 62.5 kHz ± 6 Hz	Pin 15					
Low level input current ($V_{15} = 2.1$ V)		I_{15L}	—	— 10	—	µA
High level input current ($V_{15} = 3.2$ V)		I_{15H}	—	5	—	µA
Low level input voltage	R source = 100 kΩ	V_{15L}	0	1	—	V
High level input voltage	R source = 100 kΩ	V_{15H}	—	4	—	V
Voltage threshold			—	2.8	—	V
Super sandcastle detector	Pin 7					
Blanking threshold		V_B	0.5	0.75	0.9	V
Line threshold		V_L	1.6	1.75	1.9	V
Burst gate threshold		V_G	3.2	3.5	3.8	V
Minimum frame blanking duration			1	—	—	msec
Input current ($V_7 = 1.75$ V)		I_7	— 20	—	0	µA
Chrominance input	Pin 25					
DC voltage		V_{25}	—	5.5	—	V
Maximum AC input voltage			—	—	0.5	Vpp
Impedance			0.8	1	—	kΩ

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

Characteristic		Symbol	Min.	Typ	Max.	Unit
B-Y and R-Y outputs	Pins 13 - 16					
(Standard bar pattern generator V_{25} = 250 mVpp)						
B-Y output DC voltage	Pin 13	V_{13}	—	4.15	—	V
R-Y output DC voltage	Pin 16	V_{16}	—	4.15	—	V
Maximum sink current	Pin 13		—	—	— 0.8	mA
Maximum sink current	Pin 16		—	—	— 0.8	mA
B-Y AC voltage		v_{BY}	—	1.34	—	Vpp
R-Y AC voltage		v_{RY}	—	1.05	—	Vpp
$\frac{B\text{-}Y}{R\text{-}Y}$ ratio (all standard modes)			—	1.27	—	—
Residual subcarrier			—	30	—	mV
Crosstalk between outputs (SECAM)			—	—	— 45	dB
Blanking level offset (referred with the achromatic picture level)			—	—	2	%
Differential delay between PAL and SECAM output signals			—	—	50	ns
Delay difference tolerance between NTSC 3.58 MHz and NTSC 4.43 MHz			—	—	50	ns
Delay between chroma output signals and luma signal			—	450	—	ns
B-Y output AC impedance			—	80	—	Ω
R-Y output AC impedance			—	80	—	Ω
Automatic gain control						
SECAM mode						
• 0 dB reference voltage for measurement on Pins 27 - 28 (P25 chroma input voltage = V_{25} = 250 mVpp)			50	150	250	mVpp
• AC voltage variation on Pins 27 - 28 (ΔV_{25} = + 6 dB)			— 3	—	+ 3	dB
• AC voltage variation on Pins 27 - 28 (ΔV_{25} = — 24 dB)			— 5	—	+ 1	dB
PAL/NTSC mode with identification						
• 0 dB reference voltage for measurement on Pins 13 - 16 (P25 chroma input voltage = V_{25} = 250 mVpp)						
• AC voltage variation on Pins 13 - 16 (ΔV_{25} = + 6 dB)			— 3	—	+ 3	dB
• AC voltage variation on Pins 13 - 16 (ΔV_{25} = — 24 dB)			— 5	—	+ 1	dB

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

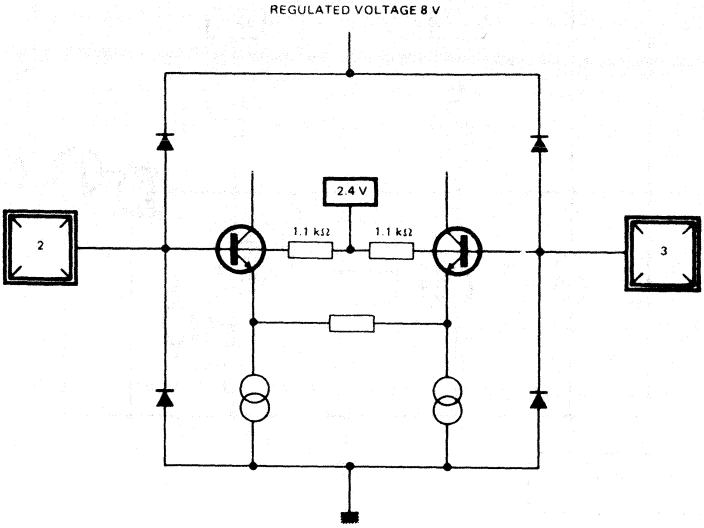
Characteristic		Symbol	Min.	Typ	Max.	Unit
Tint control (NTSC MODE)						
Range of phase change for V Pin 5 changing from 2 to 4.5 V			—	± 45	—	°
DC voltage for 0° Tint change	Pin 5	V_5	—	3.5	—	V
Input current	Pin 5	I_5	0.15	—	0.3	mA
PAL and NTSC detection						
Detection threshold	Pin 6		3	3.7	4	V
NTSC mode inhibition threshold			0.5	—	2.5	V
Leakage current			—	—	0.5	μA
Delayed signal input	Pins 2 - 3					
DC voltage in PAL mode			—	2.4	—	V
Input impedance			0.88	1.1	1.32	kΩ
Delay line attenuation compensation						
Nominal DC voltage on Pin 4 with nominal DL attenuation (V_{2-3}/V_{27-28}) = — 9 dB		V_4	3.8	4	4.2	V
Line to line output amplitude difference measured on Pins 13 - 16, when DL attenuation changed (PAL MODE)						
V_{2-3}/V_{27-28} = — 3 dB		ΔV_{13} ΔV_{16}	—	—	100	mV
V_{2-3}/V_{27-28} = — 15 dB		ΔV_{13} ΔV_{16}	—	—	100	mV
Delay line phase shift compensation						
Nominal DC voltage on Pin 5 with nominal DL phase						
Phase shift V_{27-28}/V_{2-3} = 0°		V_5	5.2	5.5	5.8	V
Line to line output difference measured on Pins 13 - 16, when DL phase shift changed						
phase shift V_{27-28}/V_{2-3} = + 45°		ΔV_{13} ΔV_{16}	—	—	100	mV
phase shift V_{27-28}/V_{2-3} = — 45°		ΔV_{13} ΔV_{16}	—	—	100	mV
Alternation line detection PAL or SECAM	Pin 11					
High differential threshold ($\Delta V_{11H} = V_{11H} - V_{23}$)		ΔV_{11H}	+ 200	+ 300	+ 400	mV
Low differential threshold ($\Delta V_{11L} = V_{11L} - V_{23}$)		ΔV_{11L}	— 400	— 300	— 200	mV
Leakage current threshold ($V_{11} = V_{23}$ + 1 V)		I_{Q11}	—	—	0.5	μA

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

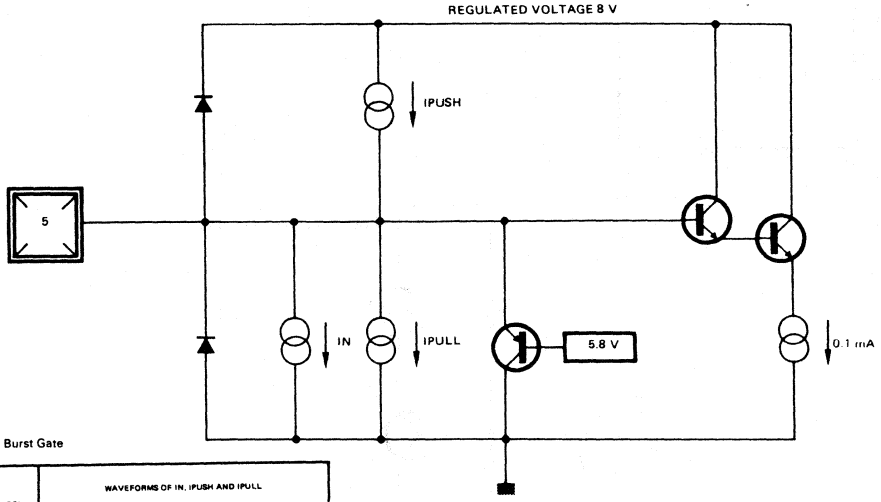
Characteristic	Symbol	Min.	Typ	Max.	Unit
De-emphasis Pins 12 - 17					
SECAM mode					
DC voltage		—	4.5	5	V
Impedance		—	11	—	kΩ
PAL-NTSC mode					
DC voltage		7.5	V_{reg}	—	V
Impedance		—	70	—	kΩ
Reference oscillator PLL					
Catching range in PAL mode		± 350	—	—	Hz
Band filter Pin 24					
Impedance SECAM mode		3.7	4.7	5.7	kΩ
PAL-NTSC mode		0.85	1.1	1.35	kΩ
Minimum switchable internal capacitance (all standards)		—	20	—	pF
Maximum switchable internal capacitance (all standards)		—	70	—	pF
Internal oscillator frequency range for:	ΔF	—	590	—	kHz
L = 10 μH					
C = 68 pF					
Frequency offset, after automatic adjustment		—	—	15	kHz
3.58 MHz switch output Pin 26					
NTSC 1 (3.58 MHz)					
DC voltage, I_{26} = 0 mA	$V_{26\ N1}$	1	—	—	V
Impedance		—	2	—	kΩ
NTSC 2 (4.43 MHz) or PAL or SECAM					
DC voltage	$V_{26\ N2}$	—	—	0.3	V
Max sink current		0.35	—	—	mA
Non-delayed signal outputs Pins 27 - 28					
DC voltage	V_{27} V_{28}	—	1.8	—	V
Sink current	I_{27} I_{28}	1	—	—	mA
Impedance		—	30	—	Ω
Identification					
BURST attenuation range					
SECAM mode (line identification)		30	—	—	dB
PAL mode		30	—	—	dB
NTSC 1 modes		30	—	—	dB

INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

- **PINS 2-3**



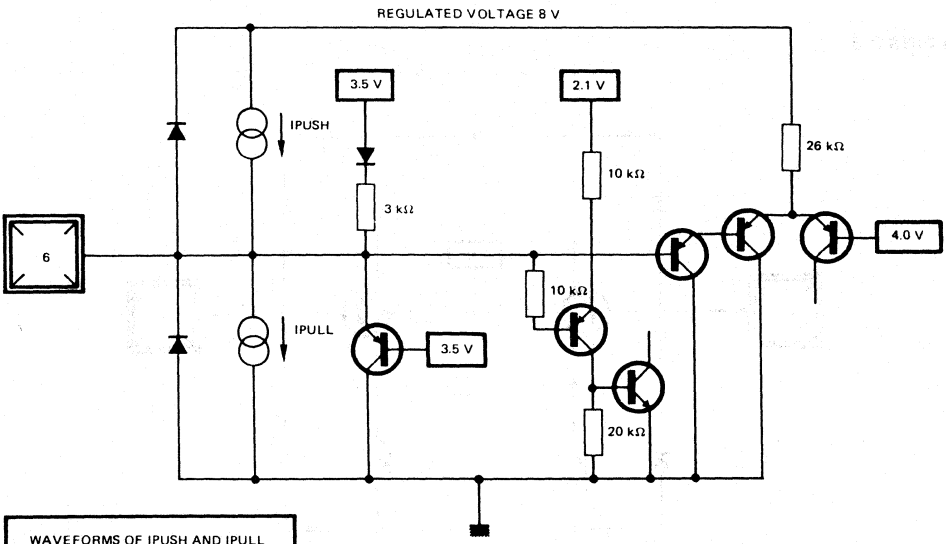
- **PIN 5**

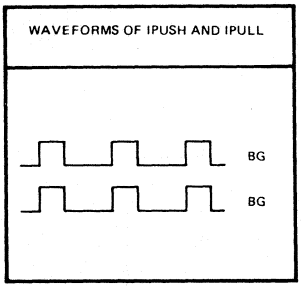


BG = Burst Gate

SYMBOL	WAVEFORMS OF IN, IPUSH AND IPULL		
	NTSC	SECAM	PAL
IN	0.14 mA	0	0
IPUSH	0	0	BG
IPULL	0	0	BG

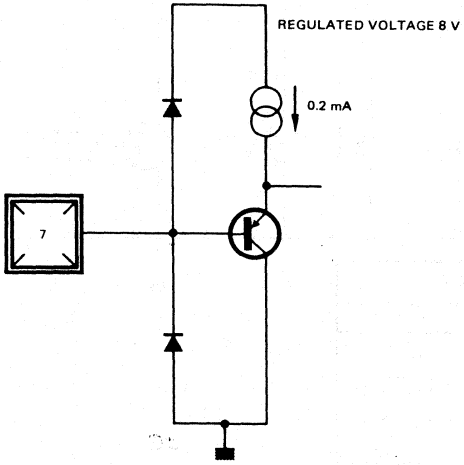
• **PIN 6**



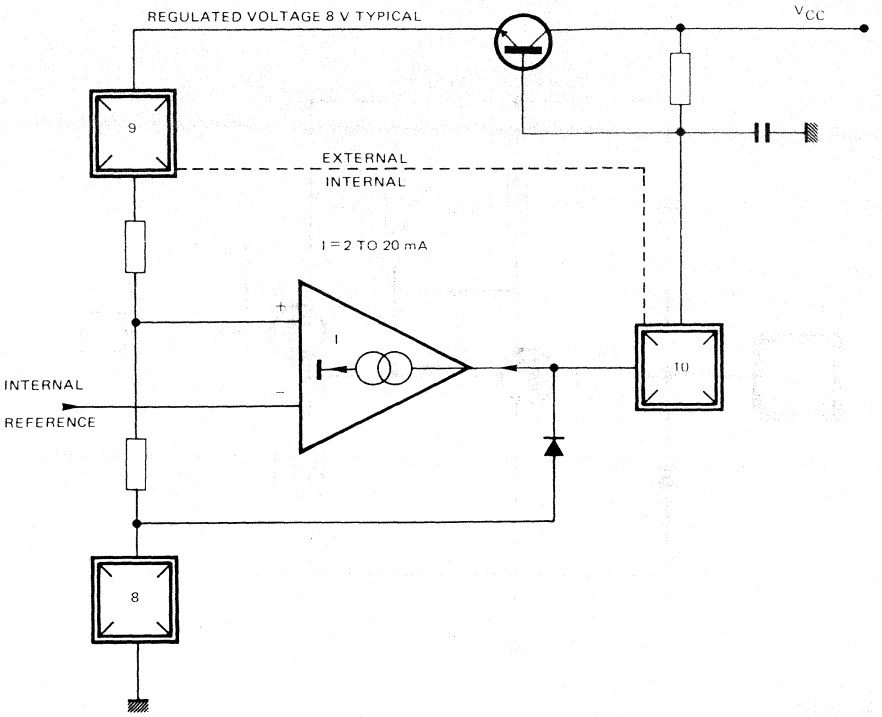


BG = BURST GATE

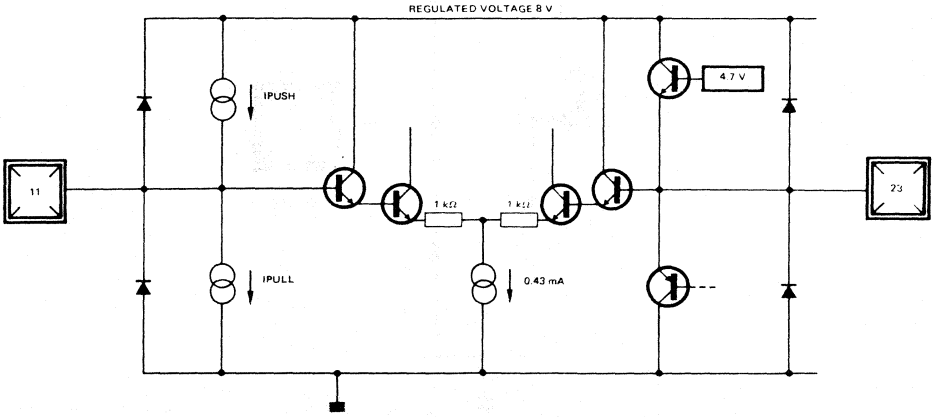
• **PIN 7**



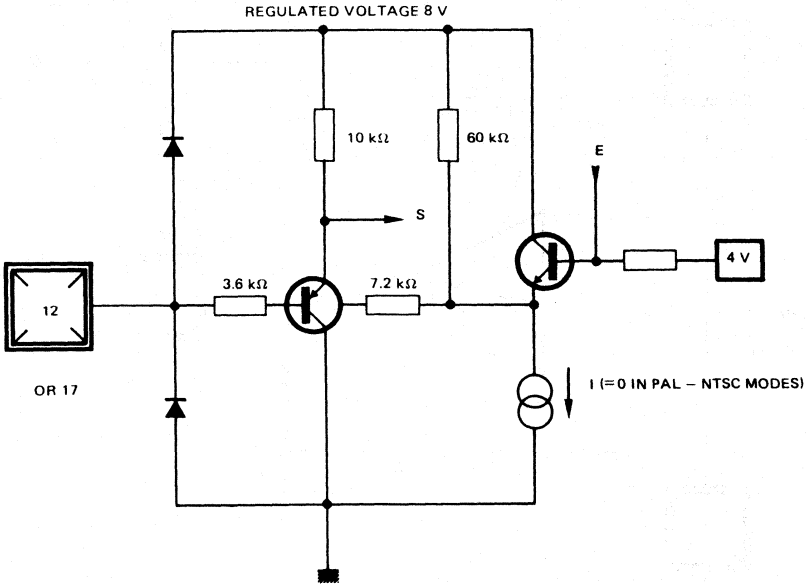
• **PINS 8-9-10**



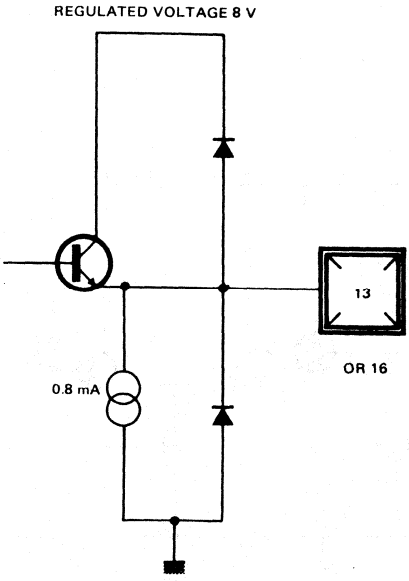
• **PINS 11-23**



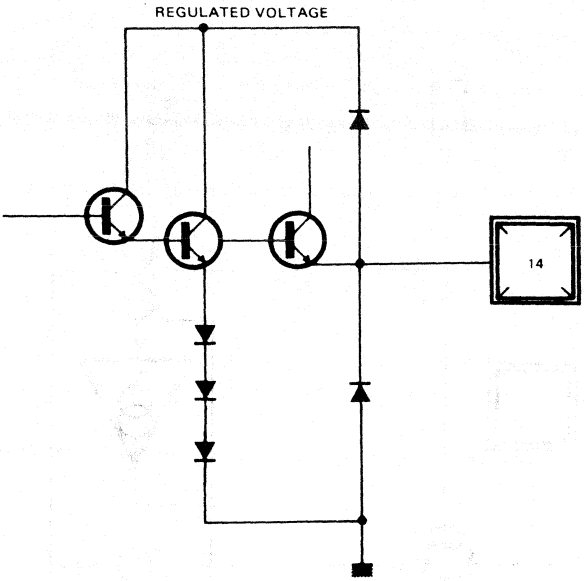
• **PINS 12-17**



• **PINS 13-16**



• PIN 14



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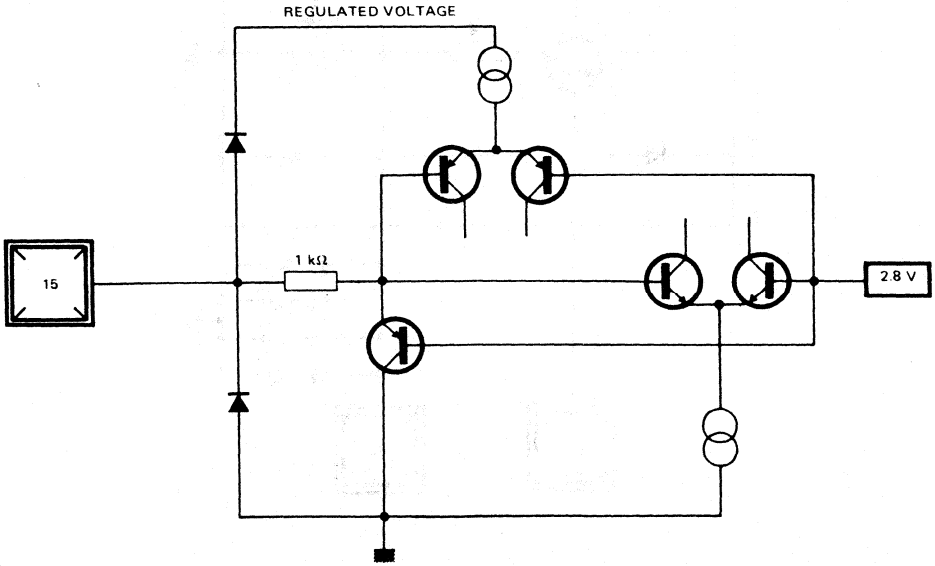
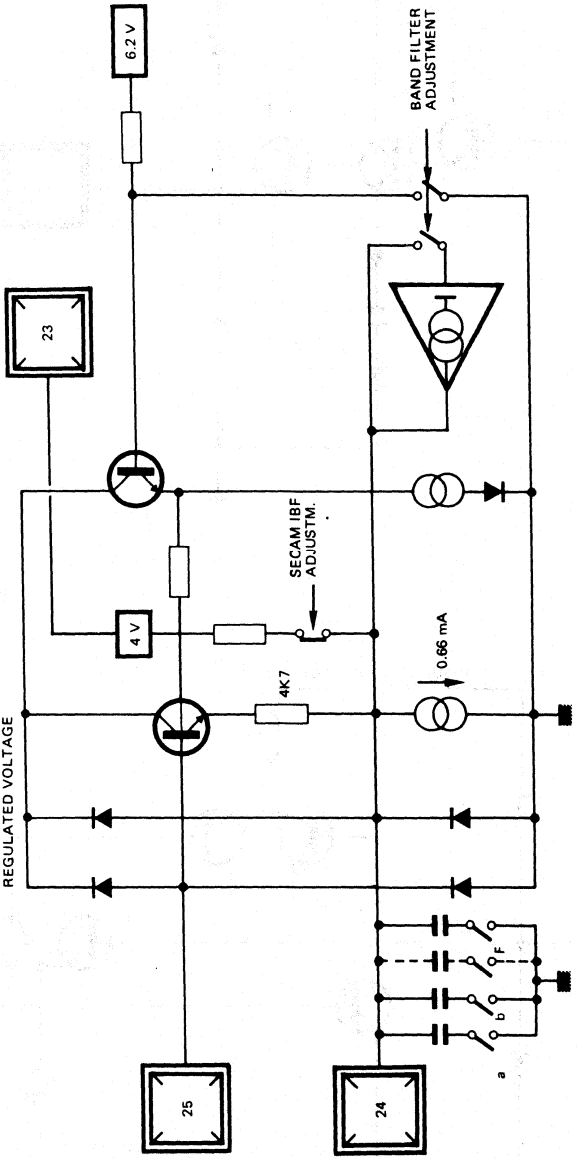
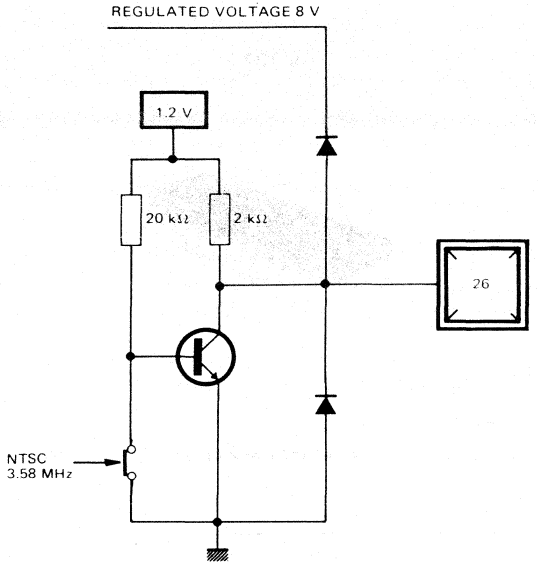


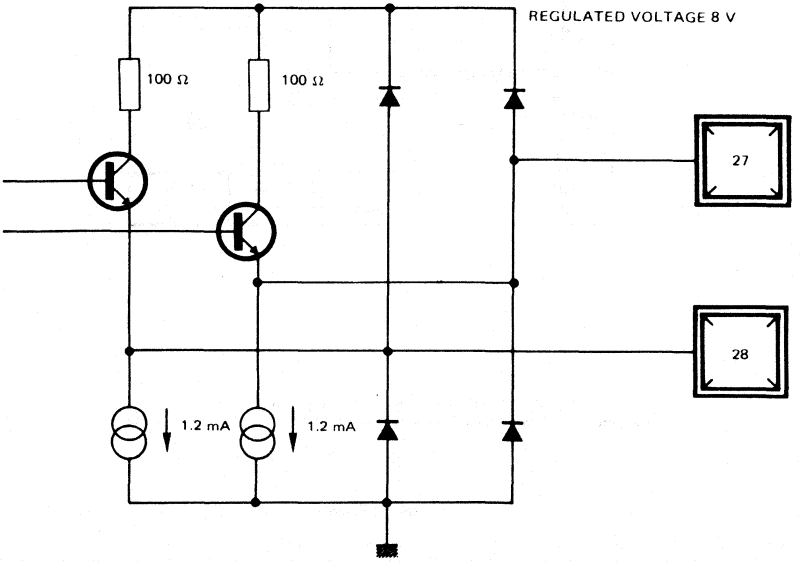
• PINS 24-25


6.2 V
BAND FILTER ADJUSTMENT
23
SECAM IBF ADJUSTM.
4 V
0.66 mA
4K7
REGULATED VOLTAGE
F
b
a
25
24

- **PIN 26**

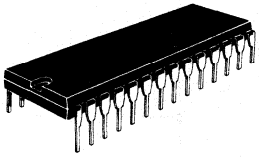


- **PINS 27-28**

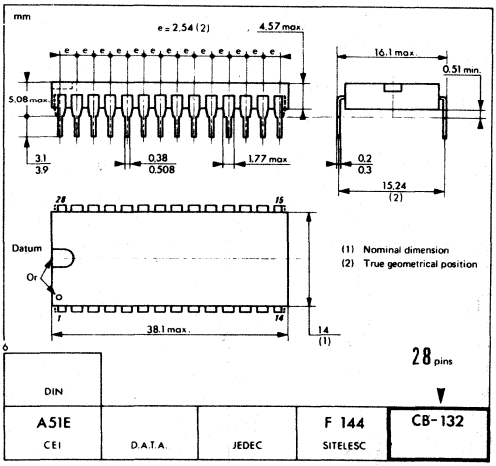


PHYSICAL DIMENSIONS

CB-132



PLASTIC PACKAGE



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Please inquire with our sales offices about the availability of the different packages.

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THOMSON COMPONENTS SEMICONDUCTEURS

TDA2540 • TDA2541

IF AMPLIFIER WITH DEMODULATOR AND AFC

The TDA 2540 and 2541 are IF amplifier and A.M. demodulator circuits for colour and black and white television receivers using PNP or NPN tuners. They are intented for reception of negative or positive modulation CCIR stantard.
They incorporate the following functions:

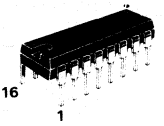
- Gain controlled amplifier
- Synchronous demodulator
- White spot inverter
- Video preamplifier with noise protection
- Switchable AFC
- AGC with noise gating
- Tuner AGC output (NPN tuner of 2540)-(PNP tuner of 2541)
- VCR switch for video output inhibition (VCR play back)

MAIN FEATURES

- Supply voltage : 12 V typ.
- Supply current : 50 mA typ.
- I.F. input voltage at f = 38.9 MHz : 100μ V_{RMS} typ.
- Video output voltage (white at 10% of top synchro) : 2.7 Vpp typ.
- I.F. voltage gain control range : 64 dB typ.
- Signal to noise ratio at V_I = 10 mV : 58 dB typ.
- A.F.C. output voltage swing for Δf = 100 kHz : 10 V typ.

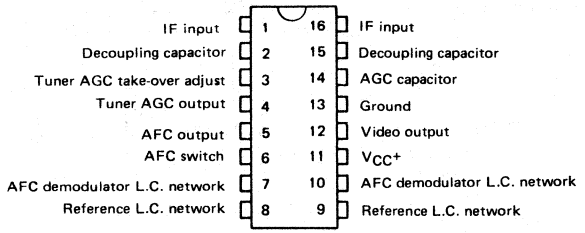
IF AMPLIFIER WITH DEMODULATOR AND AFC

Case CB-79



PLASTIC PACKAGE

PIN ASSIGNMENT



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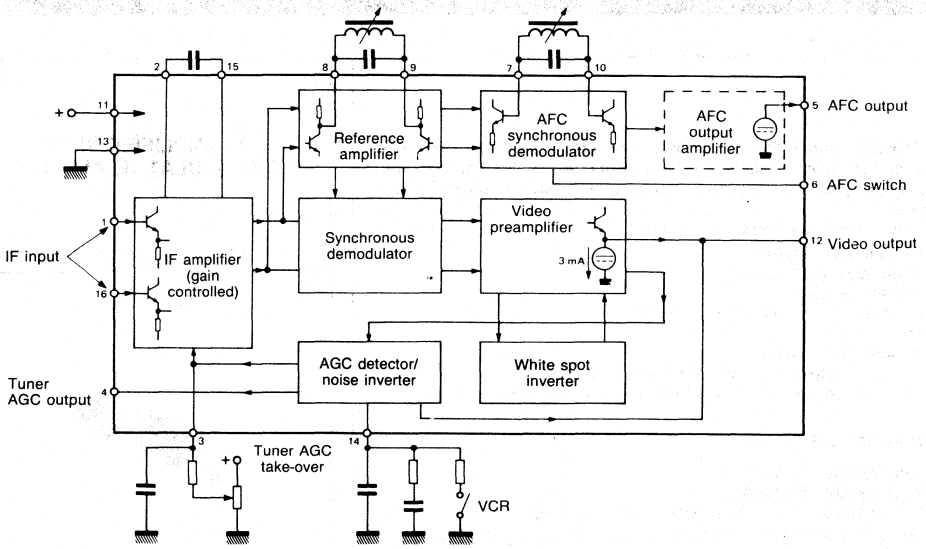
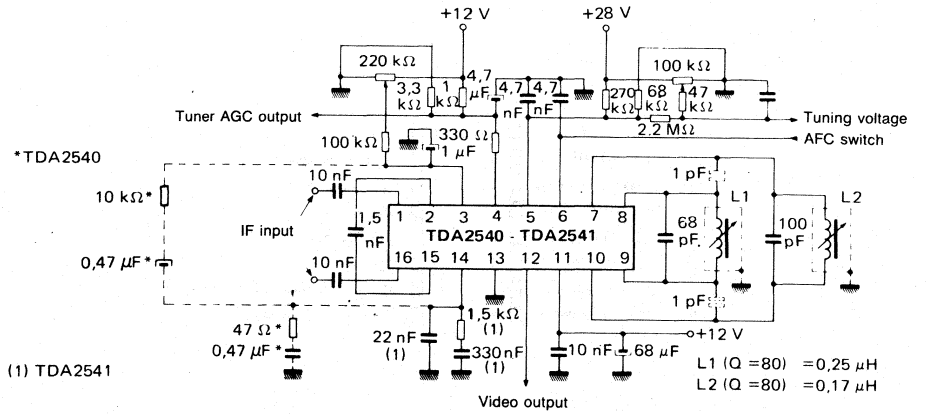
BLOCK DIAGRAM



APPLICATION CIRCUIT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V11-13	13.8	V
Tuner A.G.C voltage	V4-13	12	V
Power dissipation	P_{tot}	900	mW
Storage temperature	T_{stg}	− 55 to + 125	°C
Operating ambient temperature	T_{amb}	− 25 to + 60	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Junction-ambient thermal resistance	R_{th} (j-a)	70	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V 11-13 = 12 V ; f = 38.9 MHz (Unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max.	Unit
Supply voltage range	V11-13	10.2	12	13.8	V
Supply current	I_{11}	—	50	60	mA
IF input voltage for onset of A.G.C	V1-16RMS	60	85	180	μV
Max input voltage (pins 1-16)		—	140	—	mV
Video output voltage	V12-13	—	2.7	—	Vpp
Differential input impedance (in parallel with 2pF)	Z1-16	—	2	—	kΩ
Zero signal output level	V12-13	5.7	6	6.3	V
Top synchro output level	V12-13	2.9	3.07	3.2	V
IF voltage gain control range	ΔG_V	52	64	—	dB
Signal to noise ratio (V_I = 10 mV)(see note 1)	S/N	50	58	—	dB
Bandwidth of video amplifier (—3 dB)	B	—	6	—	MHz
Differential gain	dG	—	4	10	%
Differential phase	dΦ	—	2	10	%
Carrier signal at video output (V_I = 10 mV)	V12-13	—	4	30	mVRMS
2nd harmonic of carrier at video output (V_I = 10 mV)	V12-13	—	20	30	mVRMS
Intermodulation at 1.1 MHz (blue) (See figures 2 and 3)		46	60	—	dB
Intermodulation at 1.1 MHz (yellow) (See figures 2 and 3)		46	50	—	dB
Intermodulation at 3.3 MHz (blue) (See figures 2 and 3)		46	54	—	dB
VCR switches OFF output at : (VCR = low level)	V14-13	—	—	1.1	V
White spot inverter threshold level (see figure 1)		—	6.6	—	V
White spot insertion level (see figure 1)		—	4.7	—	V
Noise inverter threshold level (see figure 1)		—	1.8	—	V
Noise insertion level (see figure 1)		—	3.8	—	V
Tuner AGC output current range	I4	—	0 to 10	—	mA
Tuner AGC output voltage	V4—13	—	—	0.3	V
Tuner AGC output leakage current TDA2541 V14-13 = 11 V V4-13 = 12 V TDA2540 V14-13 = 5 V V4-13 = 12 V	I4	—	—	15	μA
AFC output voltage swing (Δf = 100 kHz)	ΔV_{5-13}	10	11	—	V
Change of frequency at AFC output (voltage swing of 10 V)	Δf	—	100	200	kHz
AFC switches OFF (AFC = low level) at:	V6-13	—	—	2.5	V
AFC switches ON (AFC = high level) at:	V6-13	3.2	—	—	V
AFC zero = signal output voltage (minimum gain)	V5-13	4	6	8	V

$$\text{Note 1: } S/N = \frac{V_O \text{ (black to white)}}{V_N \text{ (RMS at B = 5 MHz)}} \text{ (dB)}$$

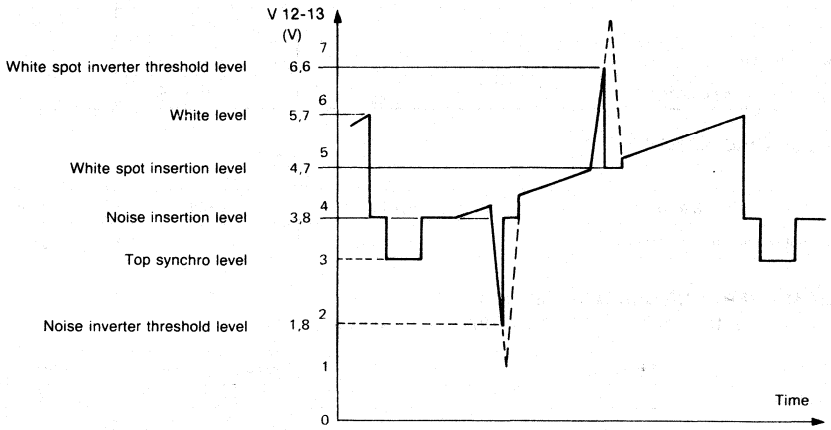


Fig. 1 — VIDEO OUTPUT WAVEFORM SHOWING WHITE SPOT AND NOISE INVERTER THRESHOLD LEVELS

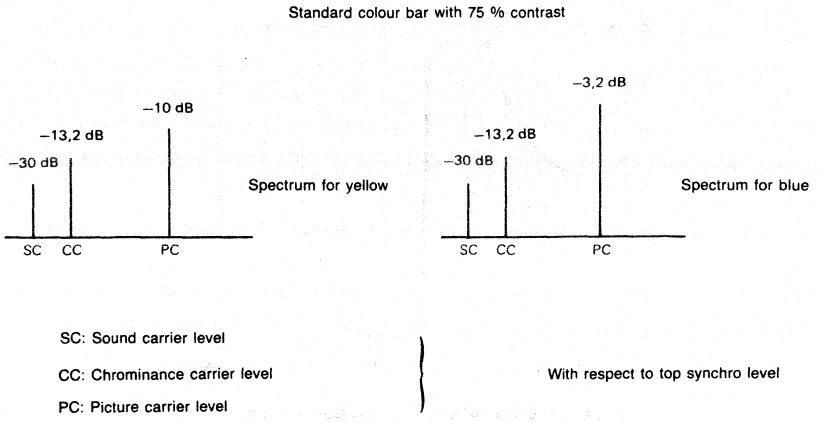
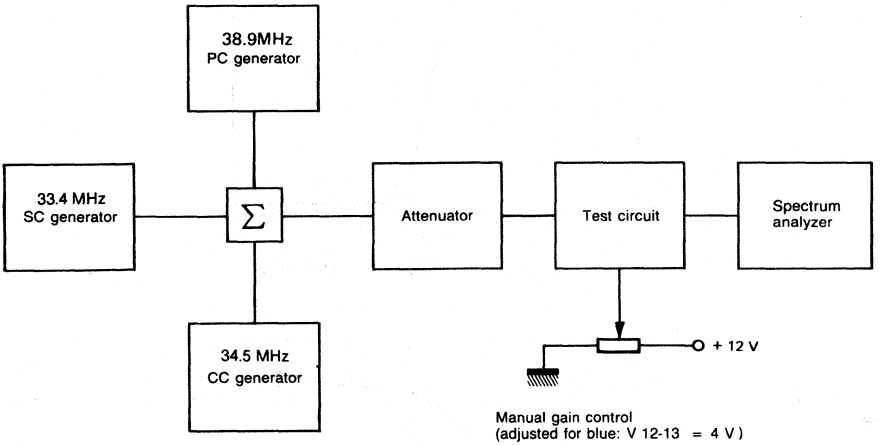


Fig. 2 — INPUT CONDITIONS FOR INTERMODULATION MEASUREMENTS



$$\text{Intermodulation 1.1 MHz} = 20 \log \left(\frac{V_O \text{ at 4.4 MHz}}{V_O \text{ at 1.1 MHz}} \right) + 3.6 \text{ dB}$$

$$\text{Intermodulation 3.3 MHz} = 20 \log \left(\frac{V_O \text{ at 4.4 MHz}}{V_O \text{ at 3.3 MHz}} \right)$$

Fig. 3 — TEST SET-UP FOR INTERMODULATION

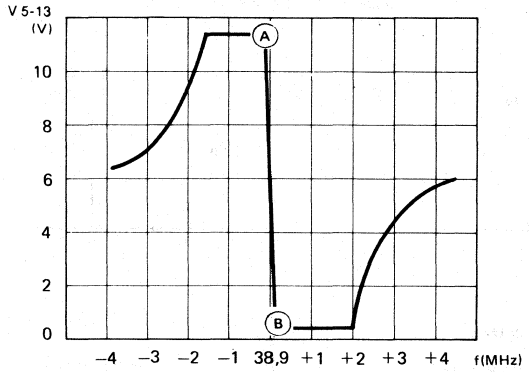


Fig. 4 — AFC VOLTAGE VERSUS FREQUENCY V 5-13

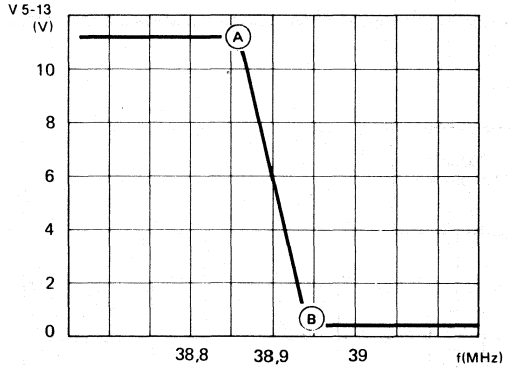


Fig. 5 — AFC VOLTAGE VERSUS FREQUENCY V 5-13

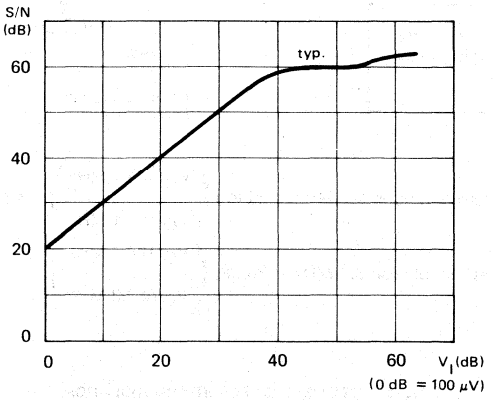
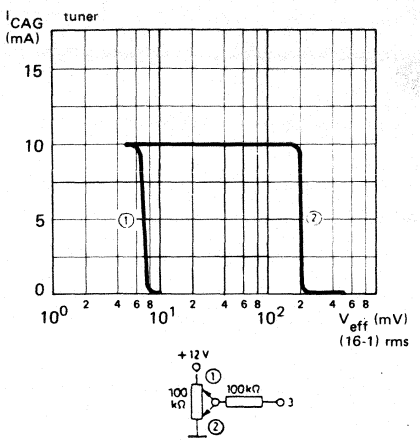
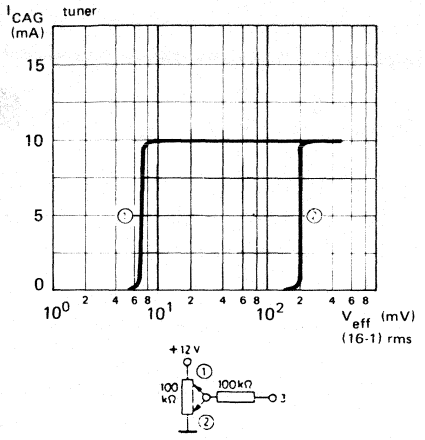


Fig. 6 — SIGNAL/NOISE RATIO VERSUS INPUT VOLTAGE V 1-16

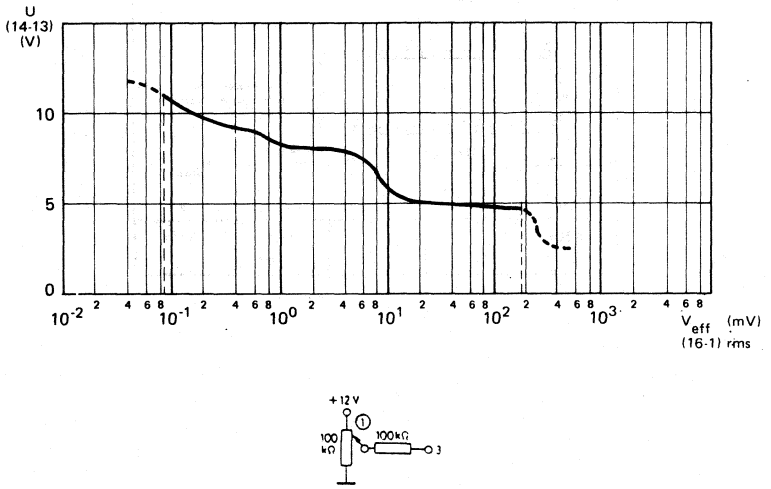
TDA 2540



TDA 2541

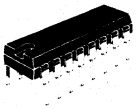


TDA 2540 – TDA 2541

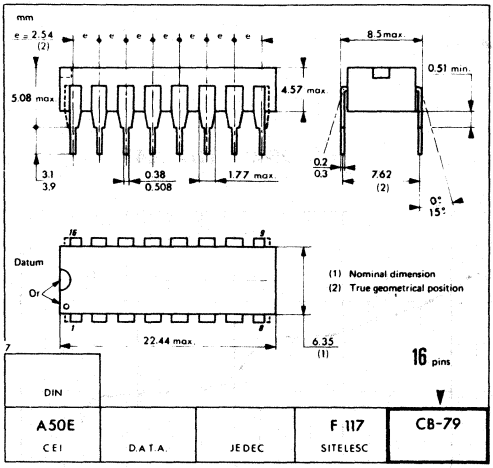


PHYSICAL DIMENSIONS

CASE CB-79



PLASTIC PACKAGE



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THOMSON COMPONENTS SEMICONDUCTEURS

TDA2542

IF AMPLIFIER WITH DEMODULATOR AND AFC FOR POSITIVE MODULATION STANDARD

The TDA 2542 is an IF amplifier and AM demodulator circuit for colour and black and white television receivers using PNP tuners. It is intended to reception positive modulation for french standard.
It incorporates the following functions

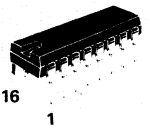
- Gain controlled amplifier
- Synchronous demodulator
- Video preamplifier
- Switchable AFC
- AGC
- Tuner AGC output (PNP tuner)

Main features

- Supply voltage : 12 V typ.
- Supply current : 50 mA typ.
- IF input voltage at f = 32.7 MHz : 100 μV_{RMS} typ.
- Video output voltage : 3 Vpp typ.
- IF voltage gain control range : 64 dB typ.
- Signal to noise ratio at V_I = 10 mV : 58 dB typ.
- A.F.C. output voltage swing for Δf = 100 kHz : 10 V typ.

IF AMPLIFIER WITH DEMODULATOR AND AFC FOR POSITIVE MODULATION STANDARD

CASE CB-79



PLASTIC PACKAGE

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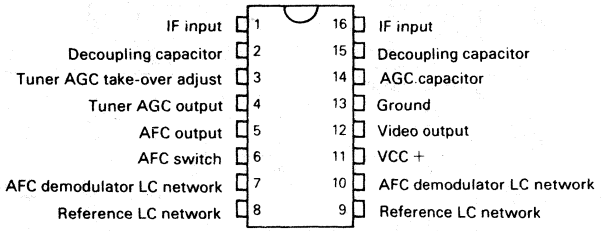

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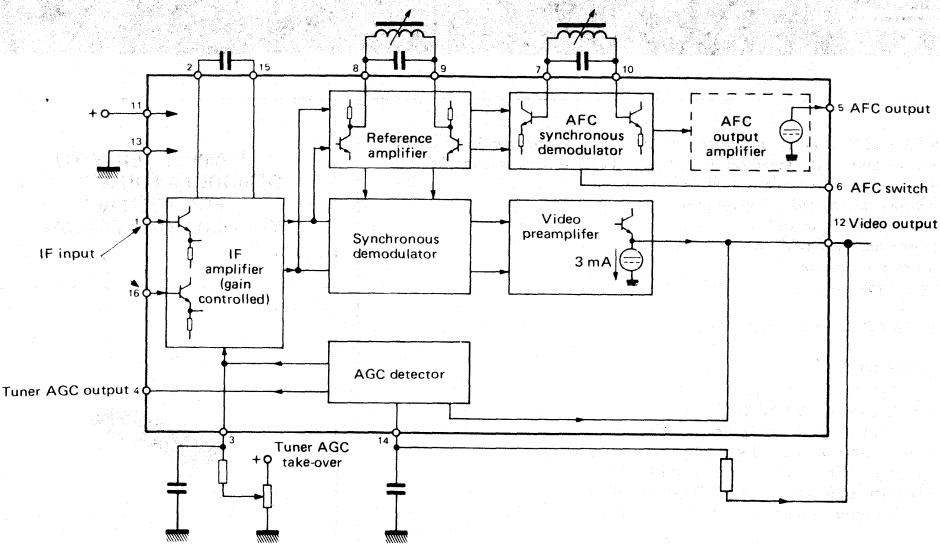
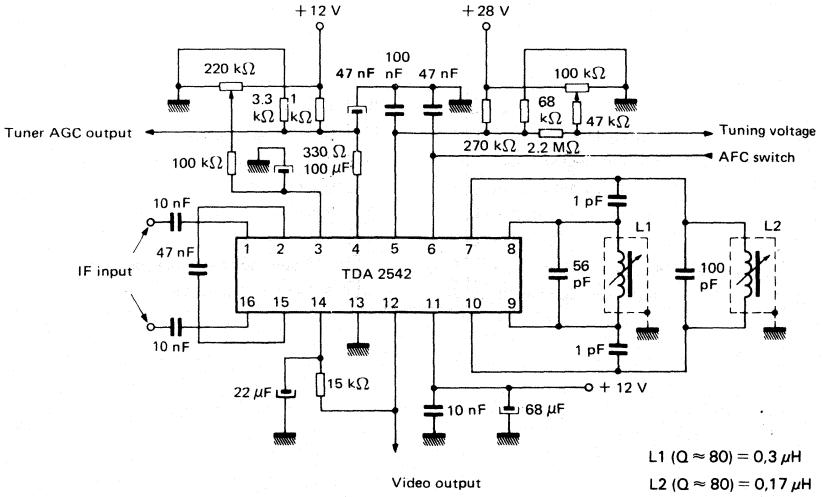
BLOCK DIAGRAM



APPLICATION CIRCUIT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V 11-13	13.8	V
Tuner A.G.C voltage	V 4-13	12	V
Power dissipation	P_{tot}	900	mW
Storage temperature	T_{stg}	- 55 to + 125	°C
Operating ambient temperature	T_{amb}	- 25 to + 60	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th}(j\text{-}a)$	70	°C/W

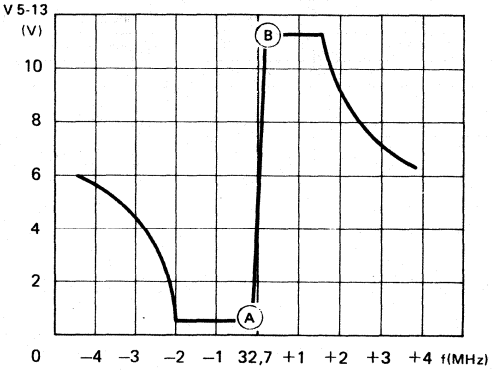
ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25°C$; V 11-13 = 12 V ; f = 32.7 MHz (unless otherwise specified)

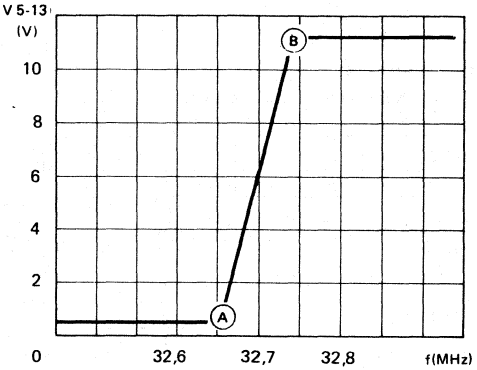
characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage range	V 11-13	10.2	12	13.8	V
Supply current	I 11	40	50	58	mA
IF input voltage for onset of A.G.C	V 1-16	–	85	160	μV RMS
Max input voltage (pins 1-16)	–	–	140	–	mV
Video output voltage	V 12-13	–	3	–	V_{pp}
Differential input impedance (in parallel with 2pF)	Z 1-16	–	2	–	kΩ
Zero signal output level	V 12-13	–	2.9	–	V
IF voltage gain control range	ΔG_V	–	64	–	dB
Signal to noise ratio (1) (V_I = 10 mV)	S/N	–	58	–	dB
Bandwidth of video amplifier (-3 dB)	B	–	6	–	MHz
Differential gain	dG	–	4	10	%
Differential phase	dΦ	–	2	10	%
Carrier signal at video output	V12-13	–	4	30	mVRMS
2nd harmonic of carrier at video output	V12-13	–	20	30	mVRMS
Reference voltage of AGC detector	V 14	–	3.9	–	V
Tuner AGC output current range	I 4		0 → 10		mA
Tuner AGC output voltage (I 4 = 10 mA)	V 4-13	–	–	0.3	V
Tuner AGC output leakage current (V 14-13 = 11 V ; V 4-13 = 12 V)	I 4	–	–	15	μA
AFC output voltage swing (Δf = 100 KHz)	V 5-13	10	11	–	V
Change of frequency at AFC output (voltage swing of 10 V)	Δf	–	100	200	kHz
AFC switches ON (AFC = high level) at:	V 6-13	3.2			V
AFC switches OFF (AFC = low level) at:	V 6-13			1.5	V

$$(1)\ S/N = \frac{V_O \text{ (black to white)}}{V_n \text{ (RMS at B = 5 MHz)}} \text{ (dB)}$$

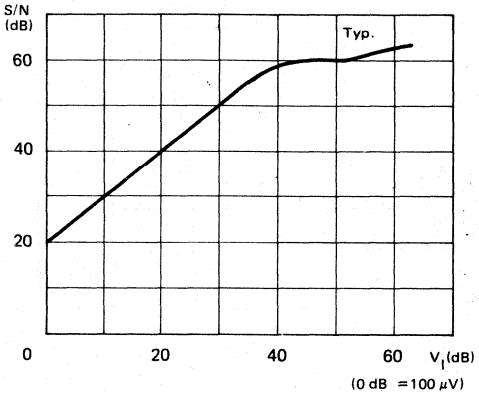
AFC VOLTAGE VERSUS FREQUENCY V 5-13

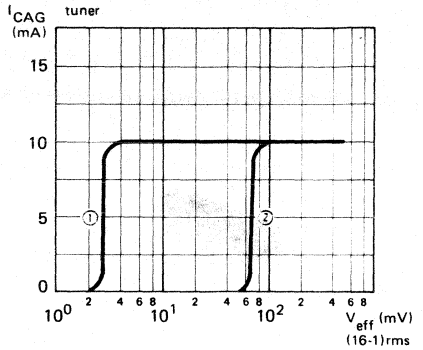


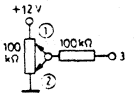
AFC VOLTAGE VERSUS FREQUENCY V 5-13



SIGNAL/NOISE RATIO VERSUS INPUT VOLTAGE V 1-16

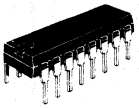



I_{CAG} (mA)
tuner
15
10
5
0
1
2
10^0
10^1
10^2
2 4 6 8
V_{eff} (mV)
(16-1)rms

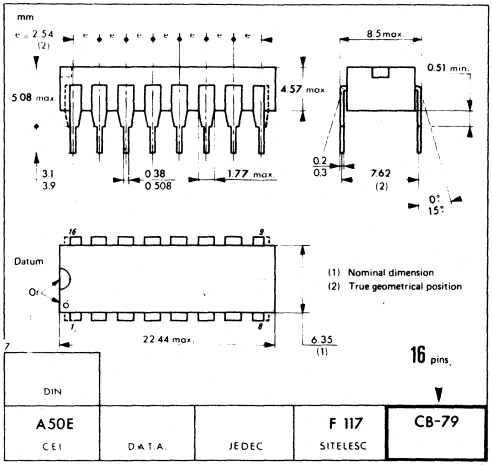

+12 V
1
100 kΩ
100 kΩ
3
2

PHYSICAL DIMENSIONS

CASE CB-79



PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

TDA4426 • TDA4427

VIDEO IF AMPLIFIER WITH DEMODULATOR AND AFC

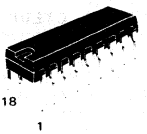
The TDA4426 and TDA4427 are IF amplifier and A.M. demodulator circuits for colour or black and white television receiver using PNP tuner. They are intended for reception of negative or positive modulation CCIR standards.

They have the following features :

- Synchronous demodulators
- Gain controlled amplifier
- Very high input sensitivity
- Constant input impedance independent of AGC
- Fixed video output voltage with small tolerance range
- Switchable AFC
- Positive or negative AGC gating pulse
- Very few external components
- Output video signal no much affected by supply voltage variations
- The TDA4426 and TDA4427 get different AFC curves (inverted AFC for TDA4427)

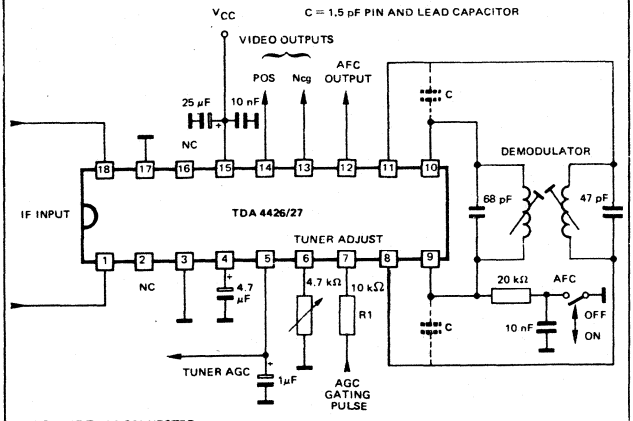
VIDEO IF AMPLIFIER WITH DEMODULATOR AND AFC

CASE CB-225



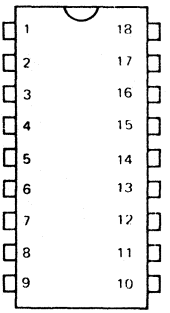
PLASTIC PACKAGE

APPLICATION CIRCUIT



NC : NOT TO BE CONNECTED

PIN ASSIGNMENT



1 - IF input
2 - Not to be connected
3 - Ground
4 - AGC filter capacitor
5 - Tuner AGC output
6 - Tuner AGC adjustment
7 - Pulse input for AGC gated
8 - Carrier tuned circuit output 1
9 - AFC tuned circuit output 1
10 - AFC tuned circuit output 2
11 - Carrier tuned circuit output 2
12 - AFC output
13 - Negative video output
14 - Positive video output
15 - Supply voltage
16 - Not to be connected
17 - Ground
18 - IF input

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MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply voltage		V_{CC}	15	V
Voltage at pin 5		V_5	V_{CC}	V
Voltage at pin 4		V_4	5	V
Output current to ground (Source current) max : 1 s	Pins 13, 14.	$I_{13} \cdot I_{14}$	30	mA
Output current from positive supply (sink current) max : 1 s	Pins 13, 14.	$I_{13} \cdot I_{14}$	5	mA
Junction temperature		T_j	125	°C
Operating ambient temperature		T_{amb}	0 to + 70	°C
Storage temperature		T_{stg}	– 25 to + 125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction - ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

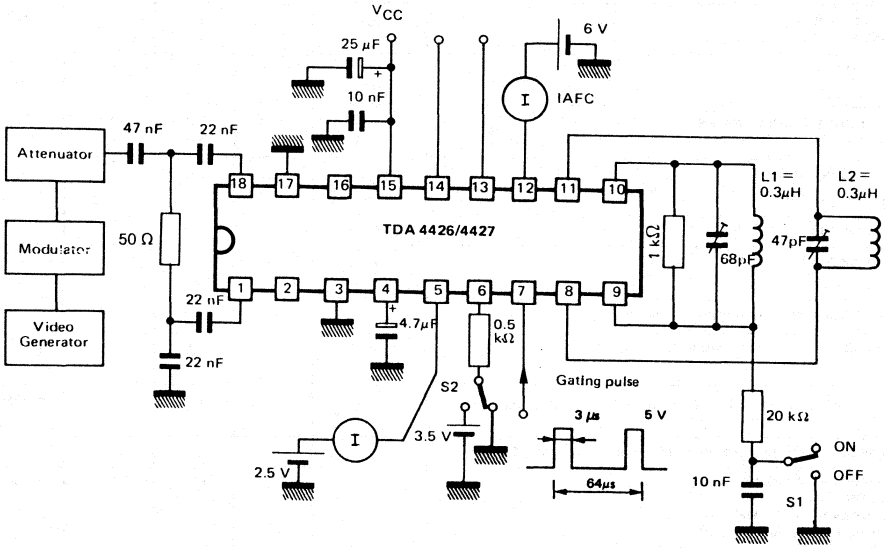
ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25°C V_{CC} = 12 V F = 38.9 MHz m = 80 % (unless otherwise specified)

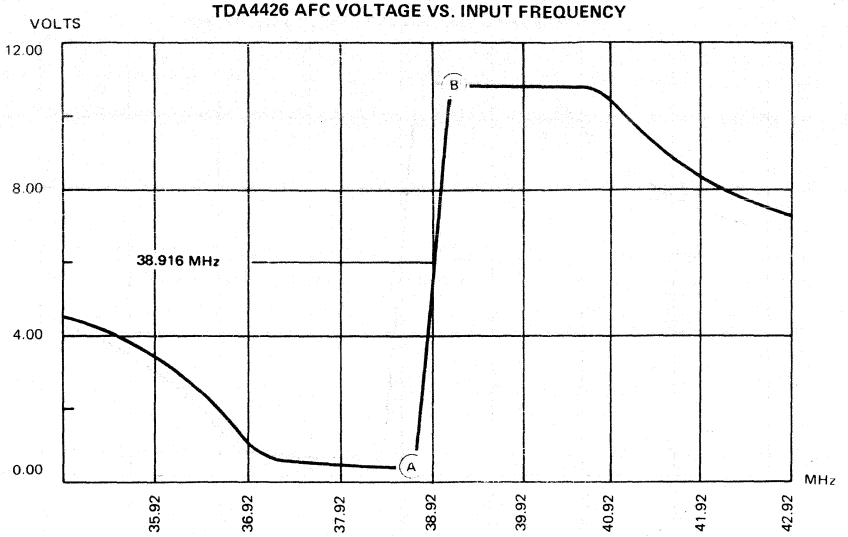
Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	10	12	15	V
Supply current V_4 = 3.5 V	I_{CC}	35	–	70	mA
Ultra white level	V_{13} V_{14}	4.7 –	5.2 1.8	5.8 –	V V
Top synchro DC output voltage	V_{13} V_{14}	1.75 –	1.9 5.0	2.05 –	V V
Output DC current (V_{13} = V_{14} = 7 V)	I_{13} - I_{14}	–	1.5	–	mA
AGC pulse input DC voltage	V_7	–	1.1	–	V
Input impedance	R_{1-18} C_{1-18}	– –	1.6 2	– –	kΩ pF
Input voltage sensitivity (output voltage 3 V_{pp})		–	100	150	µV
IF residual carrier at video output (F = 38.9 MHz) Pins 13 - 14	V_{13} - V_{14}	–	20	–	mVRMS
2nd harmonic carrier at video output (F = 77.8 MHz) Pins 13 - 14	V_{13} - V_{14}	–	40	–	mVRMS
Differential distorsion on composite video amplitude (pin 13, 14)		–	3	5	%
INTERMODULATION AT (input condition) Color subcarrier (1.07 MHz) PC : Picture carrier level = 0 dB CC : Color subcarrier level = – 6dB SC : Sound carrier level = – 24 dB		–	50	–	dB
Composite video output level	V_{13}	2.7	3.0	3.3	Vpp
V_I = 30 mV m = 80 % without load	V_{14}	2.7	3.0	3.3	Vpp
Ultra black level variation with supply voltage (V_{CC})	$\Delta V_{13}/\Delta V_{CC}$ / or $\Delta V_{14}/\Delta V_{CC}$	–	0.5	–	%
Ultra white level variation with supply voltage (V_{CC})	$\Delta V_{13}/\Delta V_{CC}$ or $\Delta V_{14}/\Delta V_{CC}$	–	3	–	%
Video bandwidth (– 3 dB) Pins 13- 14	BW	–	6	–	MHz
AGC range		55	60	–	dB
Available tuner control output current (Input level 10 dB higher than level threshold)	I_{AGCT}	7	10	–	mA
AGC tuner range		–	60	–	dB
Tuner AGC output leakage current (V_5/3 = 12 V)	I_5	–	–	20	µA
AFC tank pin DC voltage Pins 9 - 10	V_9 - V_{10}	–	3	–	V
AFC output voltage range (Δf = 200 kHz) Pin 12	V_{AFC}	– 1.0	–	V_{CC} – 1.5	V
AFC output current Pin 12	$\pm I_{AFC}$	–	1.2	–	mA
AFC slope	$\pm \frac{\Delta I_{AFC}}{\Delta f}$	–	0.2	–	mA/ 100 kHz
AFC output current (AFC switch off) Pin 12		–	–	60	µA
Switching current for AFC Pins 9 - 10		100	150	–	µA

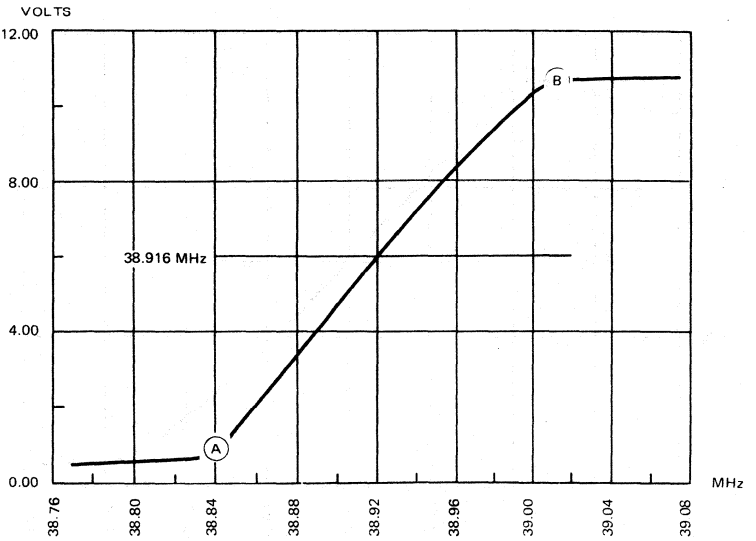
TEST CIRCUIT

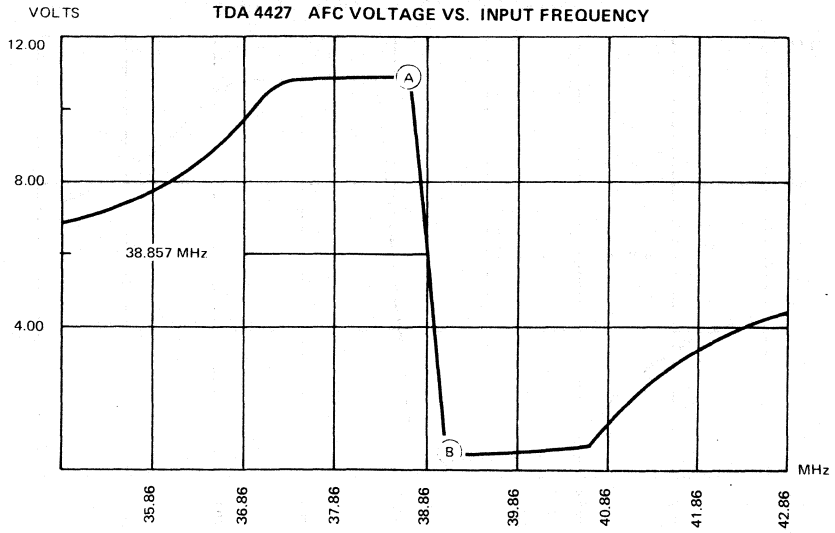
Q_{min} = 70 at I.F.

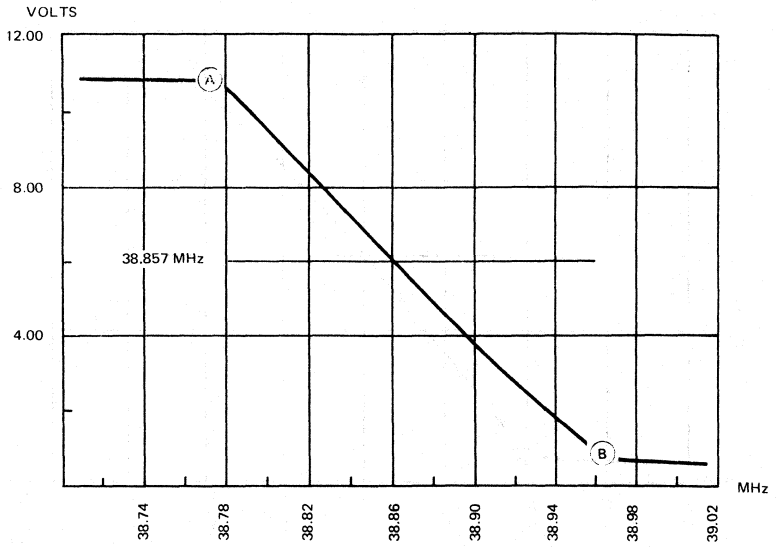


TDA4426 AFC VOLTAGE VS. INPUT FREQUENCY



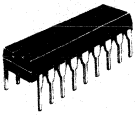



VOLTS
TDA 4427 AFC VOLTAGE VS. INPUT FREQUENCY
12.00
8.00
4.00
38.857 MHz
A
B
MHz
35.86
36.86
37.86
38.86
39.86
40.86
41.86
42.86

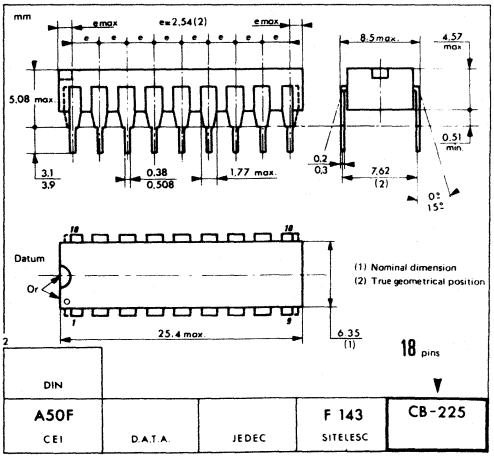

VOLTS
12.00
8.00
4.00
38.857 MHz
A
B
MHz
38.74
38.78
38.82
38.86
38.90
38.94
38.98
39.02

PHYSICAL DIMENSIONS

CB-225



PLASTIC PACKAGE



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NOTES

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THOMSON COMPONENTS SEMICONDUCTEURS

TDA4443

VIDEO IF AMPLIFIER FOR MULTISTANDARD APPLIANCES

ADVANCE INFORMATION

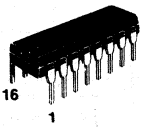
Video IF amplifier with standard switch for multistandard colour or monochrome TV sets, and VTR's.

Main features

- Switching off the IF amp. when operating in VTR mode via DIN plug
- Demodulation of negative or positive IF signals. The output remains on the same polarity in every case
- IF AGC automatically adjusts to the actual standard
- Two AGC possibilities for B/G mode :
  1. Gated AGC
  2. Ungated AGC on sync. level and controlled discharge dependent on the average signal level for VTR and Peri TV applications
- For standard L/E: Fast AGC on peak white by controlled discharge
- Positive or negative gating pulse
- Extremely high input sensitivity
- Low differential distortion
- Constant input impedance
- Very high supply voltage rejection
- Few external components
- Low impedance video output
- Small tolerances of the fixed video signal amplitude
- Adjustable, delayed AGC for PNP tuners
- Pin compatible with the IF IC's TDA4426 and TDA4427

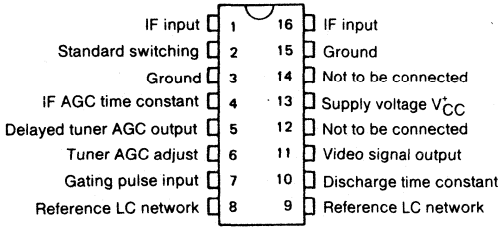
VIDEO IF AMPLIFIER FOR MULTISTANDARD APPLIANCES

CASE CB-79



PLASTIC PACKAGE

PIN ASSIGNMENT



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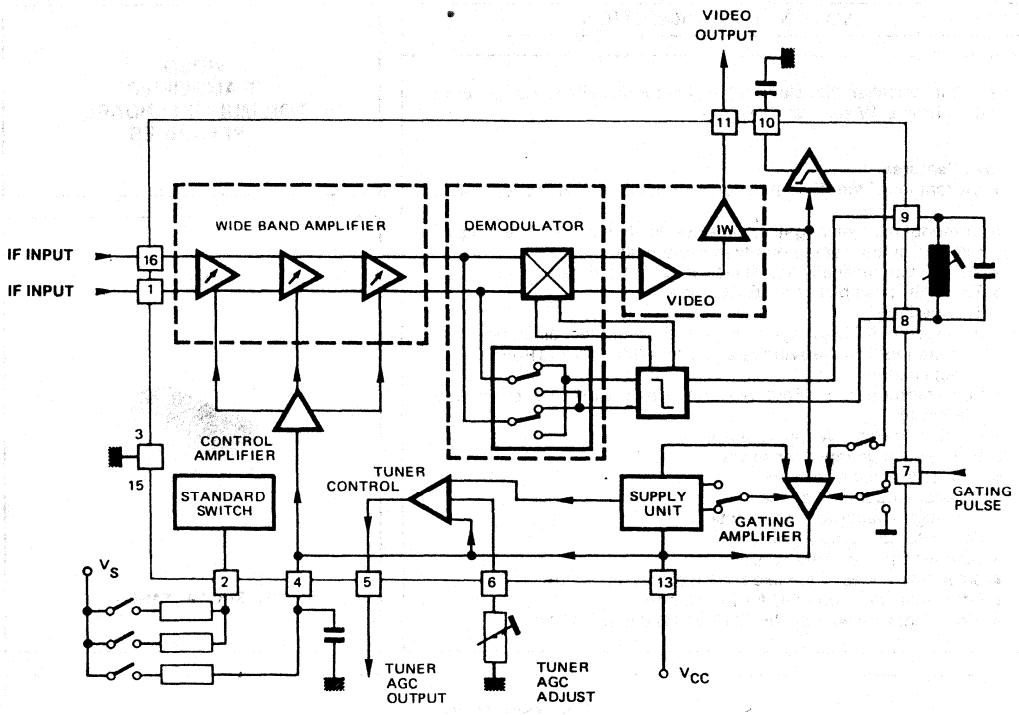
BLOCK DIAGRAM



GENERAL DESCRIPTION

This video IF processing circuit integrates the following functionnal blocks;

- Three symmetrical, very stable, gain controlled wideband amplifier stages — without feedback by a quasi-galvanic coupling
- Demodulator controlled by the picture carrier
- Video output amplifier with high supply voltage rejection
- Polarity switch for the video output signal
- AGC on peak white level
- Gated AGC
- Discharge control
- Delayed Tuner AGC
- At VTR reading mode the video output signal is at ultra white level

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply voltage range	Pin 13	V_{CC}	15	V
Supply current	Pin 13	I_{CC}	60	mA
Open loop voltage	Pin 5	V_0	max. V_{CC}	V
External voltage	Pin 4	V_{ext}	12	V
Control current for VTR mode	Pin 4	I_4	0.3	mA
Control current for standard mode	Pin 2	I_2	0.5	mA
Max. video output current	Pin 11	I_0	5	mA
Short circuit current ($t \leqslant 1$ sec)	Pin 11	I_0	30	mA
Power dissipation		P_{tot}	1	W
Junction temperature		T_j	125	°C
Ambient temperature range		t_{amb}	−25 to + 70	°C
Storage temperature range		t_{stg}	−25 to + 125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	R_{th} (j-a)	70	°C/W

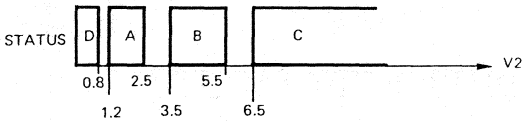
ELECTRICAL OPERATING CHARACTERISTICS

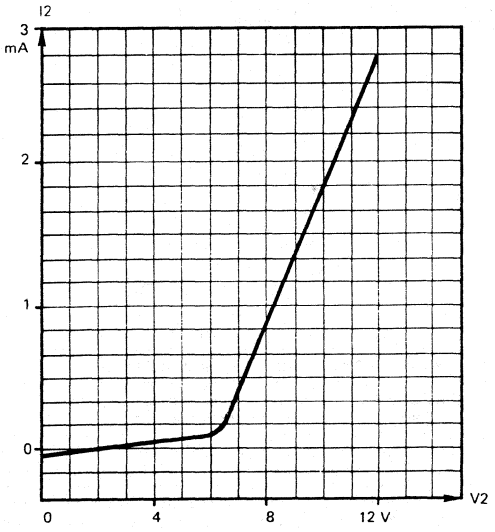
T_{amb} = 25°C, V_{CC} = 12 V, unless otherwise specified.
Test circuits page 6.

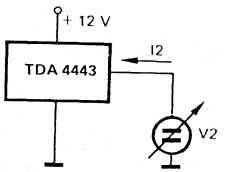
Characteristic		Symbol	Min	Typ	Max.	Unit
Supply voltage	Pin 13	V_{CC}	10	12	15	V
Supply current	Pin 13	I_{CC}	—	50	—	mA
Ultra white level at standard B/G	Pin 11	V_{11}	4.8	5.2	5.6	V
Ultra black clamping level at standard B/G	Pin 11	V_{11}	1.75	1.9	2.05	V
Picture to sync. output voltage of the video signal without load in standard B/G (residual carrier 10 %)	Pin 11	V_0	2.7	3.0	3.3	V_{pp}
Picture to blanking level output voltage of the video signal without load in standard L (blanking level at 27 % of carrier amplitude)	Pin 11	V_0	1.85	2.1	2.35	V_{pp}
Output voltage change of the picture to blanking level from standard L to standard B/G	Pin 11	$\frac{\Delta(V_p - V_{blank})}{V_p - V_{blank}}$	—	—	10	%
Supply voltage influence on the ultra black level in standard B/G	Pin 11	ΔV black	—	0.5	—	%/V
Supply voltage influence on the ultra white level in standard B/G	Pin 11	ΔV white	—	0.5	—	%/V
Video bandwidth (—3 dB)	Pin 11	B_{video}	6	—	—	MHz
Video frequency response changes within the AGC range	Pin 11	ΔV_{video}	—	—	2.0	dB
DC output current V_{11} = 10 V	Pin 11	I_0	—	1.5	—	mA
Gating pulse current	Pin 7	I_1	0.35	—	1.0	mA
DC voltage at gating input	Pin 7	V_1	—	1.1	—	V
Input voltage sensitivity (symmetrical) for V_{11} = 3.0 V_{pp}, 10 % residual carrier V4 = 0.8 V (Sync. peak level at standard B/G)	Pin 1-16	V_1	—	120	—	μV_{RMS}
Control current for status B (see status of mode switching)	Pin 2	I	20	—	40	μA
Control current for status C (see status of mode switching)	Pin 2	I	—	—	400	μA
IF AGC range		ΔG_{IF}	—	60	—	dB
Available tuner AGC current 10 dB above the AGC starting point	Pin 5	I_{AGC}	8	10	—	mA
Delay between tuner AGC and IF AGC, pin 6 not connected	Pin 5	Δ_{AGC}	—	50	—	dB
IFF residual carrier at the video o/p withing the AGC range 38.9 MHz 77.8 MHz	Pin 11 Pin 11	V_{IF} V_{2IF}	— —	20 50	— —	mV_{RMS} mV_{RMS}
Differential distortion on composite video signal amplitude	Pin 11	d	—	—	3	%
Attenuation of sound to color carrier intermodulation signal (1.07 MHz) referred to the demodulated color carrier Picture carrier = 0 dB Color carrier = — 6 dB Sound carrier = — 24 dB	Pin 11	a_{IM}	—	50	—	dB
Sync. pulse compression within the IFF AGC range		$\frac{\Delta Sync}{Sync}$	—	3	—	%
Input impedance: Resistance Capacitance	Pin 1-16 Pin 1-16	R_i C_i	— —	1.6 2	— —	KΩ pF
Switch off control voltage for VTR mode	Pin 4	V	8	—	10	V
Switch off current for VTR mode	Pin 4	I	50	—	150	μA

Status of mode switching, referring to control voltage Pin 2.

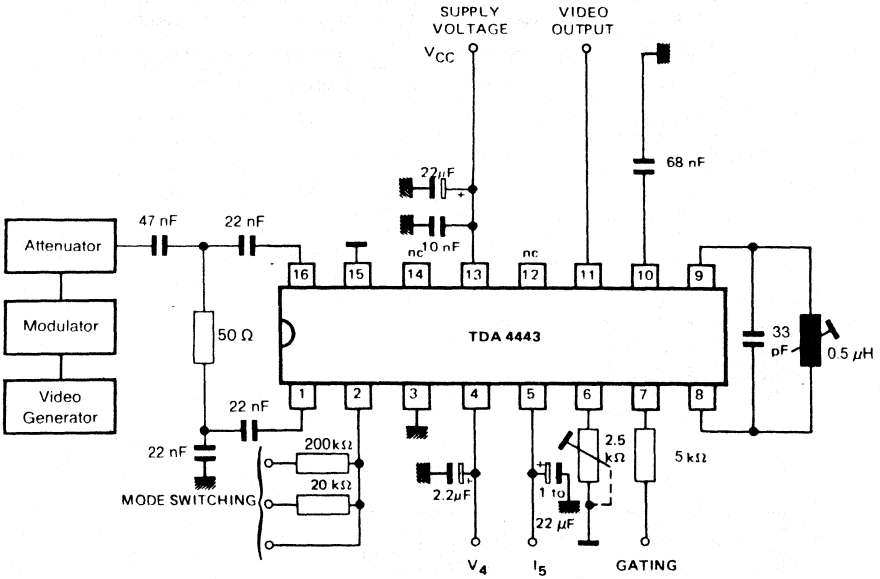
Control voltage Pin 2	Connections of Pin 2	Status	Function
1.2 to 2.2 V	open	A	Standard B/G gated sync. operation
3.0 to 5.0 V	High impedance	B	Standard B/G, no sync. operation
> 6.2 V	Low impedance	C	Standard L
0.0 to 0.8 V	Ground	D	Standard L







TEST CIRCUIT



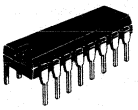
Definition of mode switching:

Status	Pin 2	Pin 4	Function
A	not connected	no external voltage	Standard B/G mode, gated charge and discharge
B	12 V high impedance	no external voltage	Standard B/G, ungated, charging up to sync. level, discharging dependant from average signal (Peri operation)
C	12 V low impedance	no external voltage	At standard L/E ungated, charging up to peak white level, discharge dependant from average signal level, inverted polarity of the video output
D	no specifications	$\geqslant$ 7.5 V	In VTR reading mode the IF amplifier is blocked, turned gain controlled down: The video output signal is fixed at constant ultra white level for standard B/G mode

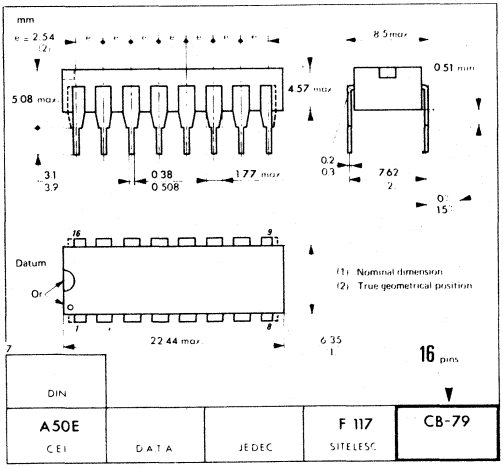
The gating pulse at Pin 7 is internally switched off.

PHYSICAL DIMENSIONS

CB-79



PLASTIC PACKAGE



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NOTES

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HOMSON COMPONENTS
EMICONDUCTEURS

TDA4445A • TDA4445B

SOUND IF AMPLIFIER

ADVANCE INFORMATION

TDA 4445A:
Sound IF amplifier, with FM processing for quasi parallel sound system.

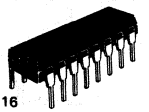
TDA 4445B:
Sound IF amplifier, with FM processing and AM demodulator, for multi-standard sound TV appliances.

Main features:
- Quadrature intercarrier demodulator.
- Very high input sensitivity.
- Excellent signal to noise ratio.
- Fast averaging AGC.
- IF amplifier can be switched off for VTR mode.
- Good AM suppression.
- Output signal stabilized against supply voltage variations.
- Very few external components.

TDA 4445B additionnal:
- Bistandard applications (B/G and L).
- No adjustment of the AM demodulator.
- Low AM distortion.

SOUND IF AMPLIFIER

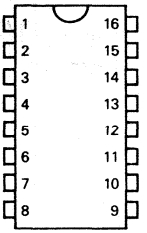
CASE CB-79



PLASTIC PACKAGE

PIN ASSIGNMENT

TDA 4445A	TDA 4445B
1 - IF input	1 - IF input
2 - Not to be connected	2 - Not to be connected
3 - IF AGC time constant	3 - IF AGC time constant
4 - Not to be connected	4 - Not to be connected
5 - Not to be connected	5 - Averaging capacitor
6 - Not to be connected	6 - A.F. sound output
7 - Not to be connected	7 - Not to be connected
8 - Reference LC network	8 - Reference LC network
9 - Reference LC network	9 - Reference LC network
10 - Not to be connected	10 - Not to be connected
11 - Supply voltage	11 - Supply voltage
12 - FM modulated sound output	12 - FM modulated sound output
13 - Ground	13 - Ground
14 - Not to be connected	14 - Not to be connected
15 - Not to be connected	15 - Not to be connected
16 - IF input	16 - IF input



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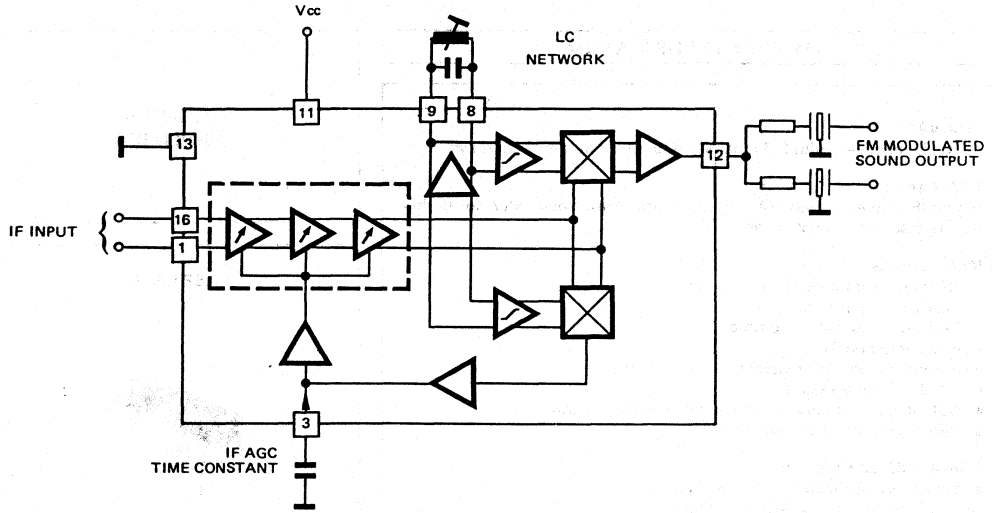
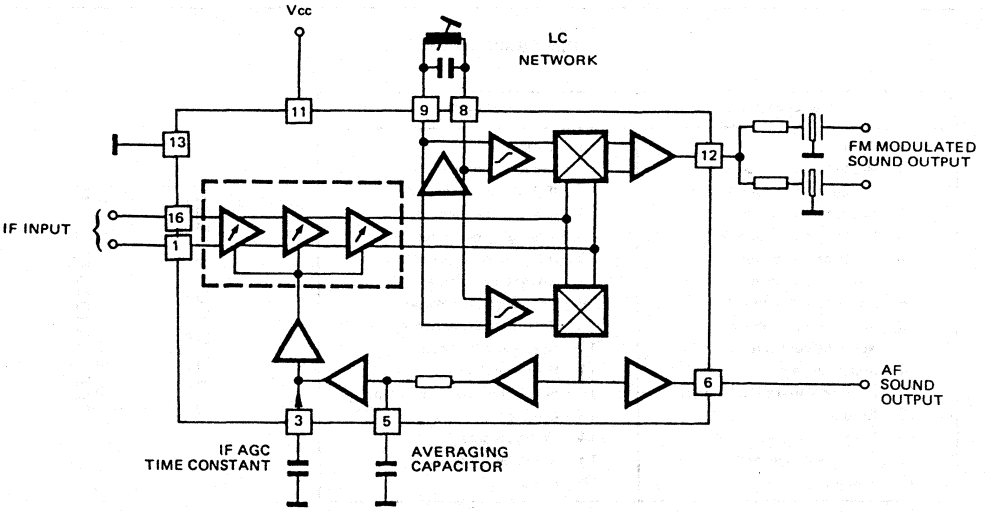
BLOCK DIAGRAMS

TDA4445A



TDA4445B



GENERAL DESCRIPTION

This circuit includes the following functions:

- Three symmetrical and gain controlled wide band amplifier stages, which are extremely stable by quasi DC coupling without feedback.
- Averaging AGC with discharge control circuit.
- AGC voltage generator.

Quasi parallel sound operation:

- High phase accuracy of the carrier signal processing, independent from AM.
- Linear quadrature demodulator.
- Sound-IF-amplifier stage with impedance converter.

AM-Demodulation (only TDA4445B):

- Carrier controlled demodulator.
- Audio frequency stage with impedance converter.
- Averaging low pass AGC.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply voltage	Pin 11	V_{CC}	15	V
Supply current	Pin 11	I_{CC}	70	mA
External voltages				
TDA4445A/TDA4445B	Pin 3	V_{ext}	12	V
	Pin 12	V_{ext}	8	V
External voltages				
only TDA4445B	Pin 5	V_{ext}	8	V
	Pin 6	V_{ext}	8	V
Power dissipation		P_{tot}	1	W
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	- 25 to + 70	°C
Storage temperature range		T_{stg}	- 25 to + 125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction - ambient thermal resistance	$R_{th(j-a)}$	70	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25°C, V_{CC} = 12 V (Unless otherwise specified)

Characteristic		Symbol	Min.	Typ	Max.	Unit
● DC CHARACTERISTICS						
Supply voltage	Pin 11	V_{CC}	10	12	15	V
Supply current V_{1-16} = 10 mV, or V_3 = 3.5 V	Pin 11	I_{CC}	—	52	—	mA
DC output voltage V_{1-16} = 10 mV, unmodulated	Pin 12	V_O	—	5.0	—	V
Output DC current V_{11} = 7.5 V, V_3 = 3.5 V	Pin 12	I_{max}	—	1.8	—	mA
Input impedance : Resistance	Pins 1 - 16	R	—	1.6	—	KΩ
Capacitance	Pins 1 - 16	C	—	2.0	—	pF
Switch off control voltage for VTR mode	Pin 3	V	8	—	10	V
Switch off control current for VTR mode	Pin 3	I	50	—	150	μA
● AGC CHARACTERISTICS IF AGC range		ΔG_{IF}	—	64	—	dB
AGC capacitor (control time constant)						
TDA4445A	Pin 3	C3	0.33	—	10	μF
TDA4445B	Pin 3	C3	—	10	—	μF
	Pin 5	C5	—	4.7	—	μF
● QUASI PARALLEL SOUND OPERATION (TDA4445A and TDA4445B) f_{PC} = 38.9 MHz, f_{SC1} = 33.4 MHz, f_{SC2} = 33.16 MHz, PC/SC_1 = 13 dB, PC/SC2 = 20 dB, PC unmodulated						
Min. input voltage 5.5 MHz - output signal - 3 dB	Pins 1 - 16	V_I	—	50	—	μV
Max. input voltage 5.5 MHz - output signal + 1 dB	Pins 1 - 16	V_I	—	80	—	mV
Sound-IF-output voltage V_{1-16} = 10 mV, SC unmodulated						
5.5 MHz output voltage	Pin 12	V_O	—	250	—	mV
5.74 MHz output voltage	Pin 12	V_O	—	110	—	mV
Signal to noise ratio measured according to CCIR 468-2 reference signal: V_{1-16} = 10 mV, FM-frequency deviation = ± 30 kHz f_{mod} = 1 kHz, measured at audio-output sound IF demodulator 2 x U 829 B						
Black screen 1. Channel/2. Channel	Pin 12	$\frac{S+N}{N}$	—	62/58	—	dB
Grid screen 1. Channel/2. Channel	Pin 12	$\frac{S+N}{N}$	—	52/49	—	dB

* f_{PC} : Picture carrier frequency, f_{SC1} : Sound 1 carrier frequency, f_{SC2} : Sound 2 carrier frequency

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

T_{amb} = + 25°C, V_{CC} = 12 V (Unless otherwise specified)

Characteristic		Symbol	Min.	Typ	Max.	Unit
● AM DEMODULATION (TDA4445B only) f_{SC} = 39.2 MHz, m = 80%, f_{mod} = 1 kHz Min. input voltage Audio output signal - 3 dB	Pins 1 - 16	V_I	—	50	—	µV
Output DC voltage V_{1-16} = 10 mV, unmodulated	Pin 6	V_O	—	4.1	—	V
Output DC current V_6 = 7.5 V, V_3 = 3.5 V	Pin 6	I_{max}	—	0.65	—	mA
Distortion V_{1-16} = 10 mV, m = 80% f_{mod} = 1 kHz	Pin 6	d	—	1.5	3.0	%
AF output voltage V_{1-16} = 10 mV, m = 80% f_{mod} = 1 kHz	Pin 6	V_O	—	850	—	mV

TYPICAL APPLICATION

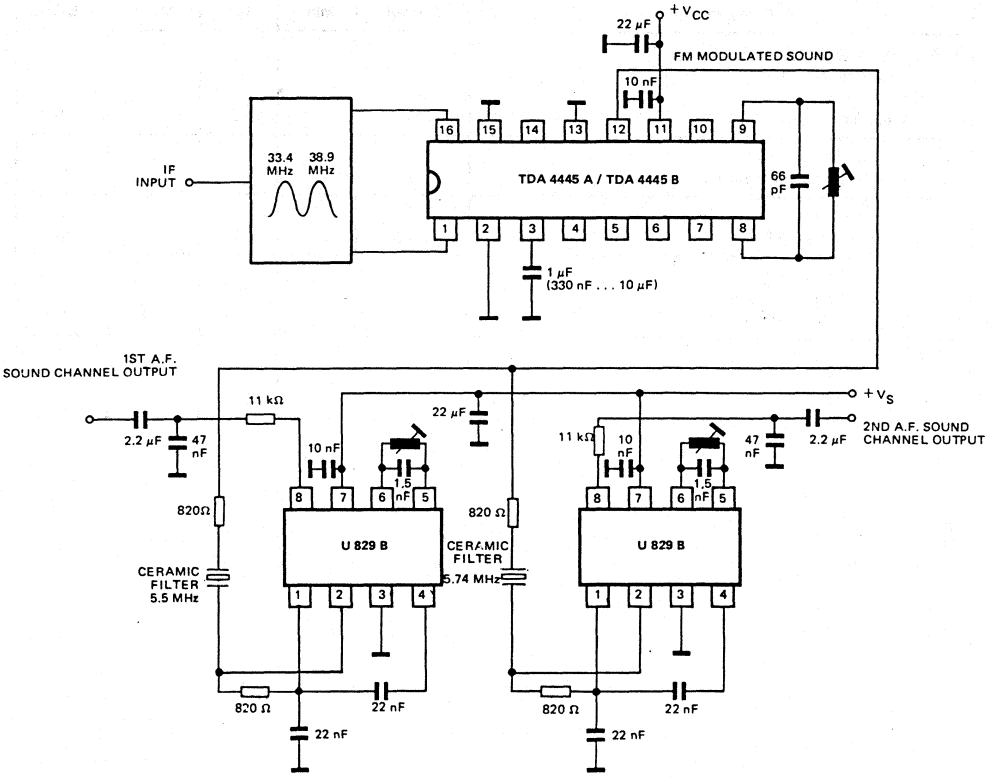


FIGURE 1 — QUASI PARALLEL SOUND OPERATION

TYPICAL APPLICATION

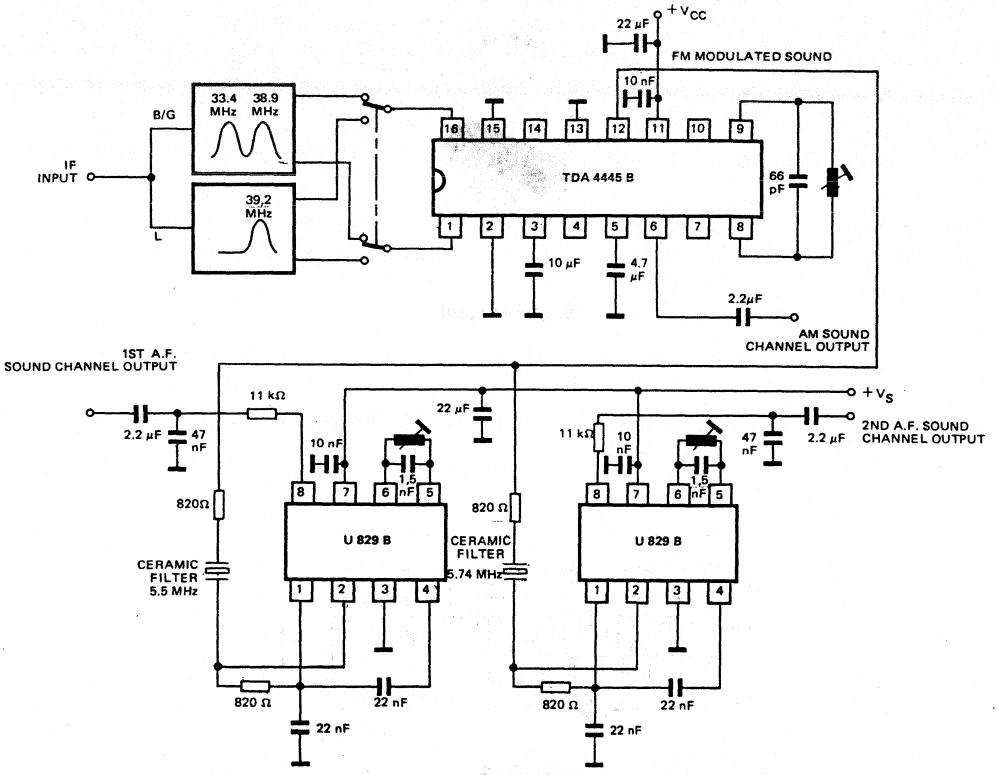
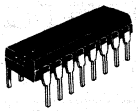


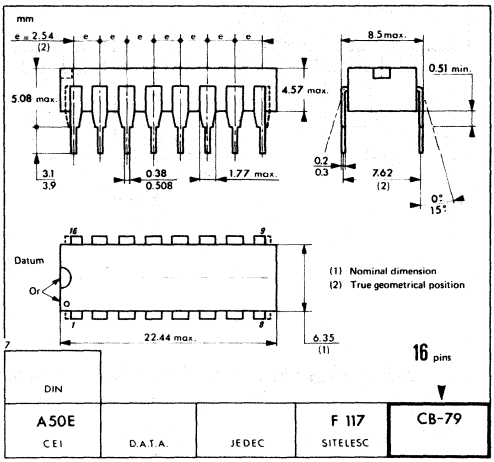
FIGURE 2 — BISTANDARD OPERATION (FM STEREO SOUND + AM SOUND)

PHYSICAL DIMENSION

CB-79



PLASTIC PACKAGE



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THOMSON COMPONENTS SEMICONDUCTEURS

TEA1014

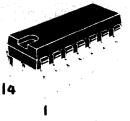
VIDEO AND AUDIO SIGNALS SWITCHING FOR THE PERI-TELEVISION PLUG

This integrated circuit provides all video and sound switching allowing connections between the peri-TV plug and video, sound sections in the TV set.
Input and output signal characteristics follow the NFC 92250/ EN 50049 norms.

- Video crosstalk:60 dB typical
- Low impedance video output 75 Ω
- Short-circuit protection of inputs and outputs
- Internal horizontal PLL time constant switching in case of video recorder reception.

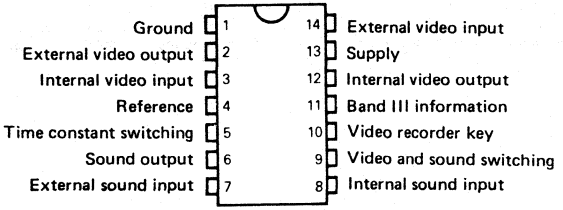
VIDEO AND AUDIO SIGNALS SWITCHING FOR THE PERI-TELEVISION PLUG

CASE CB-2



PLASTIC PACKAGE

PIN ASSIGMENT



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CIRCUIT DESCRIPTION

The main functions of the I.C. are following :

VIDEO SWITCHING

2 electronically switched inputs :

- one 2.5 Vpp input for internal video.
- one 1 Vpp input for signal coming from the peri-TV plug.

2 outputs :

- 1 Vpp output (low impedance 75 Ω) for peri-TV plug
- 1 Vpp output low impedance for video section of the TV set.

Each input and output is protected from ground short-circuit. The 75 Ω output is protected through a 75 Ω resistor.

AUDIO SWITCHING

Two electronically switched inputs :

- 300 mV rms input coming from internal audio.
- 100 mV rms input coming from the peri-TV plug

one low impedance output 300 mV rms.

Inputs and outputs are also protected against ground short-circuit.

SWITCHING LOGIC

The logic takes into account the informations on 3 pins.

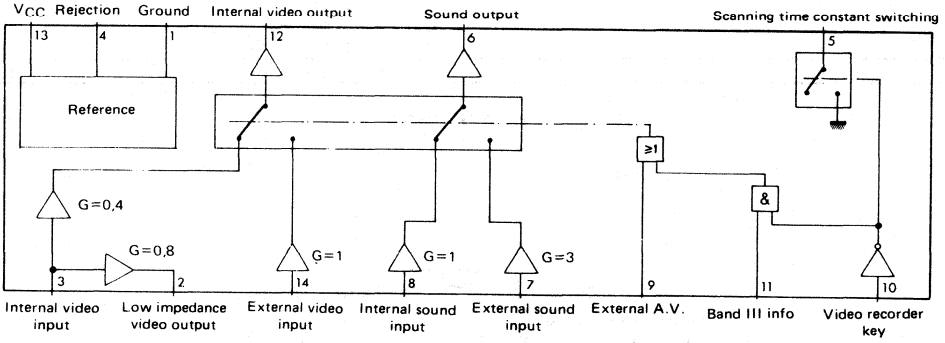
- Internal or external video and sound (pin 8 peri TV plug)
- Band III information
- Video recorder key.

External Video and Audio signals are selected in two cases.

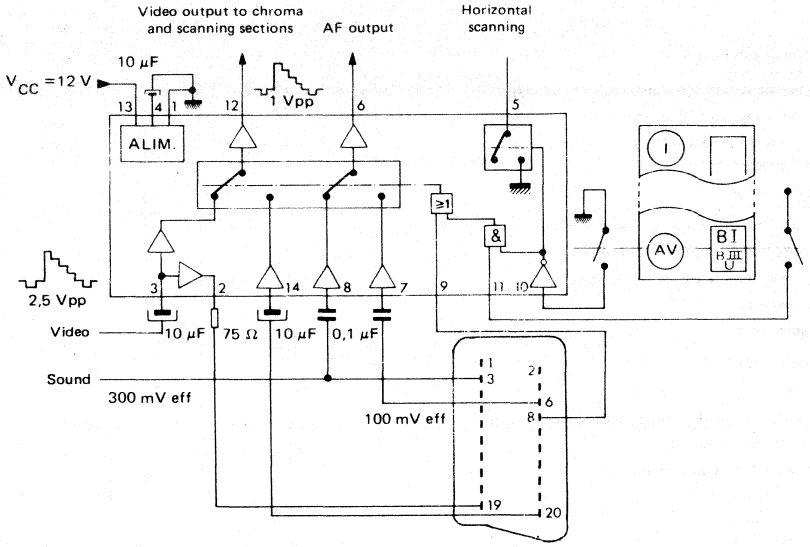
- When there is a voltage information coming from peri-TV plug.
- When the video recorder key is selected (on TV front panel) and programmed on band III.

This I.C. includes an internal switch (open collector transistor) which commutes the time constant of the horizontal PLL circuit in case of video recorder reception.

BLOCK DIAGRAM



APPLICATION CIRCUIT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	18	V
Storage temperature range	T_{stg}	- 40, + 150	°C
Junction temperature	T_j	+ 150	°C
Operating ambient temperature	T_{oper}	0 to 70	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction ambient thermal resistance	$R_{th(j-a)}$	90	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = + 25°C (Unless otherwise specified).

Characteristic	Symbol	Min	Typ	Max	Unit
Supply current, with no load		–	37	50	mA
Internal video input (coming from picture FI) (Pin 3)					
Video signal amplitude (Positive video)		–	2.5	6.8	V_{PP}
Input voltage range (refered to D.C. input voltage)		- 2.9	–	+ 3.9	V
Input impedance		5	–	–	kΩ
Input capacitance		–	–	5	pF
External video input (Coming from peri-TV plug) (Pin 14)					
Video signal amplitude (Positive video)		–	1	2.8	V_{PP}
Input voltage range (Refered to D.C. input voltage)		- 1.2	–	+ 1.6	V
Input impedance		5	–	–	kΩ
Input capacitance		–	–	5	pF
TV video output (Pin 12)					
Signal amplitude		–	1	2.8	V_{PP}
Output voltage swing (Refered to D.C. output voltage)		- 1.2	–	+ 1.6	V
Output dynamic impedance		–	–	10	Ω
D.C. output voltage (Without input signal)		–	3.5	–	V
Loading resistance		300	–	–	Ω
Video bandwidth (–1dB)		6	–	–	MHz
Gain/internal video		– 9.5	– 8	– 6.5	dB
Gain/external video		– 1.5	0	+ 1.5	dB
External video output (low impedance) (Pin 2)					
Signal amplitude (on 150 Ω grounded)		–	2	5.5	V_{PP}
Output voltage swing		- 2.4	–	+ 3.1	V
Dynamic output impedance		–	10	–	Ω
D.C. output voltage (without input signal)		–	3.5	–	V
Minimum loading resistance (Electrical performance non specified)		75	–	–	Ω
Gain/internal video		– 3.5	– 2	– 0.5	dB
Output video signals characteristics					
Video rejection between two inputs (1 MHz)		- 55	–	–	dB
Differential group delay		–	–	20	ns
Linearity distortion					
Luma (Test line 17)		–	2	–	%
Chroma (Test line 331)		–	2	–	%
Intermodulation luma-chroma (Test line 331)		–	5	–	%
Supply voltage rejection		45	–	–	dB

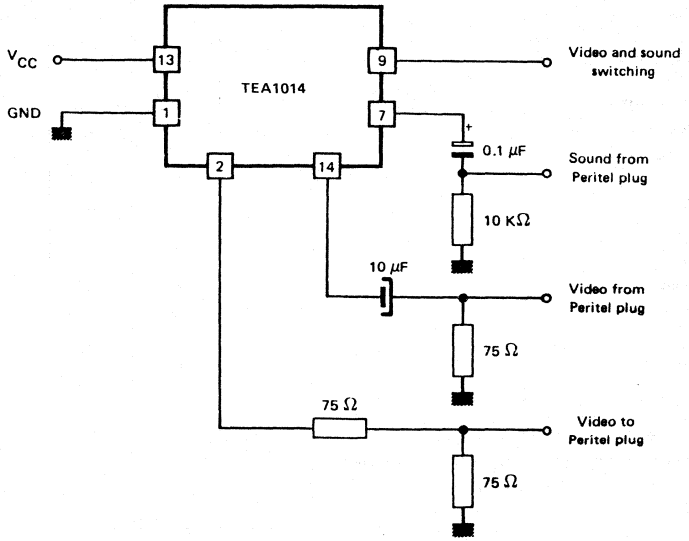
ELECTRICAL OPERATING CHARACTERISTICS (Continued)

V_{CC} = 12 V ; T_{amb} = + 25°C (Unless otherwise specified).

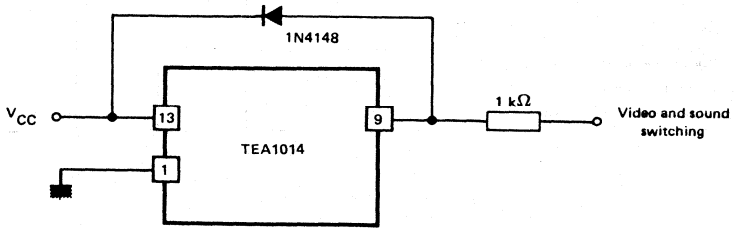
Characteristic	Symbol	Min	Typ	Max	Unit
Internal sound input (Pin 8)					
Input signal		–	0.3	2	V_{eff}
Input impedance		–	20	–	kΩ
External sound input (Pin 7)					
Input signal		–	0.1	0.7	V_{eff}
Input impedance		–	20	–	kΩ
Sound output (Pin 6)					
Output signal amplitude		–	0.3	–	V_{eff}
Output voltage swing		–	2	–	V_{eff}
Distortion (V_O = 0.6 V_{eff})		–	–	0.5	%
Bandwidth		16	–	–	KHz
Output impedance		–	40	–	Ω
Load impedance		2	–	–	kΩ
Gain/internal input		– 1.5	0	+ 1.5	dB
Gain/external input		8	9.5	11	dB
Supply voltage rejection		60	–	–	dB
Crosstalk		- 60	–	–	dB
Video/sound crosstalk		- 60	–	–	dB
LOGIC					
External A.V. input (peri-TV plug) (Pin 9)					
Unactive low level or unconnected pin (logic state 0) - (TV receiving)		0	–	3	V
Active high level (logic state 1) (Ext. receiving)		9	–	V_{CC}	
Input impedance		–	10	–	kΩ
"Band III" input (Pin 11)					
Unactive low level or unconnected pin (logic state 0)		0	–	+ 3	V
Active high level (logic state 1)		9	–	V_{CC}	V
Input impedance high level		–	10	–	kΩ
Input current low level		–	–	1	μA
Video-recorder key input (Pin 10)					
Unactive high level or unconnected pin (logic state 1)		9	–	V_{CC}	V
Active low level (logic state 0)		0	–	3	V
Input impedance		–	10	–	kΩ
Open collector output (time - constant switching) (Pin 5)					
Leakage current (open collector)		–	–	1	μA
Maximum low level voltage (I(5) = 4 mA)		–	–	1.5	V

SAFETY INFORMATION FOR CRITICAL APPLICATIONS

- Typical connection between Peritel plug and TEA2014

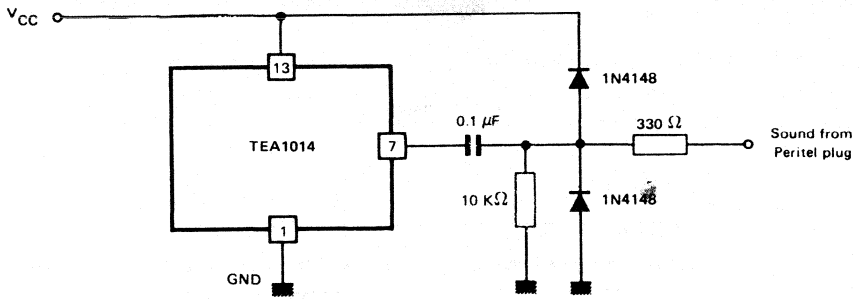


- Voltage on pin 9 must not exceed the V_{CC} voltage on pin 13. In case of risk of over voltage, use the protection as described as below:



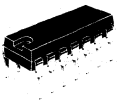
• All connections to Peritel plug are terminated by low impedance loads (75 Ω), except the external sound input.

In case of risk of electrostatic discharge, use the protection as described as below.

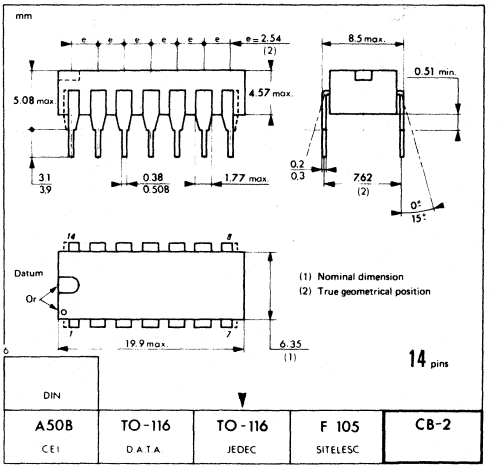


PHYSICAL DIMENSIONS

CASE CB-2 (TO-116)



PLASTIC PACKAGE



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TEA2014

VIDEO SWITCHING

ADVANCE INFORMATION

This integrated circuit provides all video switching allowing connections between the peri TV plug and video sections in the TV set. The TEA 2014 is supplied in a 8 leads case CB-98.

Main features

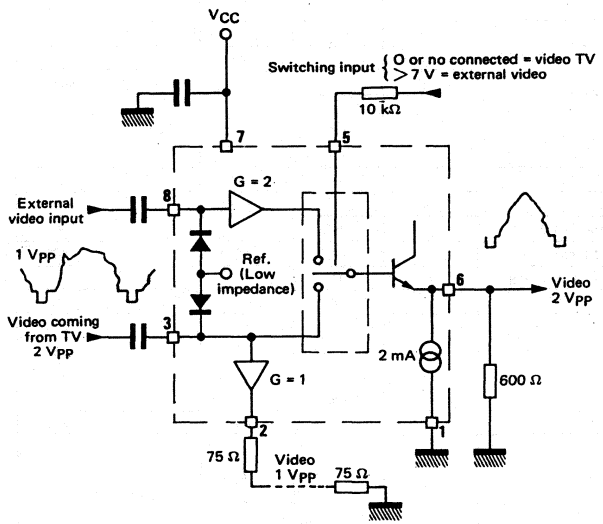
- 1 video output 75 Ω - 1 Vpp no switched
- 1 switched video output 2 Vpp
- Video cross talk : 50 db typical
- Short circuit protection of inputs and outputs
- Clamped video inputs.

VIDEO SWITCHING

CASE CB-98

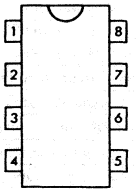
PLASTIC PACKAGE

TYPICAL APPLICATION AND TEST CIRCUIT



We advice to protect the 75 Ω output through a 75 Ω resistor for supply voltage upper than 9 V.

PIN ASSIGNMENT



1 - Ground
2 - 75 Ω video output
3 - Internal video input
4 - Not to be used
5 - Switching input
6 - Switched video output
7 - Supply voltage
8 - External video input

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	18	V
Operating temperature with load > 150 Ω with load = 75 Ω	T_{oper}	 −10,+ 100 −10,+ 70	°C
Junction temperature	T_j	−40,+ 150	°C
Storage temperature	T_{stg}	−40,+ 150	°C
Minimum DC load resistor P6		600	Ω
Minimum DC load resistor P2		75	Ω

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	90 typ.	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25°C, V_{CC} = 9 V (unless otherwise noted)

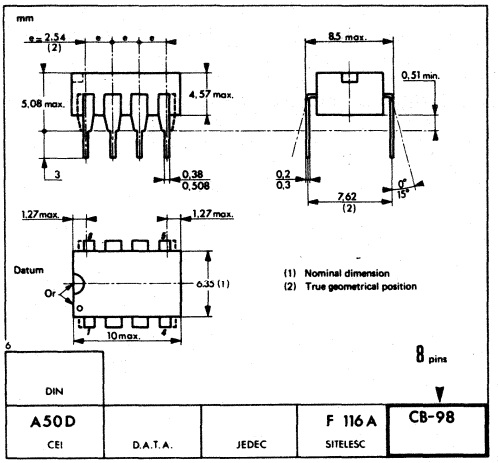
Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage range	V_{CC}	8	–	14	V
Supply current (no load on pin 2 and pin 6)	I_{CC}	–	–	20	mA
Supply current (with 75 Ω between pin 2-1, with 600 Ω between pin 6-1)	I_{CC}	–	75	–	mA
Total power dissipation with load	P_{tot}	–	450	–	mW
Internal video input swing from picture FI (Positive video)		–	–	4.5	V_{PP}
Internal video input impedance (Positive video)		–	50	–	KΩ
Internal video input bias current (Positive video)		–	10	25	40	μA
External video input swing (Positive video)		–	–	–	2	V_{PP}
External video input impedance (positive video)		–	50	–	–	KΩ
Switched video output swing		–	–	–	4.5	V_{PP}
Switched video output dynamic impedance		–	–	–	20	Ω
Switched video DC output voltage (Sync. pulse level, note 1) (600 Ω)		–	1,7	2	2,4	V
Switched video band width (−1 dB)		–	6	–	–	MHz
Switched video output gain Pin 6 - pin 8 (gain with 600 Ω load) Pin 6 - pin 3 (gain with 600 Ω load)		– –	 + 4 −1	 + 5 −0.5	 + 6 0	dB
External video output swing (with 75 Ω load)		–	–	2	2.2	V
External video dynamic output impedance		–	–	10	–	Ω
External video DC output voltage (Sync. pulse level, note 1) (75 Ω)		–	1,7	2	2,4	V
External video output gain (Pin 2 - pin 3 gain with 75 Ω load)		–	−1.8	−1	−0.4	dB
Switching input unactive low level or unconnected pin (TV receiving)		–	0	–	3	V
Switching input active level (ext. receiving)		–	7	–	V_{CC}	V
Switching input impedance		–	10	–	–	KΩ
Video rejection between two inputs 0 to 5 MHz 1 KHz		 – –	 – −50	 −50 –	 – –	dB
Differential group delay		–	–	15	–	ns
Linearity distortion Luma (test line 17) Chroma (test line 331) Intermodulation Luma - Chroma (test line 331)			 – – –	 2 2 5	 – – –	%
Supply voltage rejection (1 KHz)		–	40	50	–	dB

Note 1 : Use a video signal with a synchro pulse in order to make the clamp work in a correct way (75 Ω to the ground and 10 μF in serie).

PHYSICAL DIMENSIONS

CB-98

PLASTIC PACKAGE



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NOTES

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THOMSON COMPONENTS
EMICONDUCTEURS

TEA5114 • TEA5114A

RGB SWITCHING CIRCUIT

This integrated circuit provides RGB switching allowing connections between peri TV plug, internal RGB generator and video processor in a TV set

The input signal black level is tied to the same reference voltage on each input in order to have no differential voltage when switching two RGB generators.

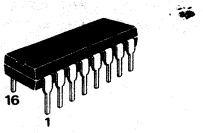
An AC output signal higher than 2 Vpp (TEA5114A) or 1.5 Vpp (TEA5114) makes gain going slowly down to 0 dB to protect the TV set video amplifier from saturation.

Fast blanking output is a logical OR between FB_1 (Pin 8) and FB_2 (Pin 10).

- 25 MHz bandwidth
- Crosstalk : 55 dB
- Short circuit to ground or V_{CC} protected
- Anti saturation gain changing
- Video switching

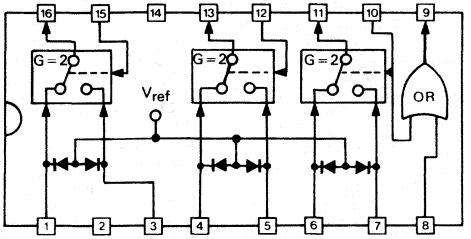
RGB
SWITCHING CIRCUIT

CASE CB-79

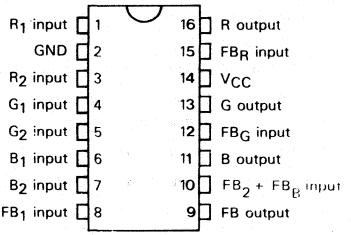


PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	18	V
Junction temperature	T_j	− 40 to + 150	°C
Storage temperature	T_{stg}	− 40 to + 150	°C
Minimum load resistor on each output V_{CC} = 12 V V_{CC} = 10 V	Z_L	 300 150	 Ω Ω
Operating ambient temperature	T_{amb}	0 to 70	°C

THERMAL CHARACTERISTICS

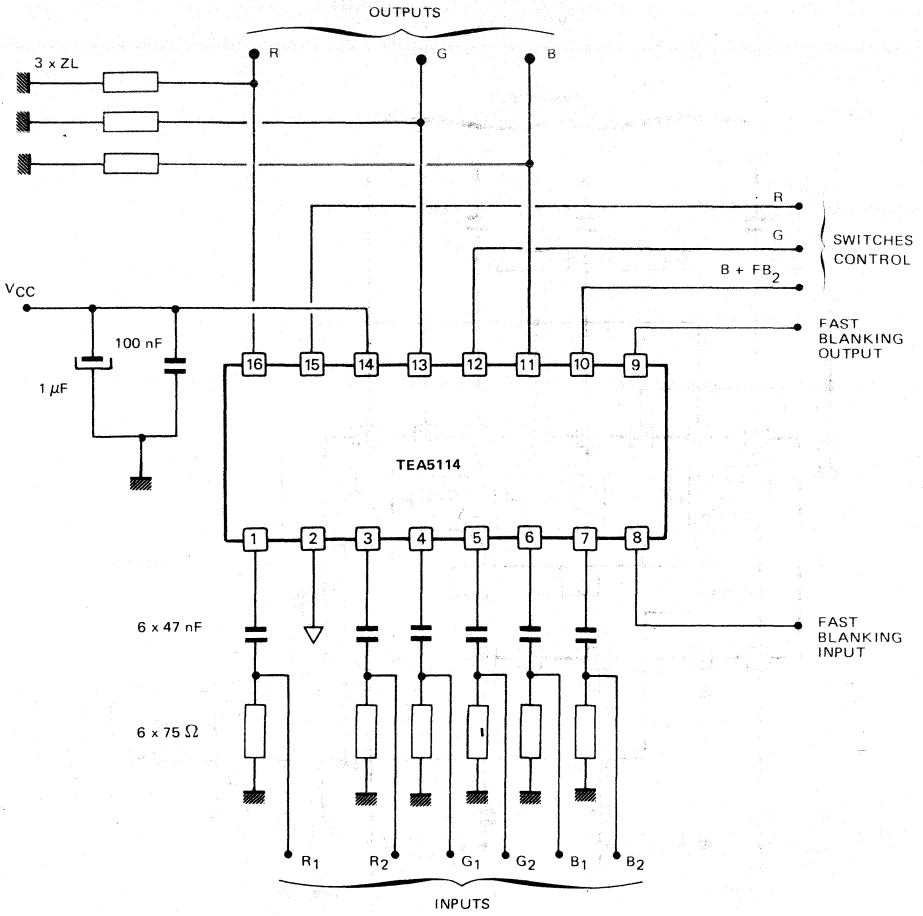
Characteristic	Symbol	Value	Unit
Junction ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C V_{CC} = 12 V, Z_L (RGB) = 300 Ω
V_{CC} = 10 V, Z_L (RGB) = 150 Ω (unless otherwise specified)

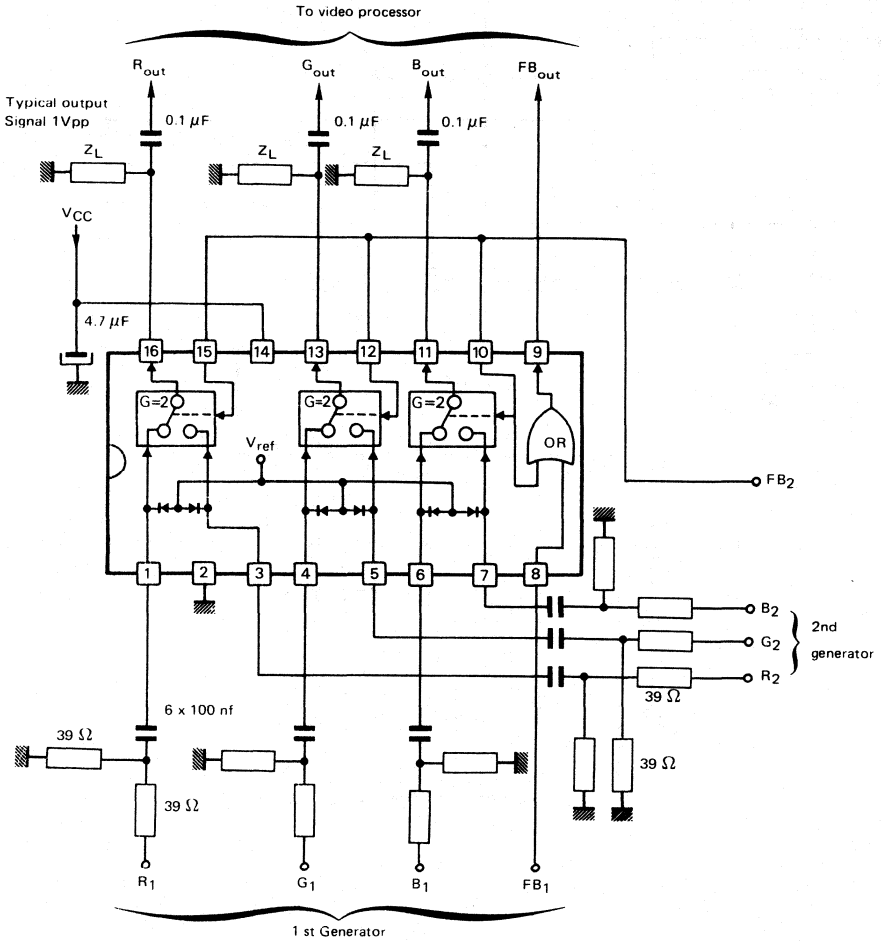
Characteristic		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	9	12	13.2	V
Supply current without load V_{CC} = 12 V		I_{CC}	20	30	40	mA
Black level output voltage (on pins 11, 13, 16 square wave output signal 1 kHz - 1 Vpp) T_j = 25 °C (5 mV/°C typical variation)		V_{ON}	1.8	2.5	2.9	V
Gain of each channel pins 11, 13, 16	TEA5114, Vo = 1 Vpp	G_{RGB}	5	5.5	6	dB
F = 1 MHz - V_o = 1 V_{pp}	TEA5114A, Vo = 2 Vpp	G_{RGB}	5	5.5	6	dB
Bandwidth (− 3 dB) V_O = 1 V_{pp}		B_{RGB}	20	25	−	MHz
Threshold output voltage for gain changing	TEA5114	V_{GC}	1.5	−	−	V_{pp}
(− 0.5 dB)	TEA5114A	V_{GC}	2	−	−	V_{pp}
Video rejection between two inputs R, G or B F = 1 MHz sinus V_O = 1 V_{pp}		V_R	50	55	−	dB
Input impedance on pins 1, 3, 4, 5, 6, 7 V_O = 1 V_{pp}		Z_{IRGB}	10	−	−	kΩ
R, G, B output impedance on pins 11, 13, 16		Z_{ORGB}	−	−	15	Ω
FB rising and falling time on pin 9. 1 V_{pp} input voltage Pins 8, 10		T_{FB}	−	20	−	ns
FB high level input voltage on pins 8, 10, 12, 15		V_{IHFB}	1	−	4	V
FB low level input voltage on pins 8, 10, 12, 15		V_{ILFB}	0	−	0.4	V
Input impedance on pins 8, 10, 12, 15		Z_{IFB}	0.7	1	1.3	kΩ
High level FB output voltage (pin 9) Input 1 V on pins 8, 10		V_{OHFB}	0.8	1	1.2	V
Low level FB output (pin 9) Input 0V on pins 8, 10		V_{OLFB}	−	−	0.3	V
FB output impedance Pin 9 high level		Z_{OFB}	−	−	30	Ω
Delay time between FB inputs and R, G, B switching		T_{dFBRGB}	−	20	−	ns

TEST DIAGRAMM



TYPICAL R, G, B SWITCHING APPLICATION

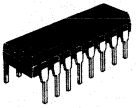
$V_{CC} = 12\ V$ $\quad Z_L \geqslant 300\ \Omega$
$V_{CC} = 10\ V$ $\quad Z_L \geqslant 150\ \Omega$



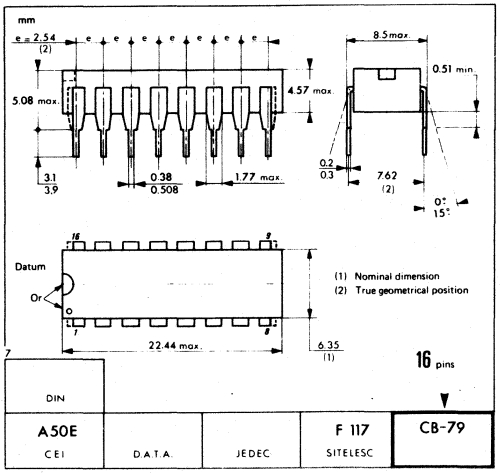
Peritelevision plug standard input value 1 Vpp

PHYSICAL DIMENSIONS

CASE CB-79



PLASTIC PACKAGE



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Please inquire with our sales offices about the availability of the different packages

NOTES

THOMSON COMPONENTS SEMICONDUCTEURS

TEA5115

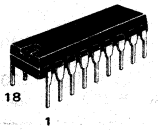
5 SWITCHES FOR VIDEO AND RGB SELECTION

ADVANCE INFORMATION

- This IC allows to select one of two channels of 5 signals : RGB, Fast Blanking and synchronizing or video signal (S).
- Each channel has 6 dB gain.
- R, G, B and S signals are clamped to the same reference voltage on each input in order to have no differential voltage when switching.
- All input levels compatible with NFC 92250 and EN 50049 norms.
- 25 MHz band width for R, G, B signal.
- Internal 6.5 V shunt regulator
  - allows low impedance loads
  - limits power dissipation
- Independant video or synchronizing signal selection.
- Simultaneous switching of R, G, B and FB signals by FB1 input.

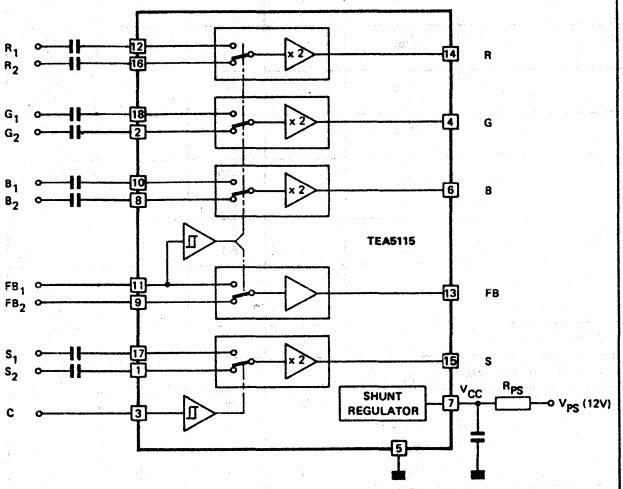
5 SWITCHES FOR VIDEO AND RGB SELECTION

CASE CB-181

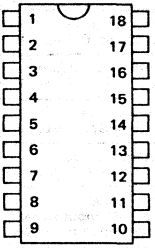


PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



1 - Synchro signal input 2
2 - Green signal input 2
3 - "C" select input
4 - Green signal output
5 - Ground
6 - Blue signal output
7 - Shunt regulator supply input
8 - Blue signal input 2
9 - Fast blanking input 2
10 - Blue signal input 1
11 - Fast blanking input 1
12 - Red signal input 1
13 - Fast blanking output
14 - Red signal output
15 - Synchro signal output
16 - Red signal input 2
17 - Synchro signal input 1
18 - Green signal input 1

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply current	I_{CC}	150	mA
Input voltage (all inputs)	V_{in}	-0.5 to $V_{CC}+0.5$	V
Operating temperature range	t_{oper}	0 to 70	°C
Junction temperature	T_j	-40 to $+150$	°C
Storage temperature	T_{stg}	-40 to $+150$	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th\ (j-a)}$	70	°C/W

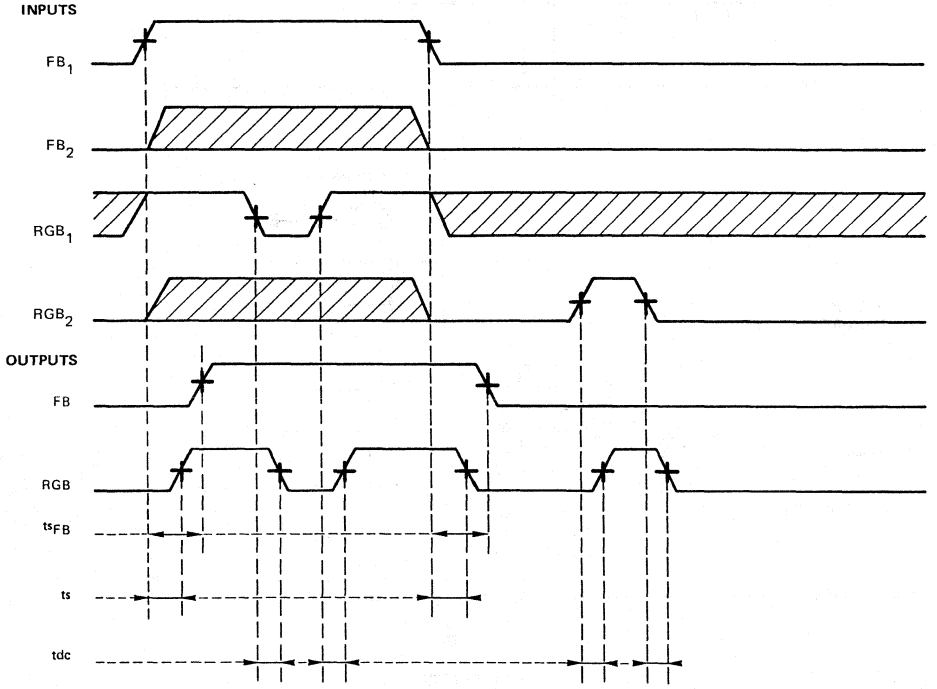
ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = +25°C$, $I_{CC} = 120$ mA
Load value = 150 Ω (sequentially switched)
} Unless otherwise specified, refer to test circuit page 4.

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	6.3	6.5	7	V
R, G, B SWITCHES (Pins 4, 6, 14)					
DC output voltage (no input voltage)	V_C	–	1.2	1.5	V
Max output swing voltage	V_{AC}	2	2.5	–	Vpp
Bandwidth (– 3dB) (input voltage : 0.7 Vpp)	B	20	25	–	Mhz
Gain of each channel (input voltage: 0.7 Vpp, F = 1 MHz)	A_V	5.5	6	6.5	dB
Gain difference between any two R, G, B channels (input voltage: 0.7 Vpp, F = 1 MHz)	A_{dc}	–	0.1	0.5	dB
Input impedance (input voltage: 0.7 Vpp, F = 1 MHz)	Z_{ic}	–	10	–	kΩ
Output impedance (input voltage: 0.7 Vpp, F = 1 MHz)	Z_{oc}	–	10	–	Ω
Switching time between FB1 input signal and any R, G, B output signal (FB1 pulse amplitude : 2 V)	t_s	–	100	–	nsec
Delay time between R, G, B inputs and R, G, B outputs (Δ input: 0.7 Vpp)	T_{dc}	–	50	–	nsec
Cross talk between any inputs (R1 and R2, or B1 and B2, or G1 and G2) (input voltage: 0.7 Vpp, F = 1 MHz)		50	–	–	dB
Cross talk between any outputs (input voltage: 0.7 Vpp, F = 1 MHz)		50	–	–	dB
FAST BLANKING SWITCH (Pin 13)					
Low level input voltage	V_{IL}	-0.5	–	0.4	V
High level input voltage	V_{IH}	1	–	$V_{CC}+0.5$	V
Low level output voltage	V_{OL}		–	0.8	V
High level output voltage	V_{OH}	1.8	–	3.5	V
Switching time between FB inputs and FB outputs (FB1 pulse amplitude: 2 V)	t_s FB	–	130	–	nsec

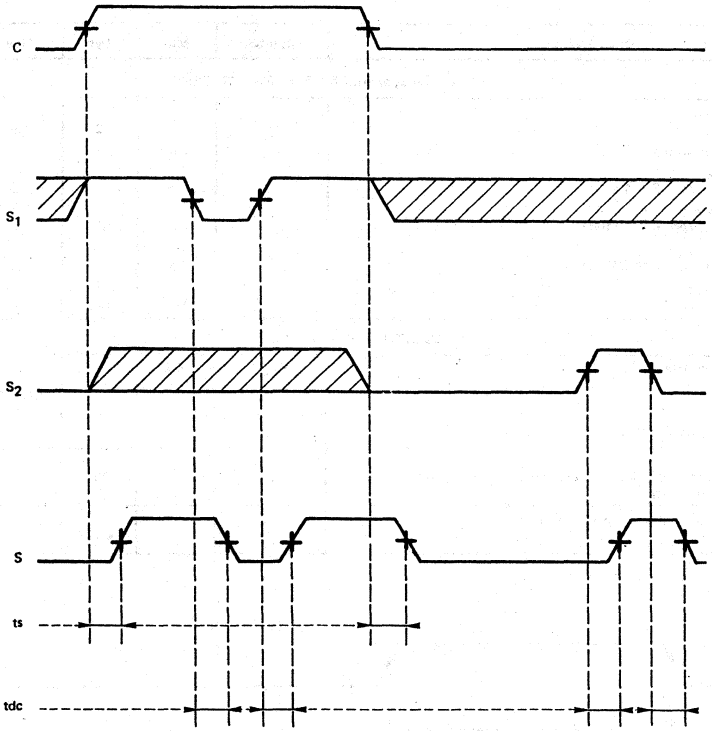
ELECTRICAL OPERATING CHARACTERISTICS (Cont'd).

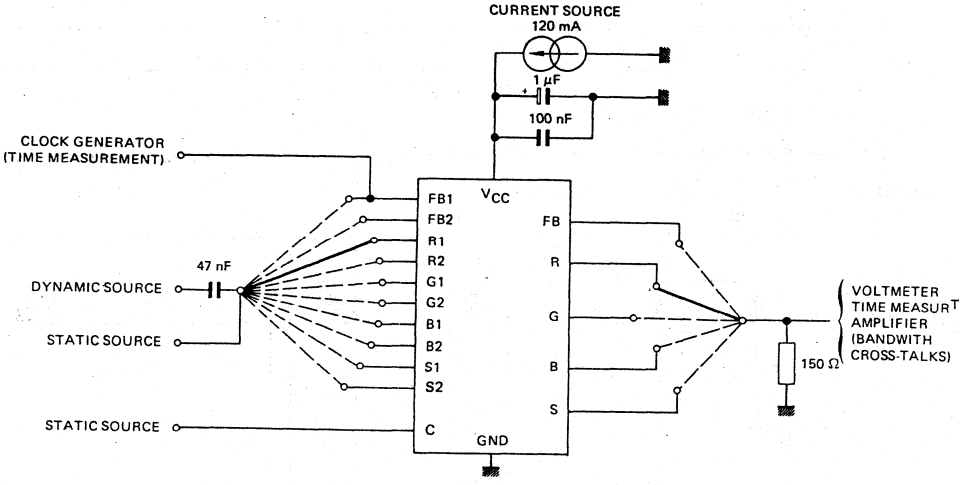
Characteristic	Symbol	Min	Typ	Max	Unit
VIDEO (or synchro.) SIGNAL SWITCH (Pin15)					
DC output voltage (no input voltage)	V_S	–	1.2	1.5	V
Max output swing voltage		2.6	–	–	Vpp
Input impedance (input voltage : 1 Vpp. F = 1 MHz)		–	10	–	kΩ
Output impedance (input voltage : 1 Vpp. F = 1 MHz)		–	10	–	Ω
Gain (input voltage : 1 Vpp. F = 1 MHz)		5.5	6	6.5	dB
Bandwidth (– 3 dB) (input voltage : 1 Vpp)		15	20	–	MHz
SELECT INPUT "C" (Pin3)					
Low level input voltage	V_{IL}	– 0.5	–	1	V
High level input voltage	V_{IH}	2	–	V_{CC}+ 0.5	V
Low level input current	I_{IL}	– 0.8	–	– 0.1	mA
High level input current (V_{IH} = 3 V)	I_{IH}			0.5	mA
Switching time between C input signal and S output signal (C pulse amplitude: 3 V)	t_s	–	100	–	nsec
Delay time between S input and S output (Δ input: 0.7 Vpp)	t_{dc}	–	50	–	nsec



SWITCHING WAVE FORMS

S CHANNEL

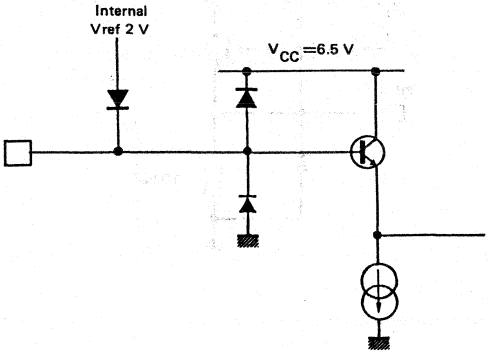




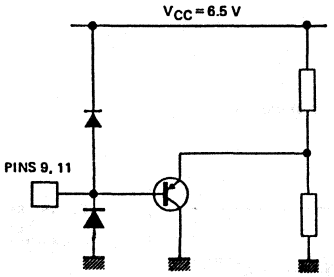
TEST CIRCUIT

INPUTS/ OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

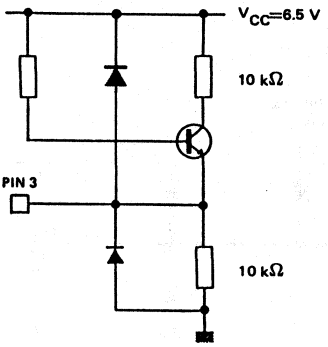
- R, G, B, S inputs (pins 1, 2, 8, 10, 12, 16, 17, 18)



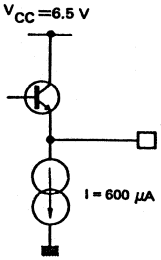
- FB inputs (pins 9, 11)



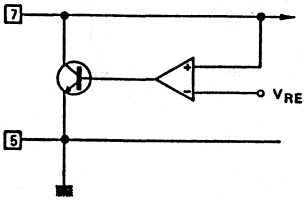
●C input (pin 3)



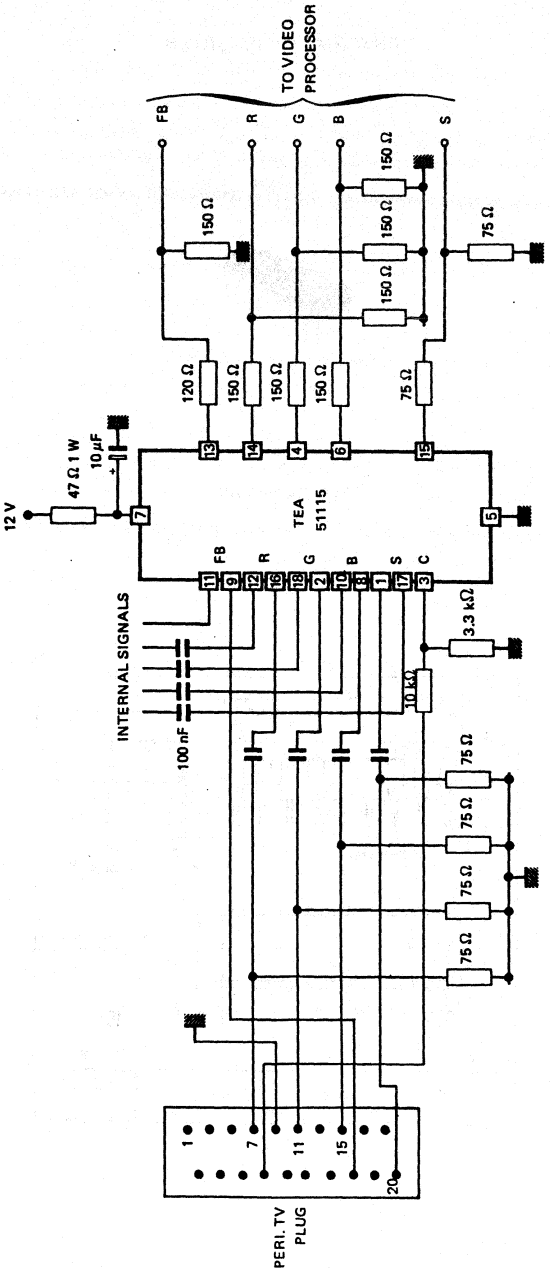
●All outputs (Pins 4, 6, 13, 14, 15)



● I_{CC} supply (Shunt transistor regulation system) (pin 7)



Refer to application diagram page 7

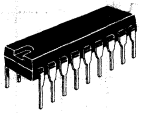


TYPICAL APPLICATION DIAGRAM

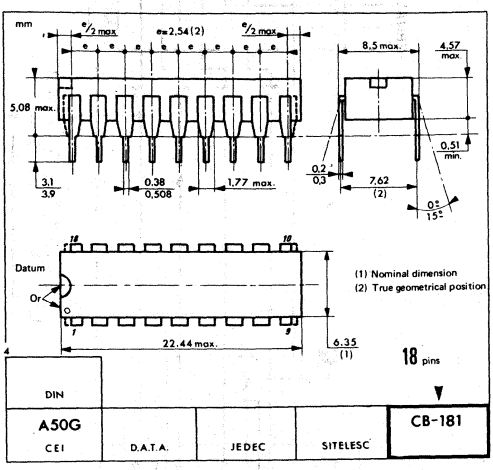
- Above given output load values are minimum values, in case of all output loading.
- Minimum output load is 150 Ω individually, provided that total supply current is less than 150 mA.

PHYSICAL DIMENSIONS

CB-181



PLASTIC PACKAGE



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THOMSON COMPONENTS SEMICONDUCTEURS

TEA5116

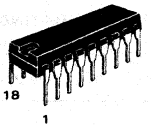
5 SWITCHES FOR VIDEO AND RGB SELECTION

ADVANCE INFORMATION

- This IC allows to select one of two channels of 5 video signals : RGB, Fast Blanking and synchronizing or video signal (S).
- Each channel has 6 dB gain.
- R, G, B and S signals are clamped to the same reference voltage on each input in order to have no differential voltage when switching.
- All input levels compatible with NFC 92250 and EN 50049 norms.
- 25 MHz band width for R, G, B signal.
- Internal 6.5 V shunt regulator
  - allows low impedance loads
  - limits power dissipation
- The five channels are simultaneously switched by only one select input.

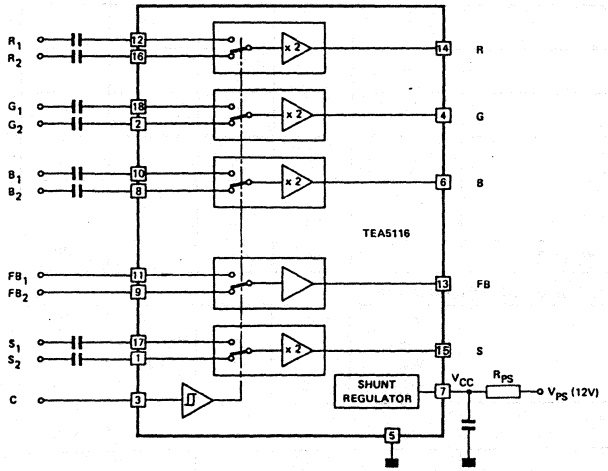
5 SWITCHES FOR VIDEO AND RGB SELECTION

CASE CB-181

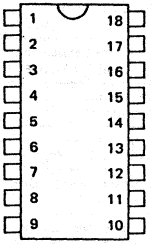


PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



1 - Synchro signal input 2
2 - Green signal input 2
3 - "C" select input
4 - Green signal output
5 - Ground
6 - Blue signal output
7 - Shunt regulator supply input
8 - Blue signal input 2
9 - Fast blanking input 2
10 - Blue signal input 1
11 - Fast blanking input 1
12 - Red signal input 1
13 - Fast blanking output
14 - Red signal output
15 - Synchro signal output
16 - Red signal input 2
17 - Synchro signal input 1
18 - Green signal input 1

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply current	I_{CC}	150	mA
Input voltage (all inputs)	V_{in}	-0.5 to $V_{CC}+0.5$	V
Operating temperature range	t_{oper}	0 to 70	°C
Junction temperature	T_j	-40 to $+150$	°C
Storage temperature	T_{stg}	-40 to $+150$	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th\ (j-a)}$	70	°C/W

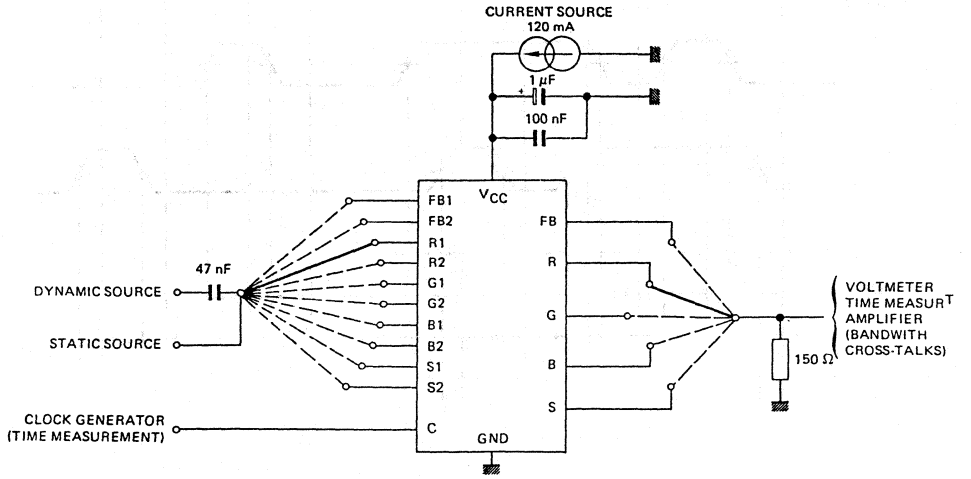
ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = +25°C$, $I_{CC} = 120$ mA
Load value = 150 Ω (sequentially switched)
} Unless otherwise specified, refer to test circuit page 3.

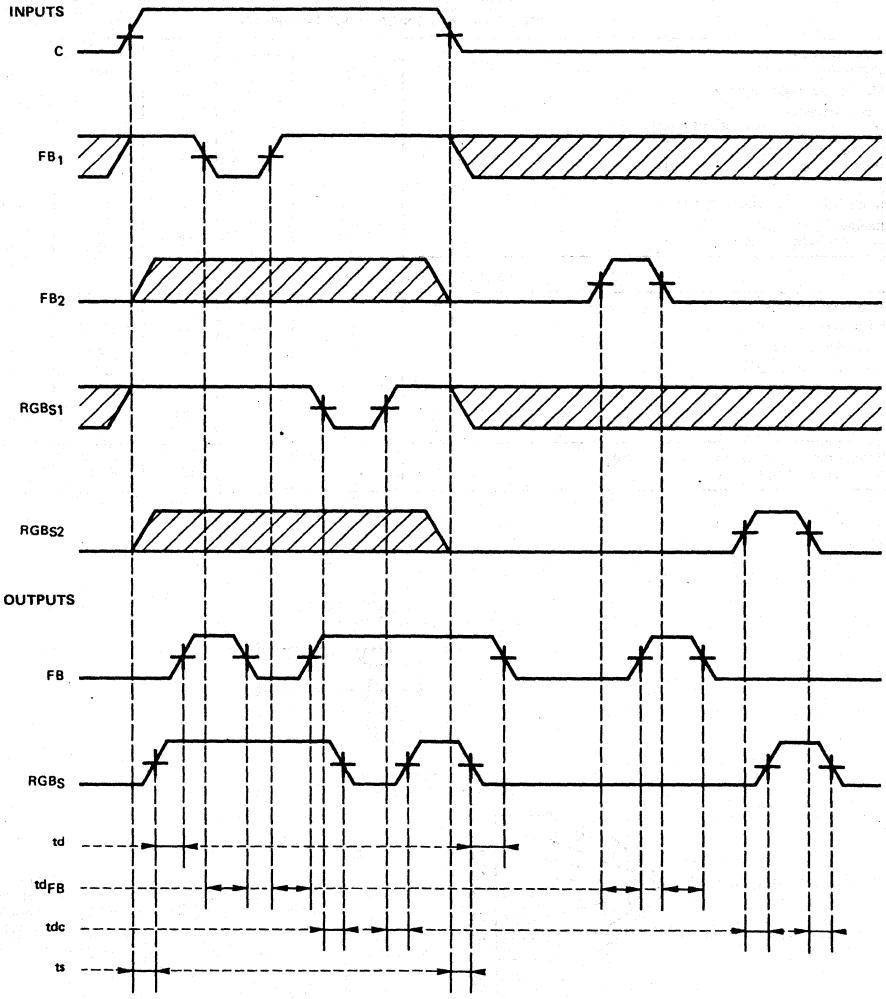
Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	6.3	6.5	7	V
R, G, B SWITCHES (Pins 4, 6, 14)					
DC output voltage (no input voltage)	V_C	–	1.2	1.5	V
Max output swing voltage	V_{AC}	2	2.5	–	Vpp
Bandwidth (– 3dB) (input voltage : 0.7 Vpp)	B	20	25	–	Mhz
Gain of each channel (input voltage: 0.7 Vpp, F = 1 MHz)	A_V	5.5	6	6.5	dB
Gain difference between any two R, G, B channels (input voltage: 0.7 Vpp, F = 1 MHz)	A_{dc}	–	0.1	0.5	dB
Input impedance (input voltage: 0.7 Vpp, F = 1 MHz)	Z_{ic}	–	10	–	kΩ
Output impedance (input voltage: 0.7 Vpp, F = 1 MHz)	Z_{oc}	–	10	–	Ω
Delay time between R, G, B inputs and R, G, B outputs (Δ inputs = 0.7 Vpp)	T_{dc}	–	50	–	nsec
Cross talk between any inputs (R1 and R2, or B1 and B2, or G1 and G2) (input voltage: 0.7 Vpp, F = 1 MHz)		50	–	–	dB
Cross talk between any outputs. (input voltage: 0.7 Vpp, F = 1 MHz)		50	–	–	dB
FAST BLANKING SWITCH (Pin 13)					
Low level input voltage	V_{IL}	-0.5	–	0.4	V
High level input voltage	V_{IH}	1	–	$V_{CC}+0.5$	V
Low level output voltage	V_{OL}		–	0.8	V
High level output voltage	V_{OH}	1.8	–	3.5	V
Delay time between R, G, B, S outputs and FB output (C signal switching)	t_d	–	30	–	nsec
Delay time between FB inputs and FB output (FB pulse input amplitude: 2 V)	t_d FB	–	130	–	nsec

ELECTRICAL OPERATING CHARACTERISTICS (Cont'd).

Characteristic	Symbol	Min	Typ	Max	Unit
VIDEO (or synchro.) SIGNAL SWITCH (Pin15)					
DC output voltage (no input voltage)	V_S	–	1.2	1.5	V
Max output swing voltage		2.6	–	–	Vpp
Input impedance (input voltage : 1 Vpp, F = 1 MHz)		–	10	–	kΩ
Output impedance (input voltage : 1 Vpp, F = 1 MHz)		–	10	–	Ω
Gain (input voltage : 1 Vpp, F = 1 MHz)		5.5	6	6.5	dB
Bandwidth (– 3 dB) (input voltage : 1 Vpp)		15	20	–	MHz
SELECT INPUT "C" (Pin3)					
Low level input voltage	V_{IL}	– 0.5	–	1	V
High level input voltage	V_{IH}	2	–	V_{CC} + 0.5	V
Low level input current	I_{IL}	– 0.8	–	– 0.1	mA
High level input current (V_{IH} = 3 V)	I_{IH}			0.5	mA
Switching time between C input signal and S output signal (C pulse amplitude : 3 V)	t_s	–	100	–	nsec
Delay time between S input and S output (Δ input: 0.7 Vpp)	t_{dc}	–	50	–	nsec

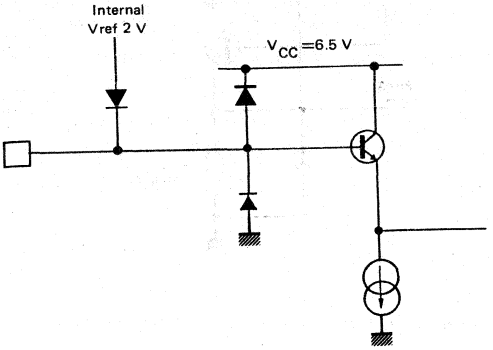


TEST CIRCUIT

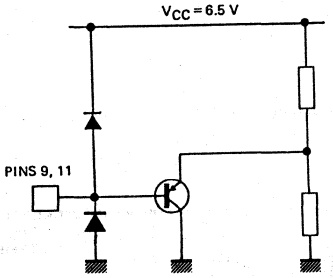

INPUTS
C
FB1
FB2
RGBS1
RGBS2
OUTPUTS
FB
RGBS
td
tdFB
tdc
ts

INPUTS/ OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

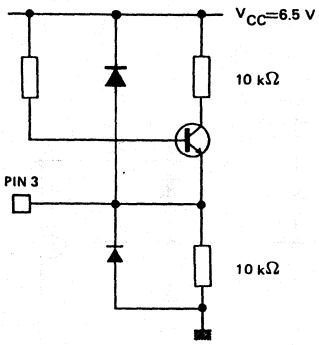
- R, G, B, S inputs (pins 1, 2, 8, 10, 12, 16, 17, 18)



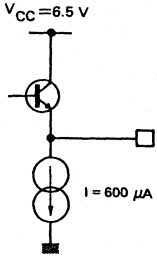
- FB inputs (pins 9, 11)



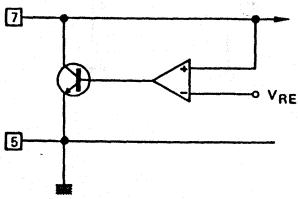
●C input (pin 3)



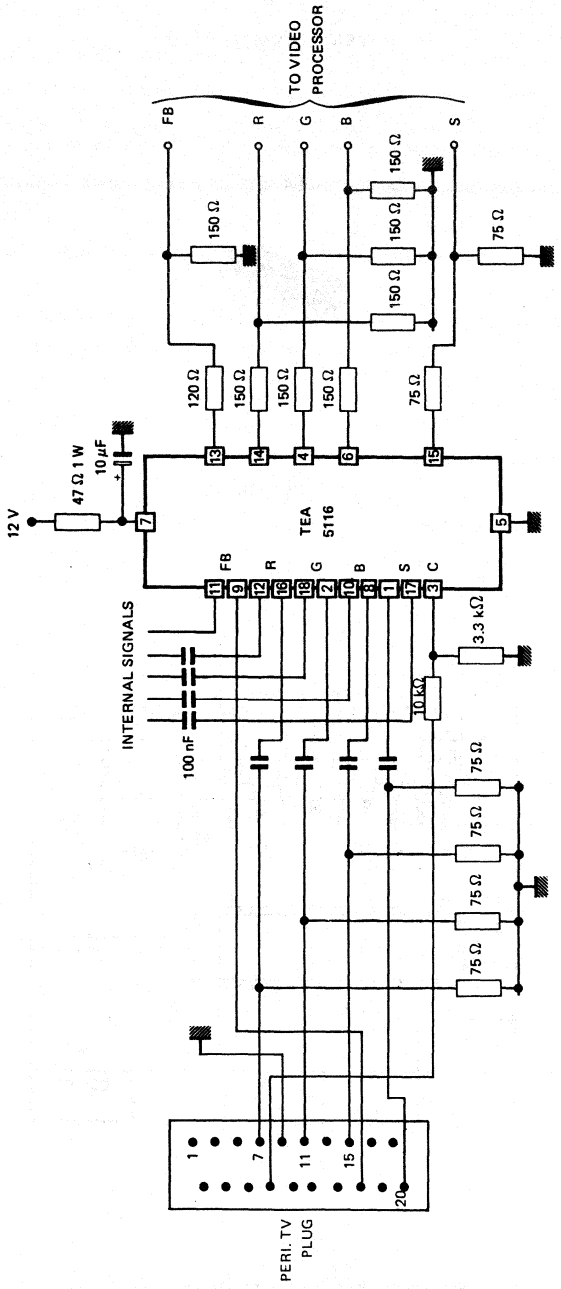
●All outputs (Pins 4, 6, 13, 14, 15)



● I_{CC} supply (Shunt transistor regulation system) (pin 7)



Refer to application diagram page 7

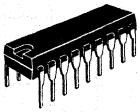


TYPICAL APPLICATION DIAGRAM

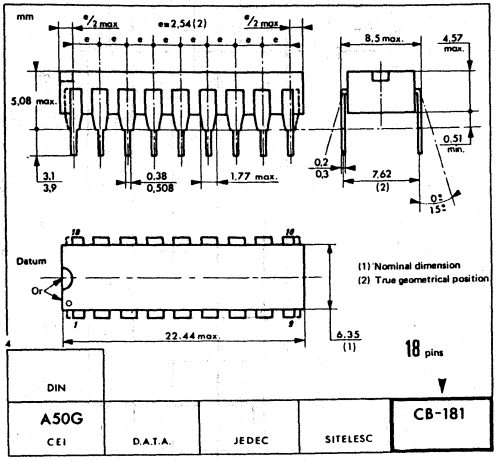
- Above given output load values are minimum values, in case of all output loading.
- Minimum output load is 150 Ω individually, provided that total supply current is less than 150 mA.

PHYSICAL DIMENSIONS

CB-181



PLASTIC PACKAGE



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THOMSON COMPONENTS SEMICONDUCTEURS

UAA4000

REMOTE CONTROL TRANSMITTER

The UAA4000 is an easily expandable, 32 command, pulse position modulation transmitter drawing zero standby current.

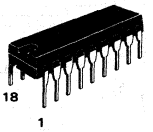
- Ultrasonic or infra-red transmission
- Direct drive for ultrasonic transducer
- Direct drive of visible LED when using infra-red
- Very low power requirements
- Pulse position modulation gives excellent immunity from noise and multipath reflections
- Single pole key matrix
- Switch resistance up to 1 kΩ tolerated
- Few external components
- Anti-bounce circuitry on chip.

Quick reference data

- Power supply : 9 V, standby 6 μA, operating 8 mA
- Modulation : pulse position with or without carrier
- Coding : 5 bits word giving a primary command set of 32 commands
- Key entry : 8 x 4 single pole key matrix
- Date rate : selectable 1 bit/sec to 10 k bit/sec
- Carrier frequency : selectable 0 Hz (no carrier) to 200 kHz

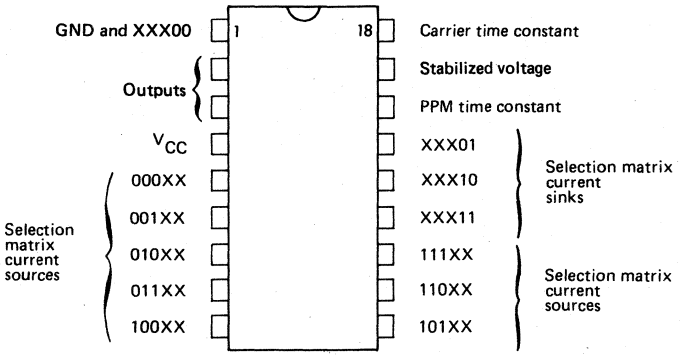
REMOTE CONTROL TRANSMITTER

CASE CB-181



PLASTIC PACKAGE

PIN CONFIGURATION



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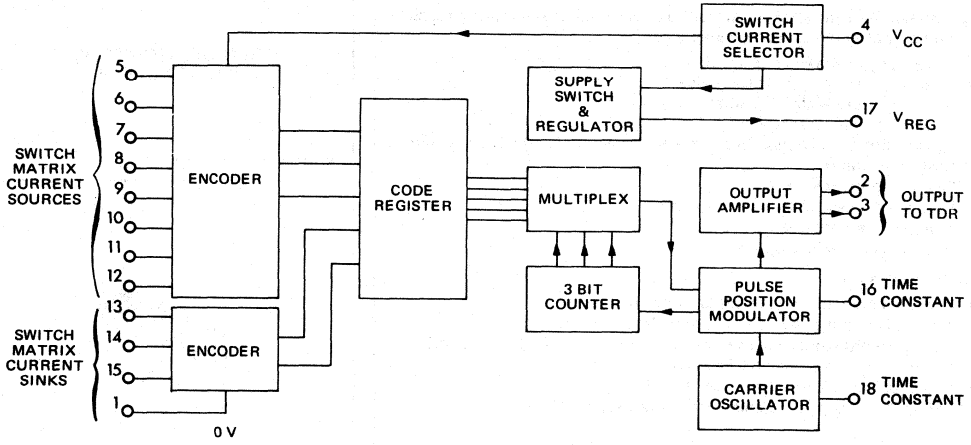
BLOCK DIAGRAM



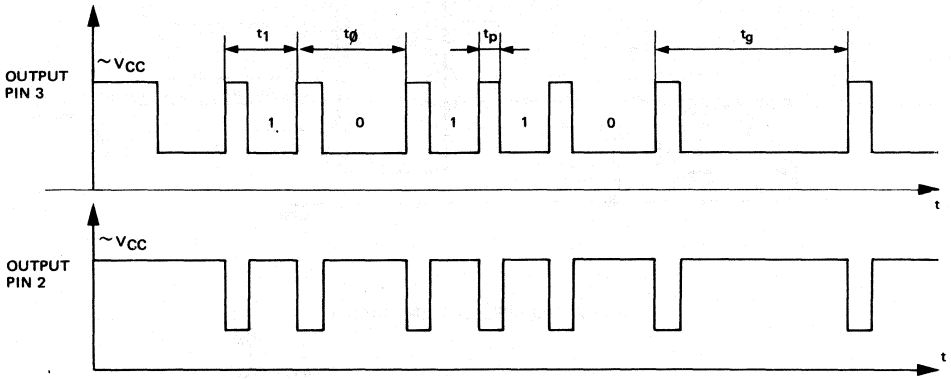
MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply voltage	pin 4	V_{CC}	11	V
Maximum power dissipation		P_{tot}	600	mW
Maximum output current	Pin 3	I_C	5	mA
Operating temperature range		t_{oper}	−10 to+ 65	°C
Storage temperature range		t_{stg}	−55 to+ 125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	70	°C/W

OUTPUT WAVEFORMS (PPM WORD NOTATION)



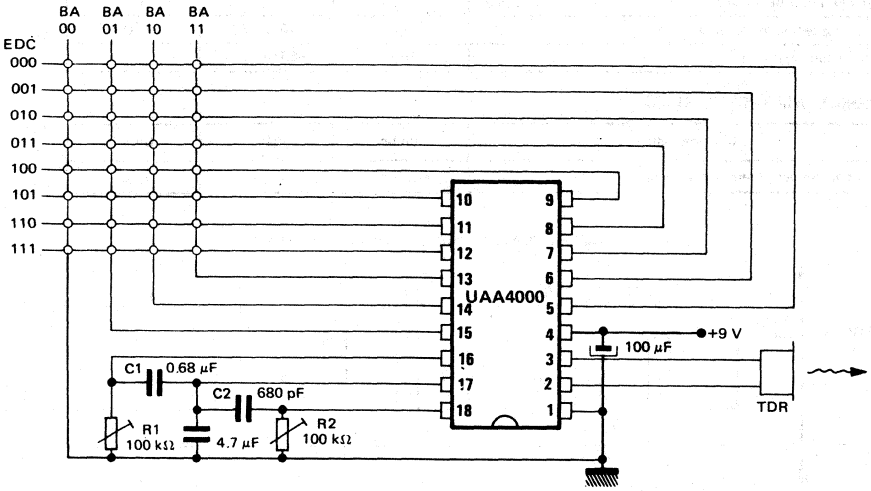
ELECTRICAL OPERATING CHARACTERISTICS (see test circuit next page)

T_{amb}= 25°C, V_{CC} = 9 V, f_o = 40 kHz, t_1 = 18 ms
4.7 µF capacitor on pin 17 (Unless otherwise specified)

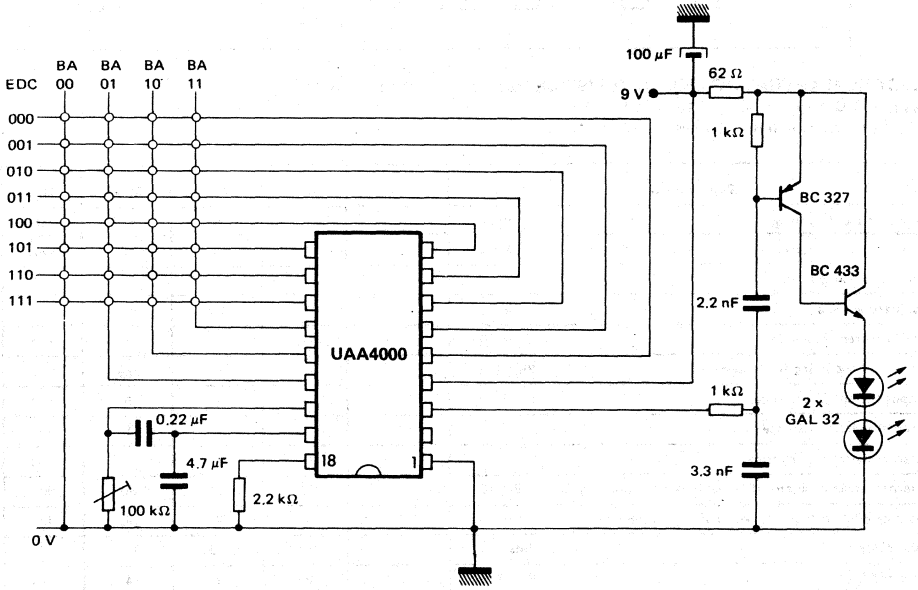
Characteristic		Symbol	Min	Typ	Max	Unit
Operating supply voltage	Pin 4	V_{CC}	7	9	11	V
Operating supply current	Pin 4		–	8	16	mA
Standby supply current	Pin 4		–	–	30	µA
Stabilized voltage	Pin 17		3.9	4.2	4.5	V
Output current available	Pin 17		–	–	1	mA
Output voltage swing (Unloaded)	Pins 2, 3		–	8	V_{CC}	V
Output current (Peak value)	Pins 2, 3		–	–	5	mA
External switch resistance			–	–	1	kΩ
External switch closing time			6	–	–	ms
External carrier oscillator (R2 required, C_2 = 680 pF)	Pin 18		20	40	80	kΩ
External PPM resistor (R1 required, C_1 = 0.68 µF)	Pin 16		15	30	60	kΩ
Ratio t0/t1	Pins 2, 3		1.4	1.5	1.6	
Pulse width	Pins 2, 3	t_p	2	3	4	ms
Inter-word gap	Pins 2, 3	t_g	50	54	58	ms

APPLICATION CIRCUITS

TEST AND ULTRASONIC APPLICATION CIRCUIT

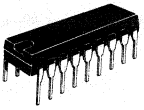


INFRA-RED APPLICATION CIRCUIT

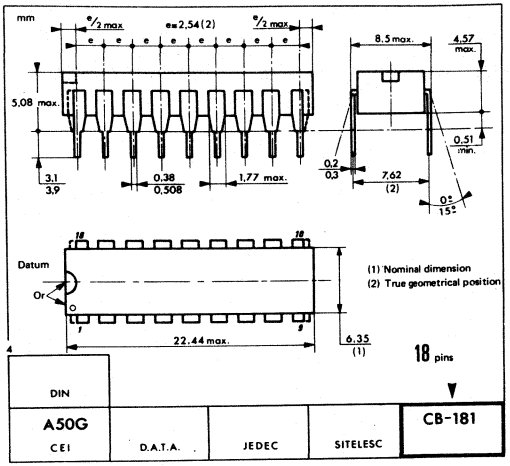


PHYSICAL DIMENSIONS

CB-181



PLASTIC PACKAGE



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NOTES

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THOMSON COMPONENTS MICONDUCTEURS

UAA4000S

REMOTE CONTROL TRANSMITTER

The UAA4000S is an easily expandable, 32 command, pulse position modulation transmitter drawing zero standby current.

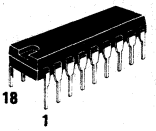
- Ultrasonic or infra-red transmission
- Direct drive for ultrasonic transducer
- Direct drive of visible LED when using infra-red
- Very low power requirements
- Pulse position modulation gives excellent immunity from noise and multipath reflections
- Single pole key matrix
- Switch resistance up to 1 kΩ tolerated
- Few external components
- Anti-bounce circuitry on chip.

Quick reference data

- Power supply : 9 V, standby 6 μA, operating 8 mA
- Modulation : pulse position with or without carrier
- Coding : 5 bits word giving a primary command set of 32 commands
- Key entry : 8 x 4 single pole key matrix
- Date rate : selectable 1 bit/sec to 10 k bit/sec
- Carrier frequency : selectable 0 Hz (no carrier) to 200 kHz

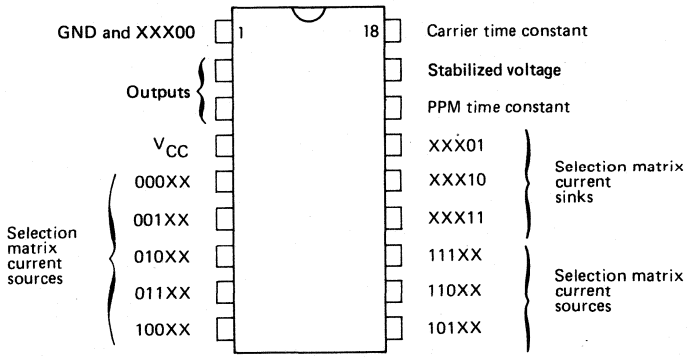
REMOTE CONTROL TRANSMITTER

CASE CB-181



PLASTIC PACKAGE

PIN ASSIGNMENT



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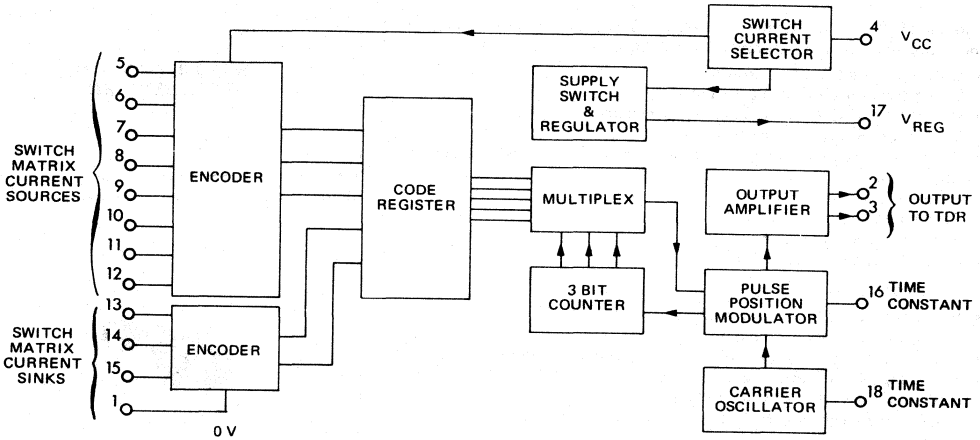
BLOCK DIAGRAM



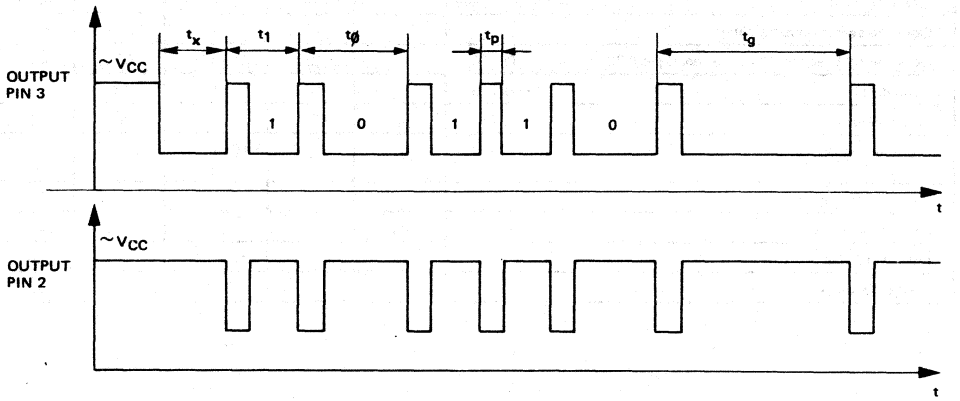
MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply voltage	pin 4	V_{CC}	11	V
Maximum power dissipation		P_{tot}	600	mW
Maximum output current	Pin 3	I_C	10	mA
Operating temperature range		t_{oper}	−10 to+ 65	°C
Storage temperature range		t_{stg}	−55 to+ 125	°C

THERMAL CHARACTERISTICS

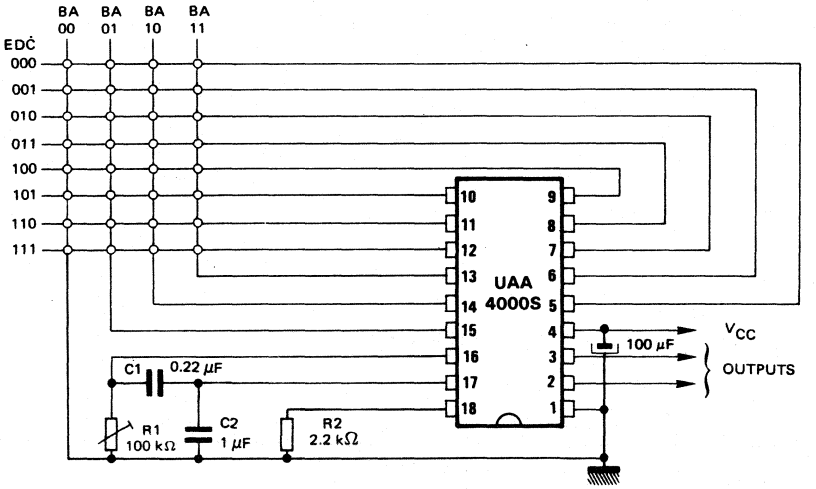
Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	70	°C/W

OUTPUT WAVEFORMS (PPM WORD NOTATION)



APPLICATION CIRCUIT.

TEST AND INFRA–RED APPLICATION CIRCUIT

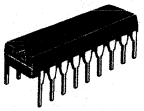


ELECTRICAL CHARACTERISTICS (See test circuit previous page)
T_{amb} = 25°C, V_{CC} = 6.5 to 11 V
1 µF capacitor on pin 17 (Unless otherwise specified).

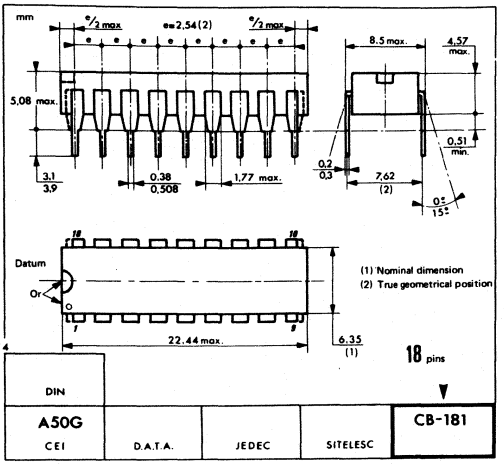
Characteristic		Symbol	Min	Typ	Max	Unit
Operating supply voltage	Pin 4	V_{CC}	6.5	9	11	V
Operating supply current (V_{CC} = 9 V)	Pin 4		—	8	16	mA
Standby supply current (V_{CC} = 9 V)	Pin 4		—	—	10	µA
Stabilized voltage	Pin 17		3.9	4.2	4.5	V
Output voltage swing (unloaded)	Pin 3		—	—	V_{CC}-0.1	V
Output current available	Pin 17		—	—	1	mA
Output current (V_{CEsat} = 1 V)	Pin 2 Pin 3		— —	— —	10 5	mA mA
External switch resistance ON OFF	Pins 5 to 15		 — —	 — —	 5 2	 kΩ MΩ
External switch closing time			6	—	—	ms
External PPM resistor (R_1 required, C_1 = 0.22 µF)	Pin 16		15	30	60	kΩ
Ratio tO/t1	Pins 2, 3		1.4	1.5	1.6	
Pulse width	Pins 2, 3	t_p	2	3	4	ms
Pre-pulse width	Pin 3	t_x	—	(2.15 to 2.33) x t_1	—	ms
Timing tolerance t_1			—	± 5	—	%
Jitter time of t_1		Δt_1	—	± 1	—	%
Inter-word gap		t_g	—	$3t_1 + \Delta t_1$	—	ms
Pre-pulse fall time			—	200	—	µs

PHYSICAL DIMENSIONS

CB-181



PLASTIC PACKAGE



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NOTES

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THOMSON COMPONENTS SEMICONDUCTEURS

UAA4009

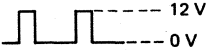
REMOTE CONTROL RECEIVER

UAA4009 is an I2L/BIPOLAR circuit for use as a receiver of remote control signals for television control applications.

This device :

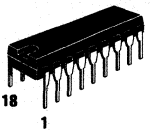
- receives 15 of the 32 codes transmitted by the UAA4000 (PPM),
- commutes tuning voltage for 12 TV channels,
- provides 0 to 6 V voltage (16 steps) for one electronic potentiometer,
- gives "stand-by" information.

MAIN FEATURES

- On-chip oscillator,
- Used with IR or ultrasonic transmission system,
- 5 bits PPM modulation, first transmitted must be zero,
- 2 successive codewords comparison,
- 12 channels set either by remote control or output pin grounding,
- Muting during channel change,
- Priority channel set by external capacitor,
- $V^+ = 12$ V
- $I^+ = 15$ mA
- PPM pulses :  12 V typ. / 0 V
- Channel output : open NPN collector with feed-back information.
- Stand-by output : open NPN collector
- V_{max}, output : 35 V.

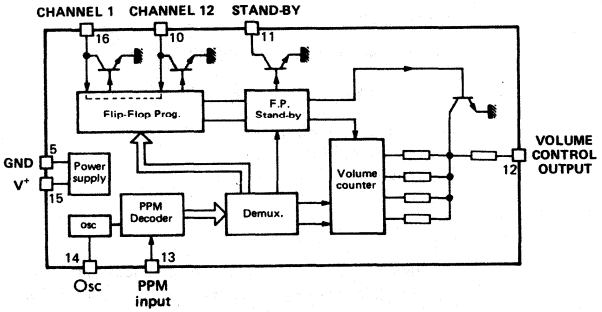
REMOTE CONTROL RECEIVER

CASE CB-225

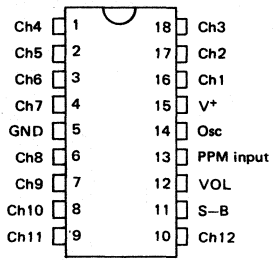


PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



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GENERAL DESCRIPTION

PPM DEMODULATION

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. Frequency is linked with transmission rate.
Following numerical values are given at f = 5.1 KHz.
For example, 5.1 KHz ensures potentiometer up or down travelling to be completed in about 5.5 s and channel 1 is set in 120 ms.

Each pulse that is received starts a counter. Input is masked for first 3.5 ms. Windows from 3.5 to 7 ms and from 7 to 13 ms determine whether a 1 or a 0 is present. Periods between pulses of 13 to 25.5 ms are recognised as word intervals.

Checks are made to ensure 5 bits are received for a word to be valid ; two consecutive and identical words allow corresponding function activation, 13 ms after receiving last pulse of the 2nd word (max 109 ms after first pulse of the first word).

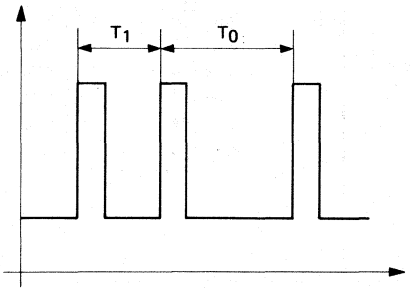
CODES

00001	Channel 1
00010	Channel 2
00011	Channel 3
00100	Channel 4
00101	Channel 5
00110	Channel 6
00111	Channel 7
01000	Channel 8
01001	Channel 9
01010	Channel 10
01011	Channel 11
01100	Channel 12
01101	Stand-by ON
01110	Volume UP
01111	Volume DOWN

NOTES : • 00001
1st last to be transmitted.

• Other codes are ignored.

PPM INPUT PULSES



CHANNELS

Channel activation is achieved either by remote control, or directly by momentary grounding corresponding pin of the circuit. This allows local push-switch control without external components.

Outputs : an open collector transistor grounds desired pin while others are high impedance (V_{max} = 35 V). The typical current grounded is 10 mA.

STAND-BY

S – B is activated (S – B ON) only by remote control ; it is disabled by activation of any channel either by remote control or front-panel switches.

S – B ON activates muting.

Output : Open collector S – B ON : high impedance
S – B OFF : grounded.

MUTING

During channel change or while S – B is on, volume is reduced to minimum by grounding external capacitor. When muting is released, volume goes back to previous value by charging capacitor with RC constant to be adjusted at desired value (R is 2 kΩ typ.).

VOLUME

A four bits binary counter drives a resistors array. It provides 0 to 6 V variation in 16 steps. Output impedance is 2 kΩ (50 Ω if muting is on).
Increment is inhibited when S – B is ON.

BEHAVIOUR AT START

When power is switched on :

- volume is preset at 0111 digital state, that is 2.8 V on volume output.
- channel with greatest capacity to the ground is activated.
  Ex. : on "typ. app. fig.", 2.2 nF have been connected to channel N.

OSCILLATOR

The minimum resistor value on pin 14 is 30 kΩ.

$T = C (160 R + 1660)$ for $V_{CC} = 12$ V.

T = oscillator period (μs)
C = capacitance (μF)
R = resistance (KΩ).

NB :

- When S – B is ON, 33 V tuning voltage must keep present. Otherwise all outputs are going to ground and consequently S – B is disabled.
- V^+ 12 V must be present to ensure output can accept 33 V.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	10 ⟶ 15	V
Voltage on "channel off" pins	V_{CHoff}	35	V
Current on "channel on" pins	I_{CHon}	20	mA
PPM input high voltage	V_{in}	20	V
Stand-by on voltage	V_{SBon}	15	V
Stand-by off current	I_{SBoff}	2	mA
Volume output current (available)	I_{VOL}	2	mA
Operating ambient temperature	T_{oper}	0+ 70	°C
Max power dissipation	P_{tot}	500	mW

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	70	°C/W

ELECTRICAL CHARACTERISTICS V_{CC} = 12 V ; T_{amb} = + 25°C (unless otherwise noted)

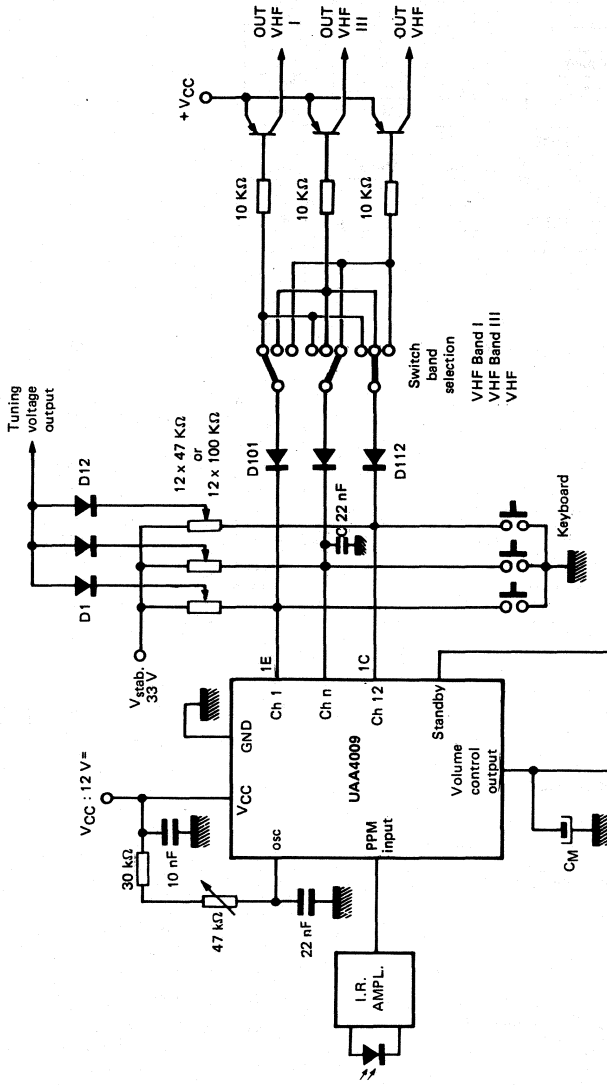
Characteristic	Symbol	Min	Typ	Max	Unit
Supply current	I_{CC}	10	15	30	mA
Voltage on "channel off" pins	V_{CHoff}	–	33	35	V
Current on "channel off" pins (V_{CHoff} = 33 V)	I_{CHoff}	–	–	1	µA
Voltage on "channel on" pins (I_{CHon} = 10 mA)	V_{CHon}	–	50	80	mV
Current on "channel on" pins	I_{CHon}	–	10	20	mA
Temperature coefficient	$\frac{\Delta V_{CHon}}{\Delta \theta}$	–	150	300	µV/°C
PPM input low voltage	V_{in}	–	0 to 3	–	V
PPM input low current (V_{in} = 0 V)	I_{in}	–	–30	–	µA
PPM input high voltage	V_{in}	–	5	20	V
PPM input high current (V_{in} = V_{CC} = 12 V)	I_{in}	–	2	–	µA
Stand-by on voltage	V_{SBon}	–	V_{CC}	15	V
Stand-by on current (V_{SBon} = 12 V)	I_{SBon}	–	–	1	µA
Stand-by off voltage (at I_{SBoff} = 1 mA)	V_{SBoff}	–	–	0.15	V
Stand-by off current	I_{SBoff}	–	1	2	mA
Volume voltage swing (unloaded)	ΔV_{VOL}	4.9	6	7	V
Volume voltage (step zero)	V_{VOL}	–	50	100	mV
Starting volume voltage	V_{VOLst}	–	2.8	–	V
Volume output impedance (S - B off)	R_{OUTvol}	1.4	2	2.6	kΩ
(S - B on)	R_{OUTVOL}	35	50	65	Ω
Volume output current (available)	I_{VOL}	–	–	2	mA
Temp. coefficient volume-voltage (Load= 20 kΩ)	$\frac{\Delta V_{VOL}}{\Delta \theta}$	–	2	–	mV/°C
V_{CC} ripple rejection (50⟶100 Hz)	–	30	40	–	dB
Oscillator frequency	F_{osc}	0.5	5.1	10	KHz
Optimum oscillator adjustment with UAA4000 transmitter	T*	–	1/29	–	t"1" transmitted
Input pulse width	–	10	–	–	µs
PPM window for "1"	t"1"	19.5	–	34.5	T*
for "0"	t"0"	35.5	–	66.5	T*
for "synchro"	t"s"	67.5	–	130.5	T*
Oscillator max allowable dispersion (transmitter f_{osc}= cst)	f_{osc}	–	–	± 20	%
Channel change delay	T_{ch}	–	2 words+ 67 T*	–	–
Volume swing average delay	T_{VOL}	2.8	2.8 x 10^4 T*	–	s

EXTERNAL FORCED SWITCHING

External channel activating level	–	–	–	3.5	V
Minimum switching time	–	–	20	–	µs

T* : Receiver oscillator period at optimal frequency matching between transmitter and receiver.

TYPICAL APPLICATION

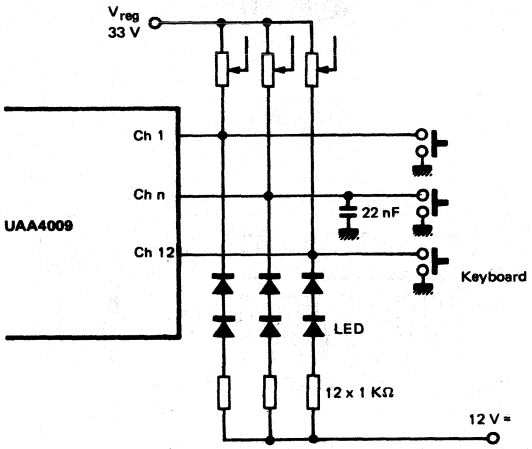


Remark : D1 to D12 must be polarised correctly.

C : Channel priority capacitor.
This capacitor must be present to ensure the channel stability.

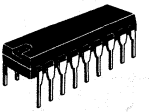
CM : Time constant 47 µF ⟶ 0.25!

APPLICATION WITH LED DISPLAY

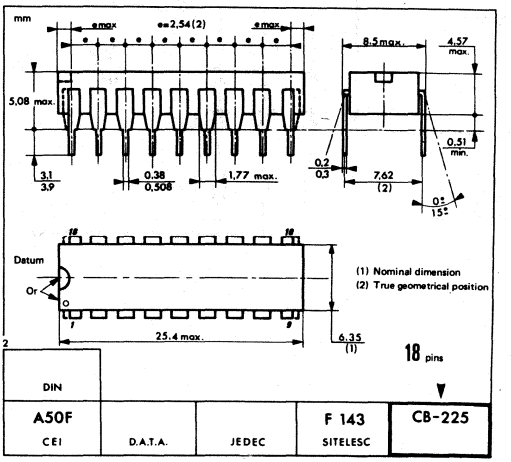


PHYSICAL DIMENSIONS

CB-225



PLASTIC PACKAGE



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Please inquire with our sales offices about the availability of the different packages

THOMSON COMPONENTS SEMICONDUCTEURS

TEA5049

INFRA-RED PREAMPLIFIER

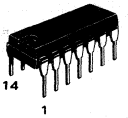
The TEA5049 is a low cost integrated infra-red preamplifier for remote control reception. It is intended for use in pulse carrier mode I_R transmission (400 kHz).

It incorportates:

- Integrated filters central frequency: 400 kHz
- External filter improvement ability
- Large amplification with AGC and noise reduction system
- Integrated monoflop pulse former
- Word recognition and voltage survey system
- Voltage reference

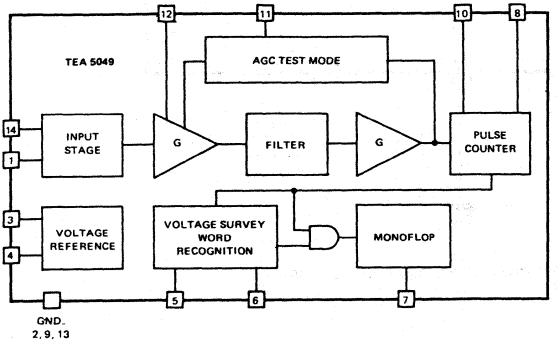
INFRA-RED PREAMPLIFIER

CASE CB2

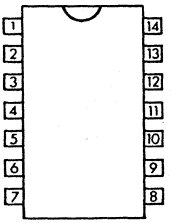


PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



1 - Input
2 - Ground
3 - Voltage reference
4 - V_{CC1}
5 - V_{CC2}
6 - Word recognition capacitor
7 - Open collector output

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC1}	6	V
Supply voltage	V_{CC2}	17	V
Power dissipation	P_{TOT}	100	mW

FILTERS SPECIFICATIONS

Characteristic	Symbol	Value	Unit
HIGH PASS FILTER (5 order Butterworth) Cut off frequency Dispersion	f_L	 250 ±30	kHz %
LOW PASS FILTER (3 order Butterworth) Cut off frequency Dispersion	f_H	 550 ±30	kHz %
Gain inside bandwidth (see figure 1)		15 to 25	dB

AGC (PIN 11)

Characteristic	Symbol	Value (typical)	Unit
AGC range		40	dB
AGC capacitor current discharge		0.5	µA
Output impedance when charging a capacitor		800	ohm

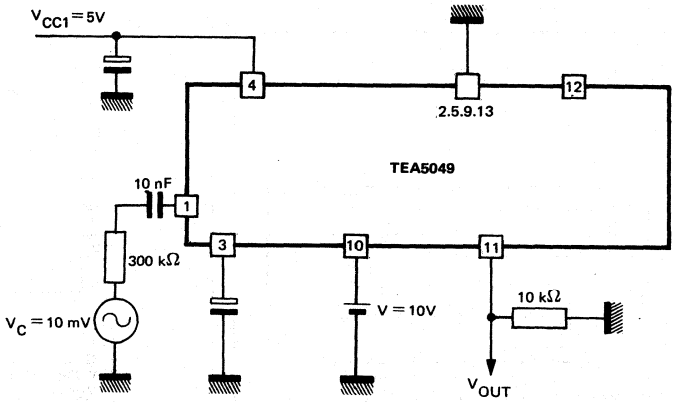


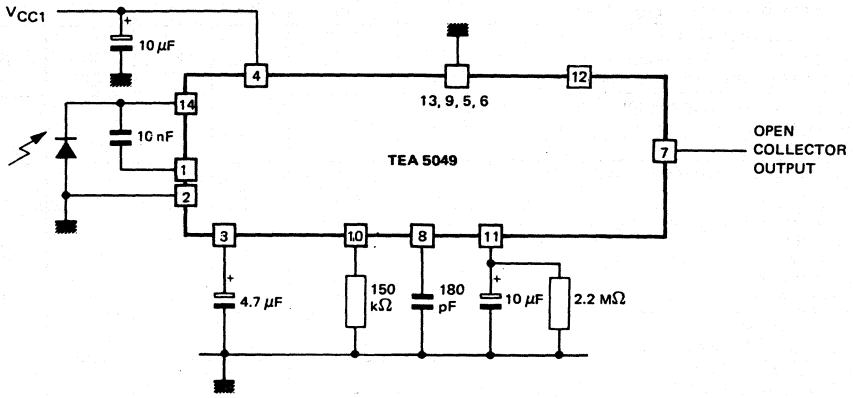
FIGURE 1 – TEST CONFIGURATION FOR FILTERS

ELECTRICAL OPERATING CHARACTERISTICS ($T_{amb} = +25°C$)

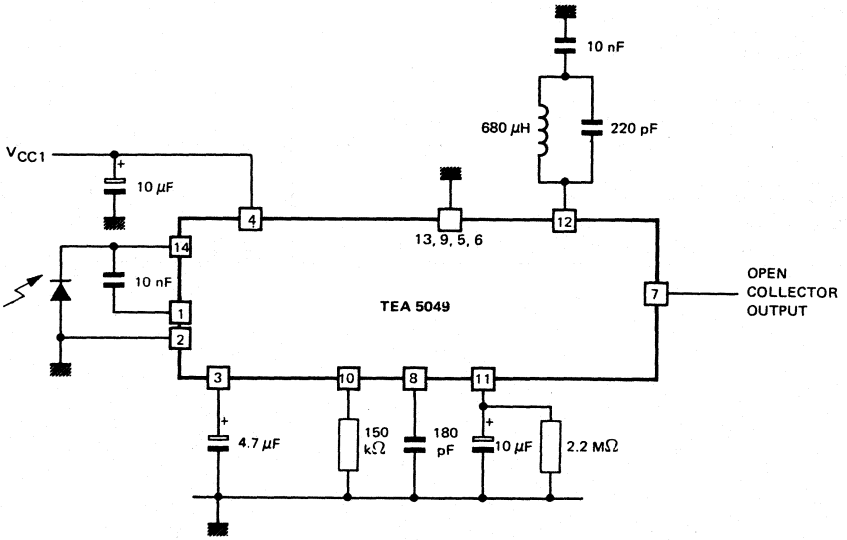
Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage (Pin 4) - ($V_{CC2} = 0$ V)	V_{CC1}	4.5	5	6	V
Supply current ($V_{CC2} = 0$ V)	I_{CC1}		2.5	3.5	mA
Supply voltage (Pin 5)	V_{CC2}			17	V
Supply current	I_{CC2}			3.5	mA
Supply voltage (pin 4) (7 V $\leqslant V_{CC2} \leqslant$ 17 V)	V_{CC1}	4.5	5.5	6	V
Pulse counter capacitor (Pin 8)					
Charge current ($V_{CC1} = 5$ V - $V_{CC2} = 0$ V)		20	25	35	µA
Activation level ($V_{CC1} = 5$ V - $V_{CC2} = 0$ V)		1.8	2	2.2	V
Current programming resistor (Pin 10)					
Output current					
($V_{CC1} = 5$ V - $V_{CC2} = 0$ V - $R_{ext} = 150$ kΩ)			25		µA
Pulse former output pulse duration (Pin 7)					
($V_{CC1} = 5$ V - $V_{CC2} = 0$ V)	T_S	30	60	90	µs
Word recognition capacitor (Pin 6) ($V_{CC2} \geqslant 11$ V)					
Charge current			300		µA
Discharge current			1.5		µA
High activation level	V_{WRH}		4.2		V
Low activation level	V_{WRL}		2.5		V
Reference voltage (Pin 3)	V_{ref}				
(4.5 V $\leqslant V_{CC1} \leqslant$ 6 V - $V_{CC2} = 0$ V)		3.7	3.85	4.1	V
Output signal (Pin 7)					
WORD RECOGNITION SYSTEM AND VOLTAGE SURVEY UNUSED (Pin 5 connected to ground)					
Saturation voltage during Pulse (Pin 7 connected to V_{CC1} by 3 kΩ resistor)	V_{CESAT}			1	V
Output voltage without infra red transmission (Pin 7 connected to V_{CC1} by 3 kΩ resistor)			V_{CC1}		V
Output signal (pin 7)					
WORD RECOGNITION SYSTEM AND VOLTAGE SURVEY USED					
Output voltage $V_{CC2} < 6$ V voltage on pin 6 (word recognition capacitor) $< W_{WRH}$ Pin 7 connected to V_{CC1} by 3 kΩ resistor.				1	V
Output voltage $V_{CC2} > 11$ V voltage on pin 6 $< W_{WRH}$ - Pin 7 connected to V_{CC1} by 3 kΩ resistor.				1	V
Output voltage between two pulses $V_{CC2} > V_{CC1}$ - voltage on pin 6 $> W_{WRH}$ - Pin 7 connected to V_{CC1} by 3 kΩ resistor			V_{CC1}		V
Output voltage. During pulses $V_{CC2} > 11$ V Voltage on pin 6 $> V_{WRH}$ - Pin 7 connected to V_{CC1} by 3 kΩ resistor.				1	V
Voltage Survey					
High activation level (Voltage on word recognition capacitor = V_{CC1})	VSH	9	10	11	V
Low activation level (Voltage on word recognition capacitor = V_{CC1})	V_{SL}	6.5	7	7.5	V

TYPICAL APPLICATIONS

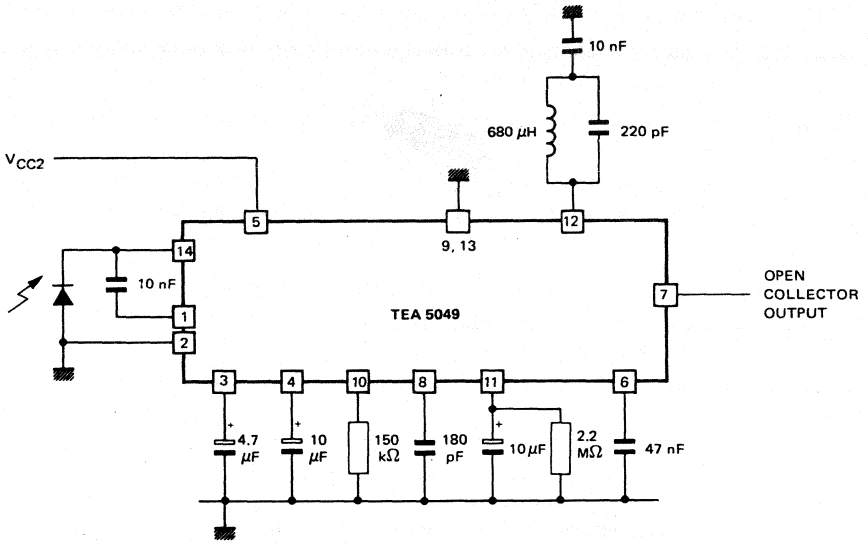
a) Minimum configuration (voltage - survey / word recognition system / additional filter } not used)



b) Configuration with external filter improvement (voltage survey / word recognition system } not used)

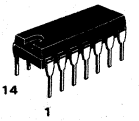


c) Voltage survey, word recognition and additional filter used

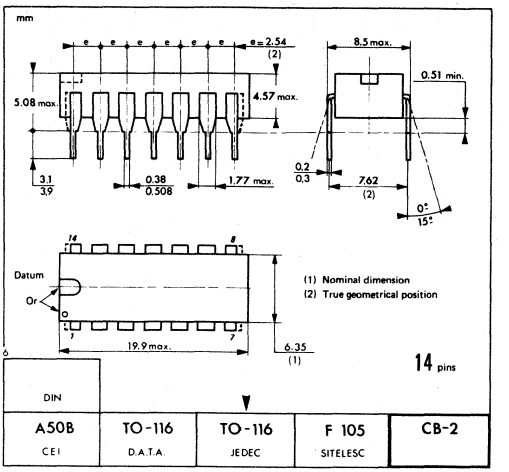


PHYSICAL DIMENSIONS

CB2



PLASTIC PACKAGE



DIN				
A50B CEI	TO-116 D.A.T.A.	TO-116 JEDEC	F 105 SITELESC	CB-2

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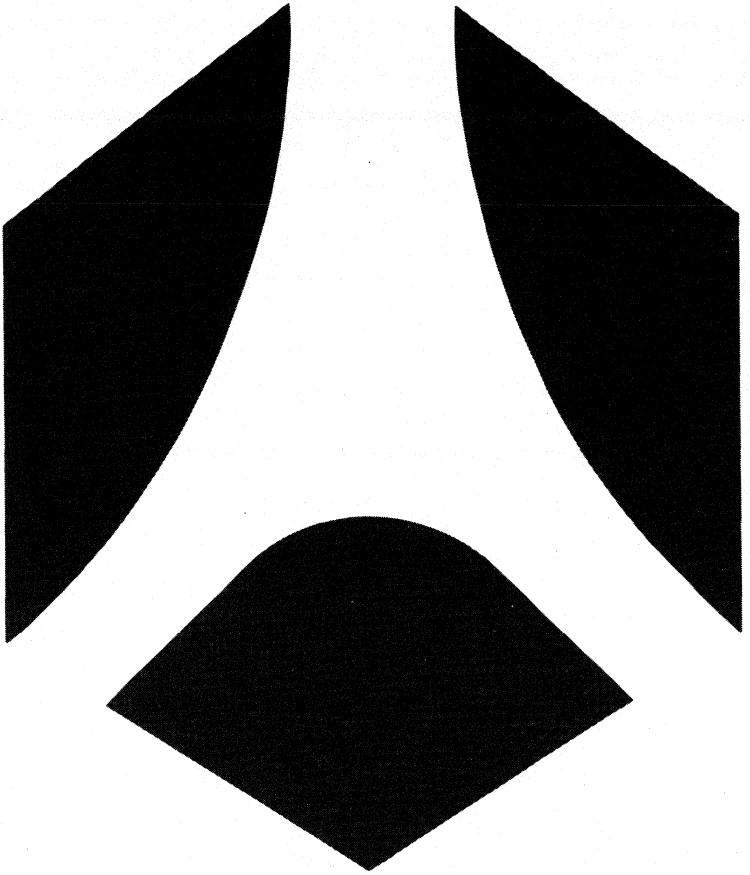
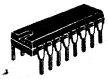


AF amplifiers

PERITELEVISION INTERFACE CIRCUIT

Application	Part number	MAX. VALUES		NOMINAL CONDITIONS			Note	Package	Page
		V_{CC}(V)	I_O(A)	V_{CC}(V)	R_L(Ω)	P_O(W)			
Radio and portable recorders	TBA820	16	1.5	9	8	1.2	—	DIL14	2-5
	TBA820M	16	1.5	9	8	1.2	—	DIL8	2-13
	TCA830SM	20	2	9	4	2	—		2-21
Portable radio dual AF amplifier	TEA2025B	15	1.5	9	4	2.3*	Fully protected	DIL16 	2-29
Car radio	TDA2003	18/40**	3.5	14.4	2	10	Fully protected		2-35
TV and record players	TDA2006	30	3	24	4	12	Fully protected		2-49
	TDA2030	36	3.5	28	4	18	Fully protected	SIL5	2-61
	TDA2030A42	42	3.5	28	4	18	Fully protected		2-75
Hi-Fi/Stereo TV receivers	TDA2040	40	4	32	4	22 d = 0.5%	Fully protected		2-89

* P_O (W) Output per channel except bridge applications (both amplifiers)
** Peak voltage (50 ms)

TBA820

AF AMPLIFIER

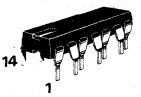
The TBA820 is a monolithic integrated audio power amplifier.
Its main features:
- working with supply voltages from 3 to 16 volts,
- low idle current (4 mA typ.),
- high efficiency,

make it especially suitable for mobile, battery operated equipments.
Other features include:
- output power up to 2W without any external heat sink,
- high input impedance, low bias current,
- high ripple rejection,
- no thermal runaway,
- no cross-over distortion,
- few external components required.

The TBA820 is supplied in a quad-in-line, 14 leads package.

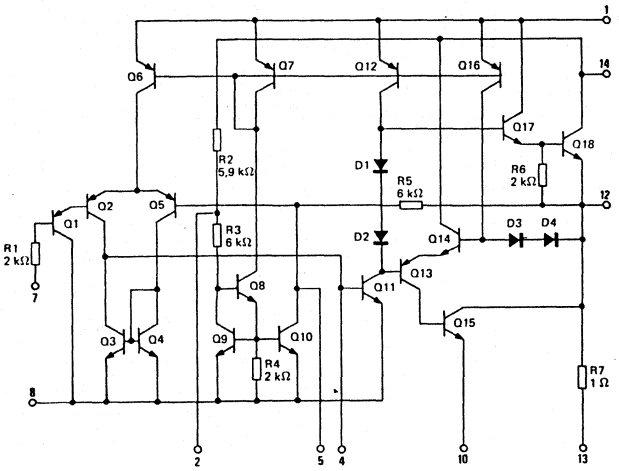
AF AMPLIFIER

CASE CB-21

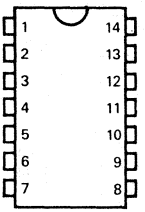


PLASTIC PACKAGE

SCHEMATIC DIAGRAM



PIN ASSIGNMENT



1 Bootstrap	**8** Ground (substrate)
2 Decoupling	**9** NC
3 NC	**10** Ground
4 Compensation	**11** NC
5 Feed-back network	**12** Output
6 NC	**13** Compensation
7 Input	**14** V_{CC}

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ABSOLUTE RATINGS (LIMITING VALUES)

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	16	V
Output peak current	I_O	1.5	A
Storage temperature	T_{stg}	− 40, + 150	°C
Junction temperature	Tj	+ 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C (note 1) (Unless otherwise stated)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	3	–	16	V
Quiescent output voltage Pin 12 V_{CC} = 9 V	V_O	4	4.5	5	V
Quiescent drain current V_{CC} = 9 V	I_{CC}	–	4		mA
Bias current Pin 7 V_{CC} = 9 V	I	–	0.1	–	µA
Output power V_{CC} = 12 V ; R_L = 8 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz V_{CC} = 9 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz V_{CC} = 6 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz V_{CC} = 3.5 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz	P_O	– – – – –	2 1.6 1.2 0.75 0.22	– – – – –	W
Input sensitivity V_{CC} = 9 V ; P_O = 1.2 W ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz V_{CC} = 9 V ; P_O = 1.2 W ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz V_{CC} = 9 V ; P_O = 50 mW ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz V_{CC} = 9 V ; P_O = 50 mW ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz	S	– – – –	16 60 3.5 12	– – – –	mV
Input resistance	R_I	–	5	–	MΩ
Frequency response (− 3 dB) V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C_B = 680 pF V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C_B = 220 pF	B		25 to 7.000 25 to 20.000		Hz
Distortion V_{CC} = 9 V ; P_O = 500 mW ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz V_{CC} = 9 V ; P_O = 500 mW ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz	d	– –	0.8 0.4	– –	%
Voltage gain (open loop) V_{CC} = 9 V ; R_L = 8 Ω ; f = 1 kHz	A_V	–	75	–	dB
Voltage gain (closed loop) V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz	A_V	– –	45 34	– –	dB
Input noise voltage V_{CC} = 9 V ; B (− 3 dB) = 25 to 20.000 Hz	V_n	–	3	–	μV_{eff}
Input noise current V_{CC} = 9 V ; B (− 3 dB) = 25 to 20.000 Hz	I_n	–	0.4	–	nA
Signal to noise ratio V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; R1 = 100 kΩ P_O = 1.2 W ; B (− 3 dB) = 25 to 20.000 Hz		–	70	–	dB
Supply voltage rejection (see fig. 2) V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C6 = 50 µF f (ripple) = 100 Hz	SVR	–	42	–	dB

Note 1 : The characteristics above were obtained using the circuit shown in fig. 1.

TEST AND APPLICATION CIRCUITS

FIGURE 1 – LOAD CONNECTED TO THE SUPPLY VOLTAGE

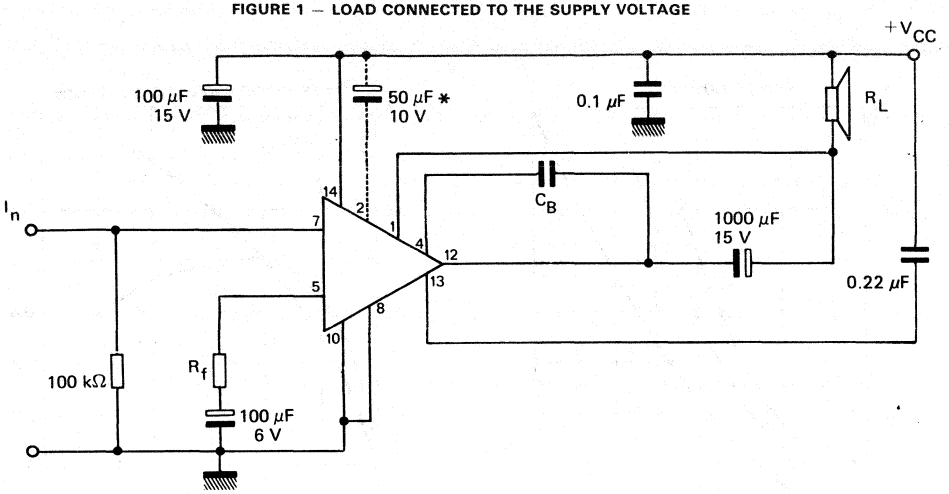
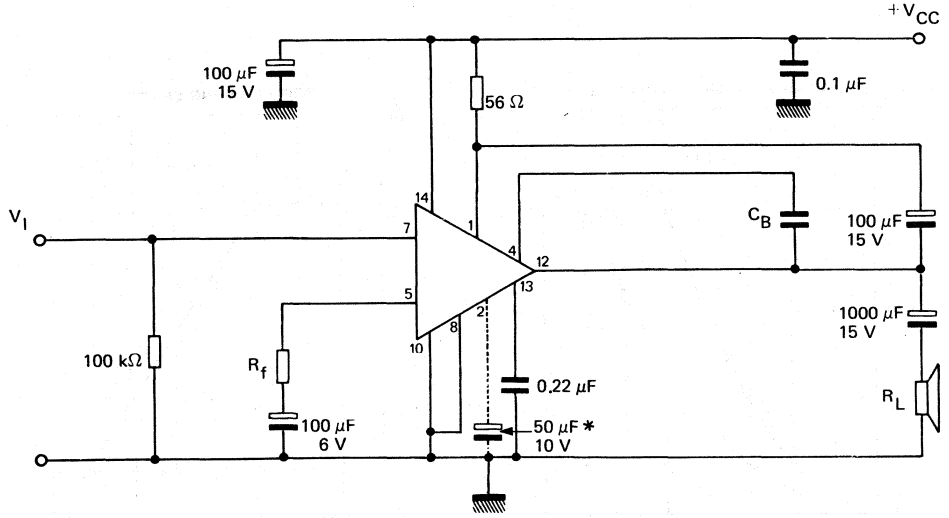
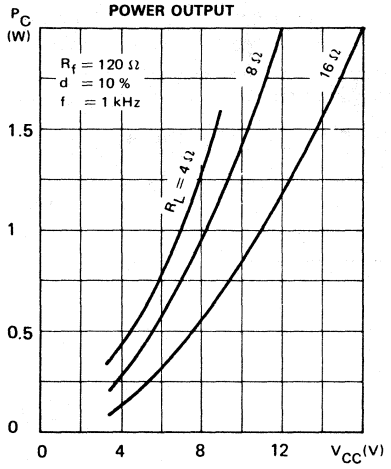


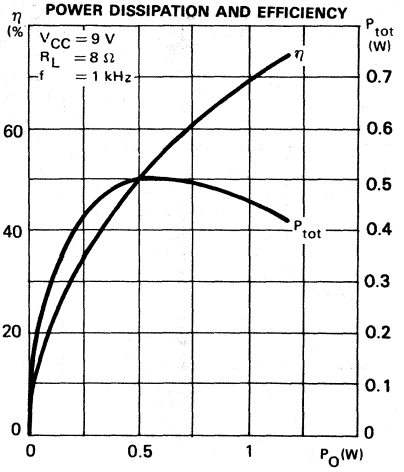
FIGURE 2 – LOAD CONNECTED TO GROUND

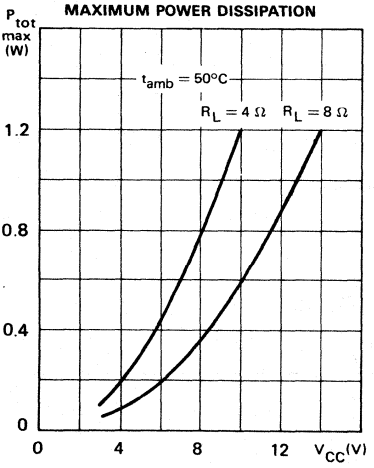


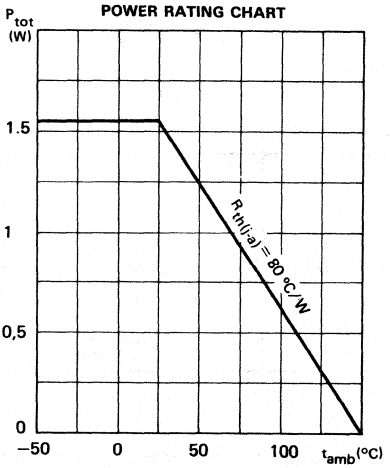
*C6 : Must be used when high ripple rejection is requested.

TYPICAL CHARACTERISTICS

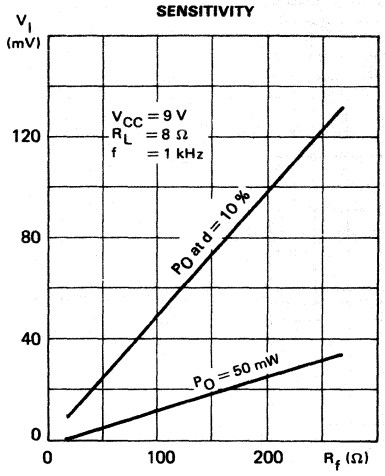


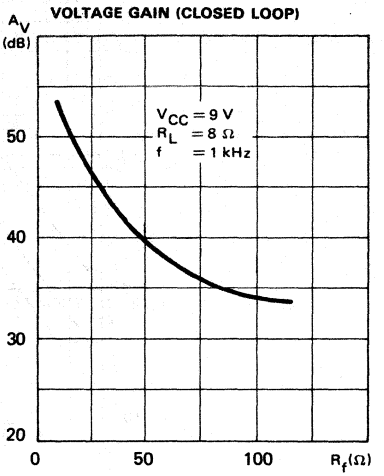


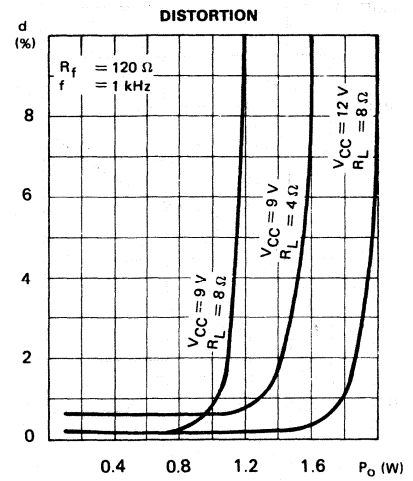


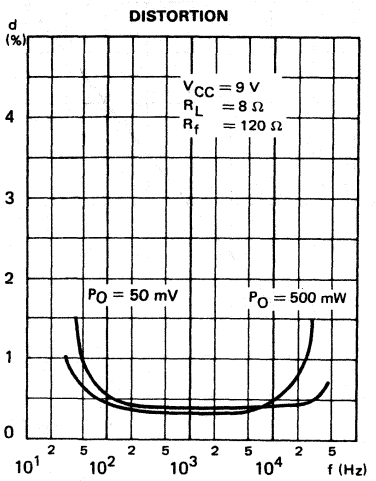


TYPICAL CHARACTERISTICS



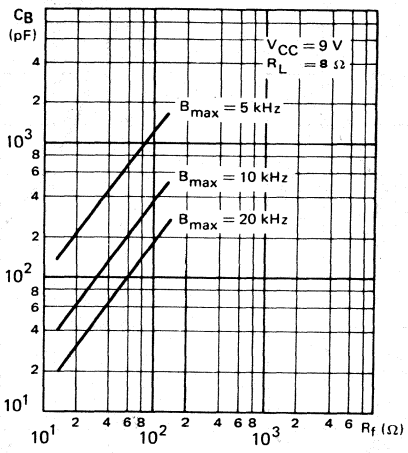




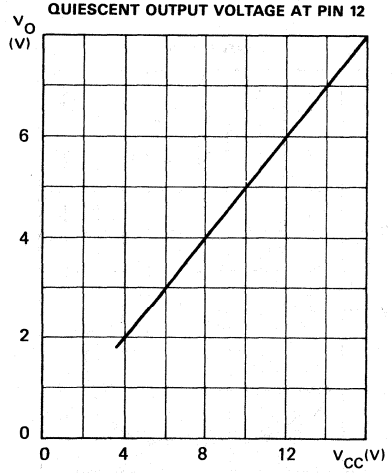


TYPICAL CHARACTERISTICS

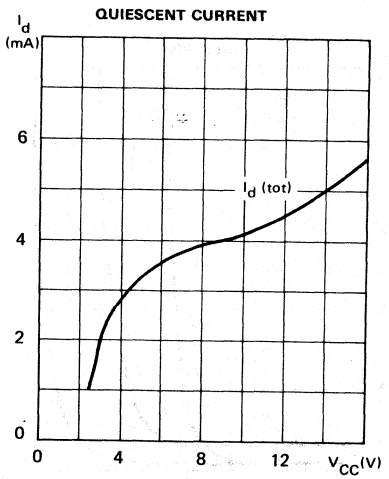
TYPICAL VALUE OF C_B VERSUS R_f AND B



QUIESCENT OUTPUT VOLTAGE AT PIN 12



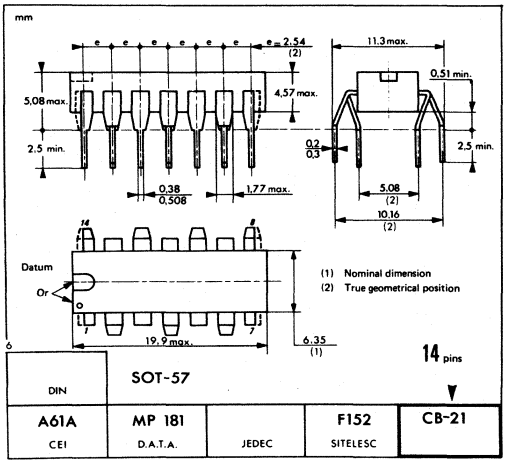
QUIESCENT CURRENT



PHYSICAL DIMENSIONS

CB-21

PLASTIC PACKAGE



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NOTES

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THOMSON COMPONENTS MICONDUCTEURS

TBA820M

AF AMPLIFIER

The TBA 820 M is a monolithic integrated audio power amplifier.
Its main features:

- working with supply voltages from 3 to 16 volts,
- low idle current (4 mA typ.),
- high efficiency,

make it especially suitable for mobile, battery operated equipments.
Other features include:

- output power up to 2 W without any external heat sink,
- high input impedance, low bias current,
- high ripple rejection,
- no thermal runaway,
- no cross-over distortion,
- few external components required.

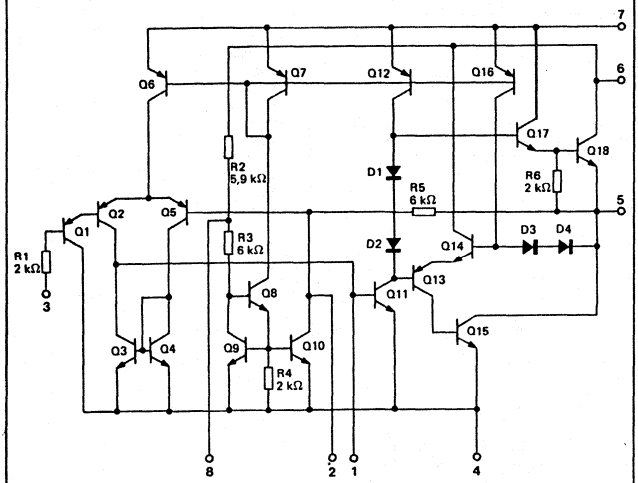
The TBA 820 M is supplied in a dual-in-line, 8 leads package.

AF AMPLIFIER

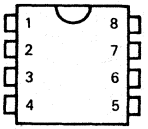
CASE CB-98

PLASTIC PACKAGE

SCHEMATIC DIAGRAM



PIN ASSIGNMENT



1 Compensation	**5** Output
2 Feedback	**6** Supply
3 Input	**7** Bootstrap
4 Ground	**8** Filtering

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	16	V
Output peak current	I_O	1.5	A
Storage temperature	T_{stg}	− 40 , + 150	°C
Junction temperature	Tj	+ 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C (note 1) (Unless otherwise stated)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	3	—	16	V
Quiescent output voltage Pin 5	V_O				V
V_{CC} = 9 V		4	4.5	5	
Quiescent drain current	I_{CC}				mA
V_{CC} = 9 V		—	4	12	
Bias current Pin 3	I				µA
V_{CC} = 9 V		—	0.1	—	
Output power measured at pin 5	P_O				W
V_{CC} = 12 V ; R_L = 8 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz		—	2	—	
V_{CC} = 9 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz		—	1.6	—	
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz		0.9	1.2	—	
V_{CC} = 6 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz		—	0.75	—	
V_{CC} = 3.5 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz		—	0.25	—	
Input sensitivity	S				mV
V_{CC} = 9 V ; P_O = 1.2 W ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz		—	16	—	
V_{CC} = 9 V ; P_O = 1.2 W ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz		—	60	—	
V_{CC} = 9 V ; P_O = 50 mW ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz		—	3.5	—	
V_{CC} = 9 V ; P_O = 50 mW ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz		—	12	—	
Input resistance	R_I	—	5	—	MΩ
Frequency response (− 3 dB)	B				Hz
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C_B = 680 pF			25 to 7.000		
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C_B = 220 pF			25 to 20.000		
Distortion	d				%
V_{CC} = 9 V ; P_O = 500 mW ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz		—	0.8	—	
V_{CC} = 9 V ; P_O = 500 mW ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz		—	0.4	—	
Voltage gain (open loop)	A_V				dB
V_{CC} = 9 V ; R_L = 8 Ω ; f = 1 kHz		—	75	—	
Voltage gain (closed loop)	A_V				dB
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz		—	45	—	
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz		—	34	—	
Input noise voltage	V_n				μV_{eff}
V_{CC} = 9 V ; B (− 3 dB) = 25 to 20.000 Hz		—	3	—	
Input noise current	I_n				nA
V_{CC} = 9 V ; B (− 3 dB) = 25 to 20.000 Hz		—	0.4	—	
Signal to noise ratio					dB
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; R1 = 100 kΩ P_O = 1.2 W ; B (− 3 dB) = 25 to 20.000 Hz		—	70	—	
Supply voltage rejection fig. 2	SVR				db
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C6 = 50 µF f (ripple) = 100 Hz		—	42	—	

Note 1 : The characteristics above were obtained using the circuit shown in fig. 1.

TEST AND APPLICATION CIRCUITS

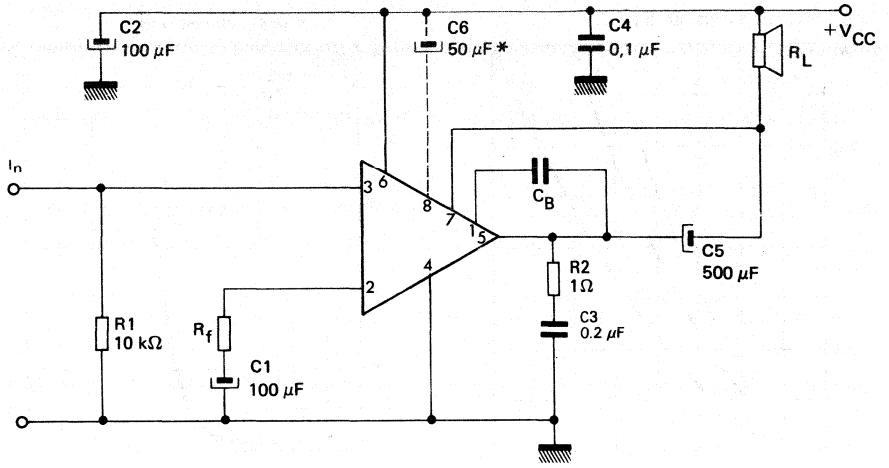


FIGURE 1 – LOAD CONNECTED TO THE SUPPLY VOLTAGE

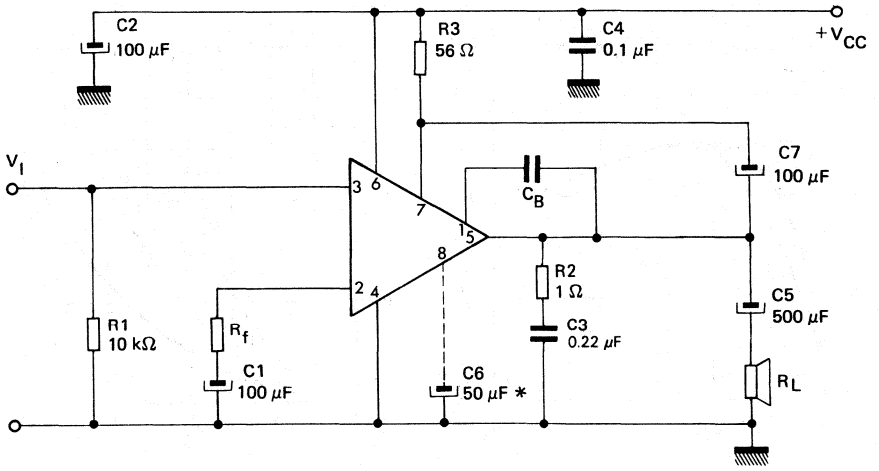


FIGURE 2 – LOAD CONNECTED TO GROUND

*Must be used when high ripple rejection is requested.

TYPICAL CHARACTERISTICS

FIGURE 3 – POWER OUTPUT

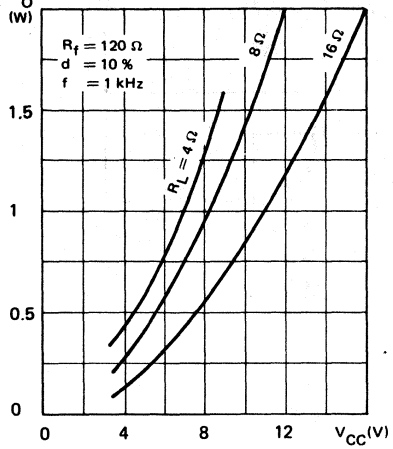


FIGURE 4 – DISTORTION

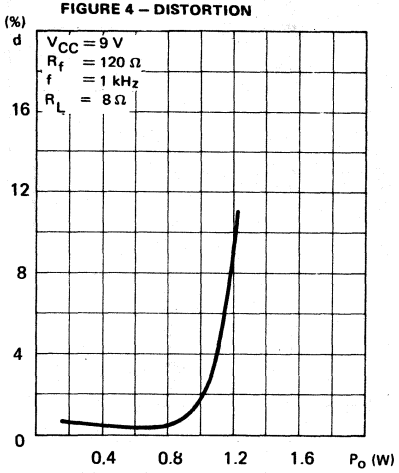


FIGURE 5 – POWER DISSIPATION AND EFFICIENCY

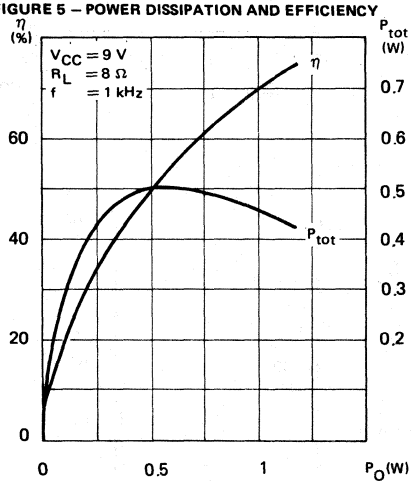
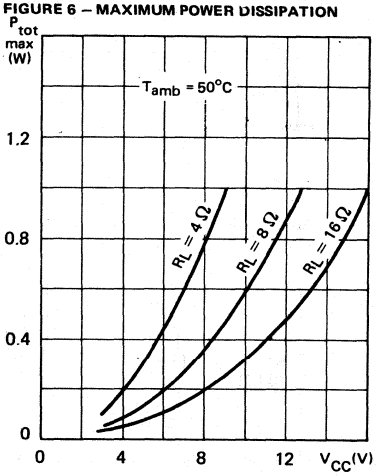


FIGURE 6 – MAXIMUM POWER DISSIPATION



TYPICAL CHARACTERISTICS

FIGURE 7 – TYPICAL VALUE OF C_B VERSUS R_f AND B

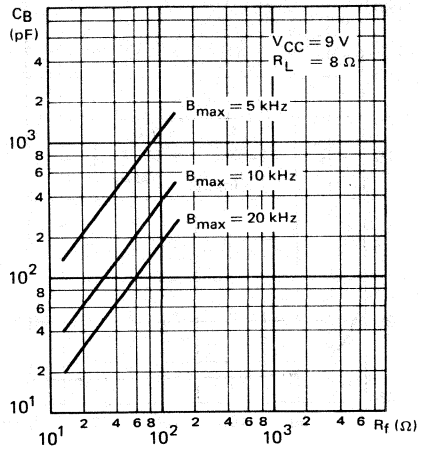


FIGURE 8 – RELATIVE FREQUENCY RESPONSE

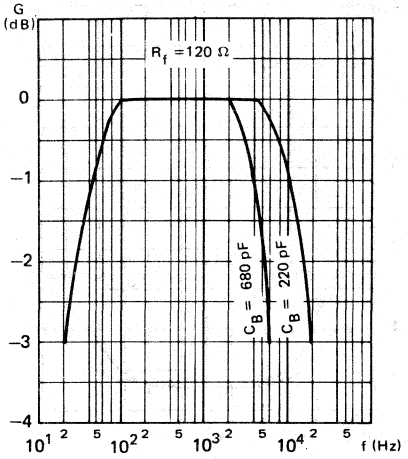


FIGURE 9 – SENSITIVITY

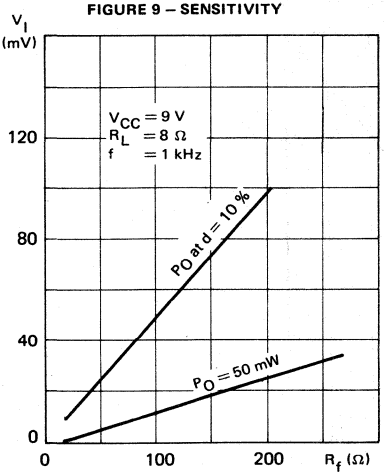
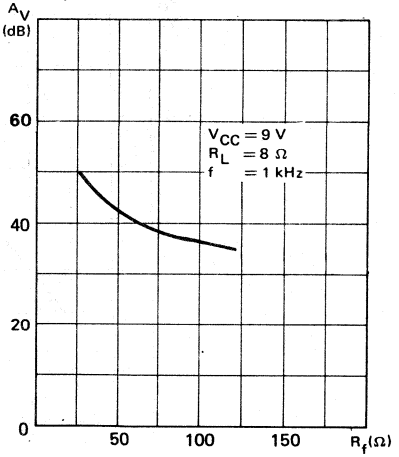


FIGURE 10 – VOLTAGE GAIN (CLOSED LOOP)



TYPICAL CHARACTERISTICS

FIGURE 11 – DISTORTION

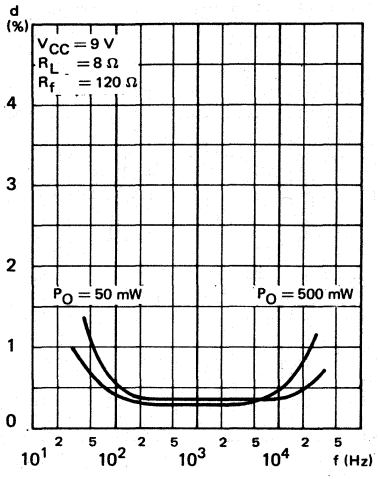


FIGURE 12 – SUPPLY VOLTAGE REJECTION (see figure 2)

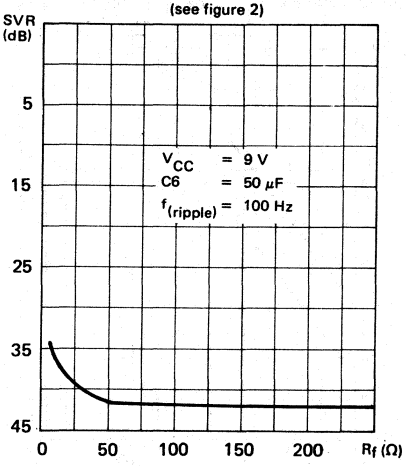
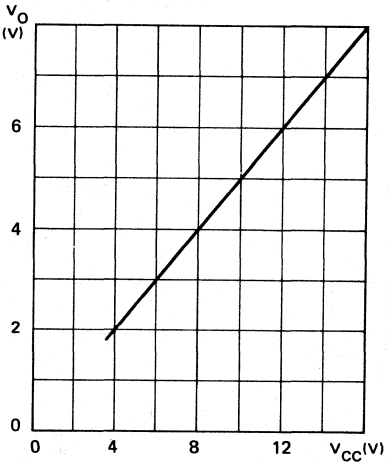


FIGURE 13 – QUIESCENT OUTPUT VOLTAGE AT PIN 5



TYPICAL CHARACTERISTICS

FIGURE 14 – QUIESCENT CURRENT

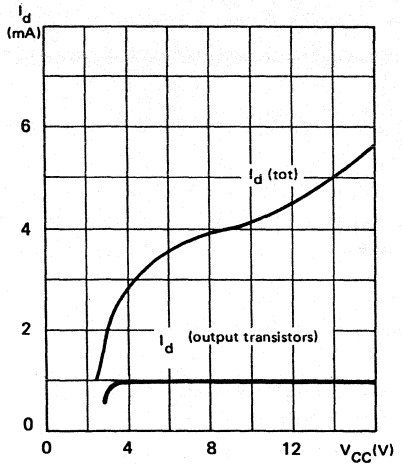


FIGURE 15 – POWER RATING CHART

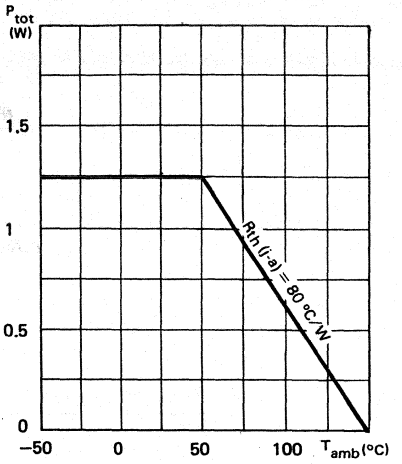
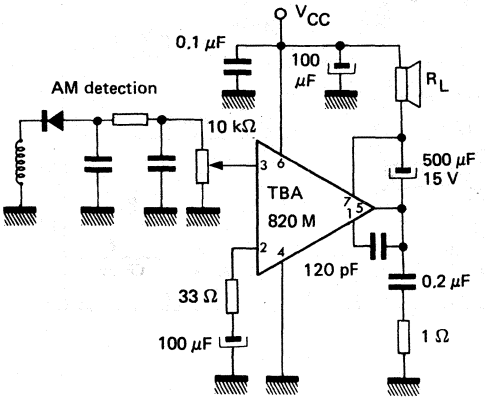


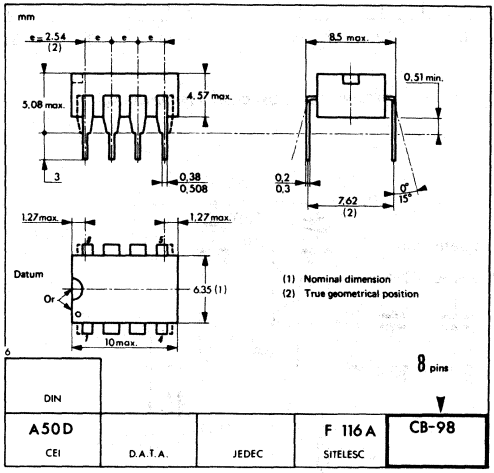
FIGURE 16 – LOW COST APPLICATION



PHYSICAL DIMENSIONS

CB-98

PLASTIC PACKAGE



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TCA 830SM
AF AMPLIFIER

The TCA 830SM is a monolithic integrated circuit designed for class B audio amplification, with up to 2.3 W output power ; it is internally protected against overheating.
It provides the advantages following :

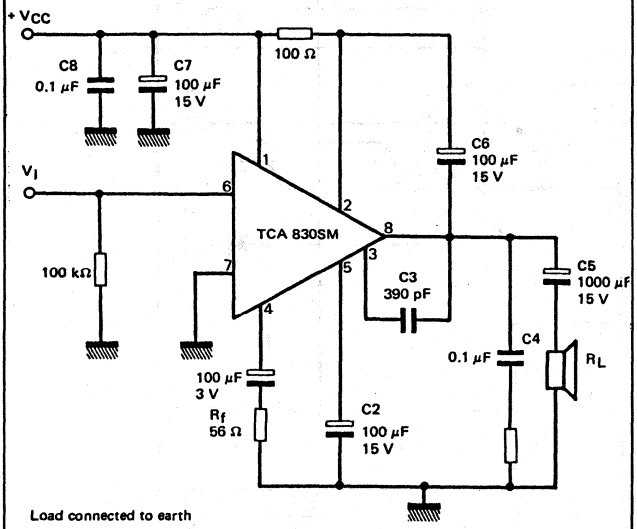
- The high idling current stability obtained from a built-in temperature and voltage-compensating network makes thermal runaway impossible.
- Open-loop gain is high enough to allow a great amount of feedback (low distortion) and keep a sufficient closed loop-gain (high sensitivity).
- The use of PNP transistors in the preamplifier allows D.C. input voltage to be zero.
- The exceptional D.C. output voltage stability and minimized potential loss, give to the output voltage high power capability.
- The minidip package makes it easy to use where limited space is available.
- Others highlights include : few external components and not any adjustment.

AF AMPLIFIER

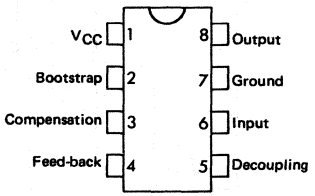
CASE CB-98

PLASTIC PACKAGE

TYPICAL APPLICATION



PIN ASSIGNMENT



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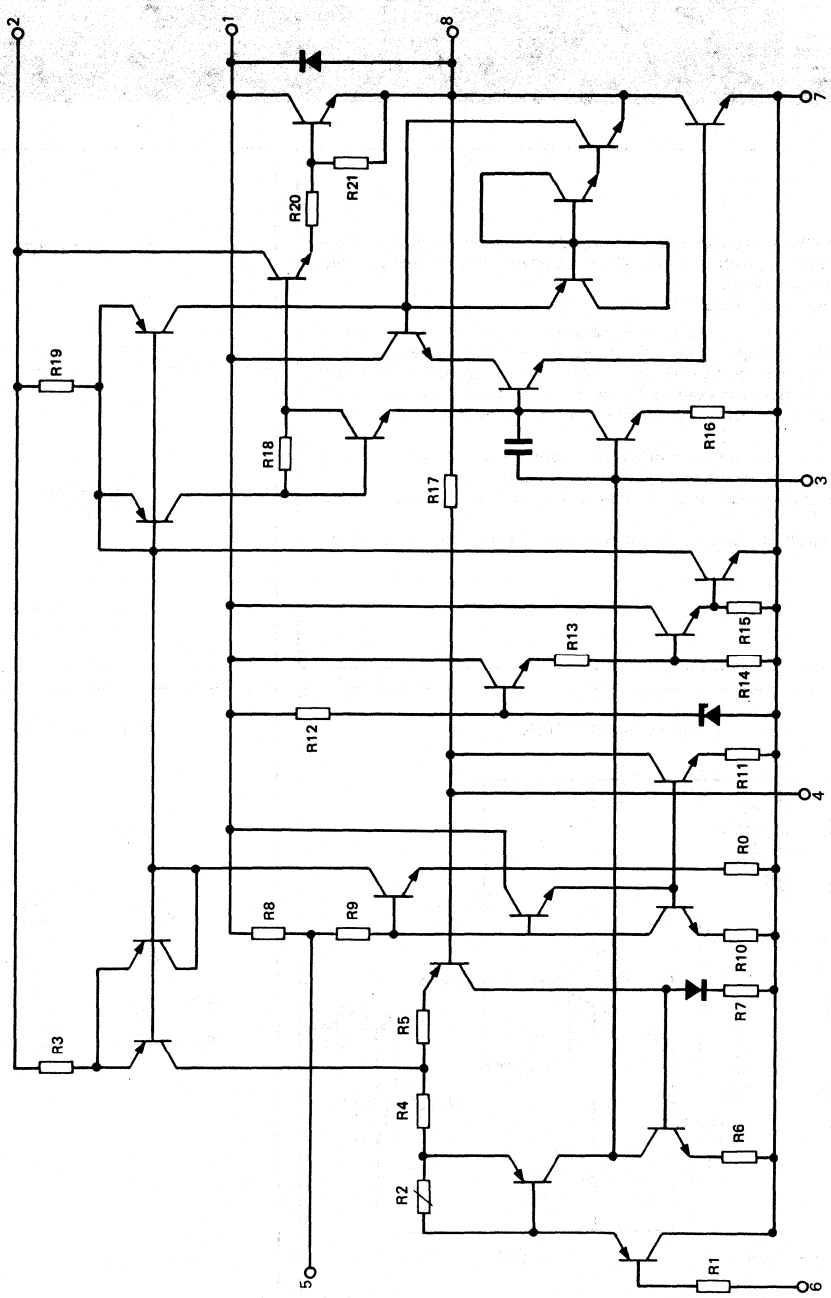
SCHEMATIC DIAGRAM



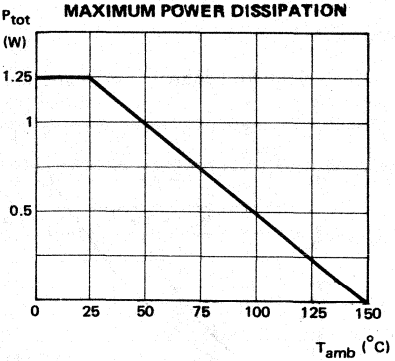
ABSOLUTE MAXIMUM RATING

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	20	V
Peak output current (no repetitive)	I_O	2.5	A
Peak output current (repetitive)	I_O	2	A
Junction temperature	T_j	+ 150	°C
Storage temperature	T_{stg}	- 40, + 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	85	°C/W

MAXIMUM POWER DISSIPATION



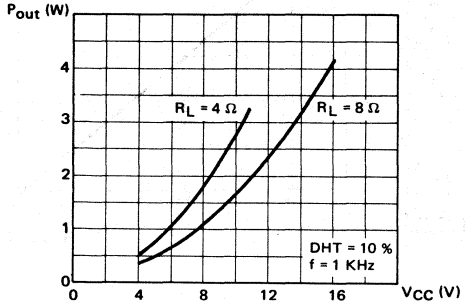
STATIC CHARACTERISTICS

T_{amb} = 25°C (Unless otherwise noted) (Note 1)

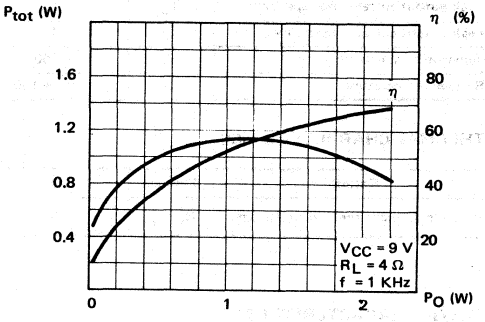
Characteristic		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4	–	20	V
Quiescent output voltage (V_{CC} = 12 V)	Pin 8	V_O	5.3	6	6.7	V
Quiescent current (V_{CC} = 9 V)	Pin 1	I_{CC}	–	8.5	16	mA
Bias current (V_{CC} = 12 V)	Pin 6	I_B	–	0.2	–	µA
Output power (d = 10 % ; f = 1 KHz)		P_O				W
R_L = 4 Ω ; V_{CC} = 9 V			1.6	2	–	
R_L = 4 Ω ; V_{CC} = 6 V			0.75	1.0	–	
R_L = 8 Ω ; V_{CC} = 12 V			–	2.3	–	
Maximum input voltage peak		V_I	–	–	310	mV
Input resistance	Pin 6	Z_I	–	5	–	MΩ
Frequency response (- 3 dB)						
V_{CC} = 9 V ; R_f = 56 Ω ; C3 = 390 pF ; R_L = 4 Ω				40 - 10.000		Hz
Distortion						
V_{CC} = 9 V ; P_O = 50 mW to 1 W ; R_L = 4 Ω ; R_f = 56 Ω ; f = 1 KHz		d	–	0.3	1	%
Voltage gain (V_{CC} = 9 V ; R_L = 4 Ω ; f = 1 KHz)		A_V				dB
Open loop			60	75	–	
Closed loop (R_f = 56 Ω)			34	37	40	
Input noise voltage (V_{CC} = 9 V ; R_G = 0 ; B (- 3dB) = 40-10.000 Hz)		V_n	–	2	–	µV
Input noise current (V_{CC} = 9 V ; B (- 3 dB)= 40 - 10.000 Hz)		I_n	–	0.1	–	nA
Efficiency (V_{CC} = 9 V ; P_O= 1.6 W ; R_L = 4 Ω ; f = 1 KHz)		η	–	62	–	%
Supply voltage rejection		SVR				dB
(V_{CC} = 9 V ; R_L = 4 Ω ; f_{ripple} = 100 Hz ; R_f = 56 Ω)						
C2 = 100 µF			40	45	–	
C2 = 25 µF			–	38	–	

Note 1 : The above characteristics were obtained using the circuit shown in figure 1. (See page 6/7).

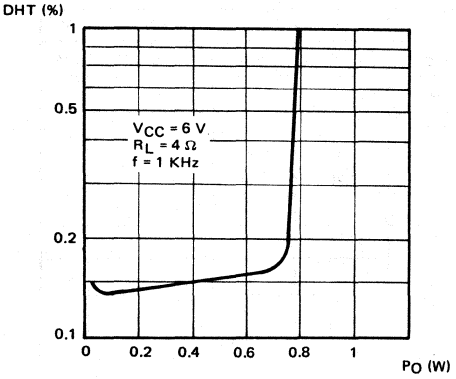
OUTPUT POWER VS SUPPLY VOLTAGE



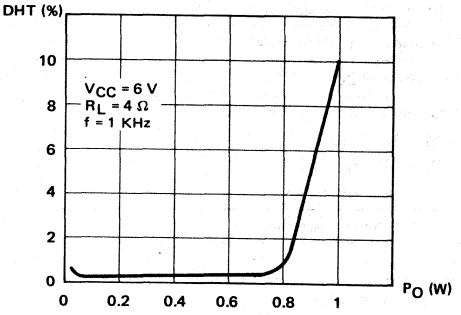
TOTAL DISSIPATED POWER VS OUTPUT POWER



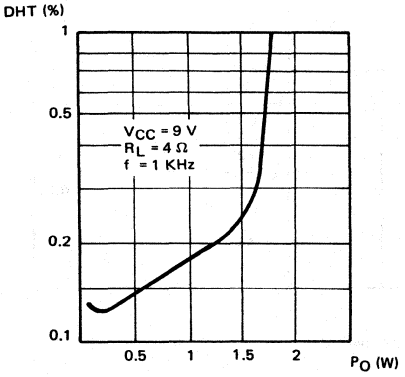
DISTORTION VS OUTPUT POWER



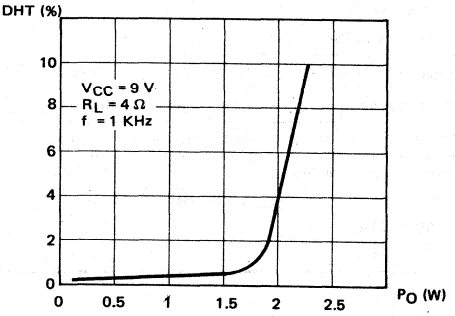
DISTORTION VS OUTPUT POWER



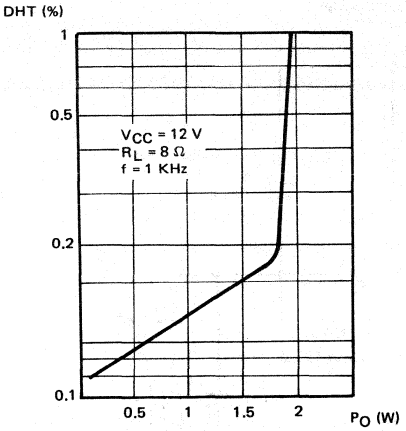
DISTORTION VS OUTPUT POWER



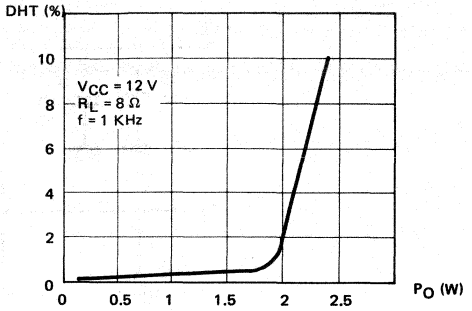
DISTORTION VS OUTPUT POWER



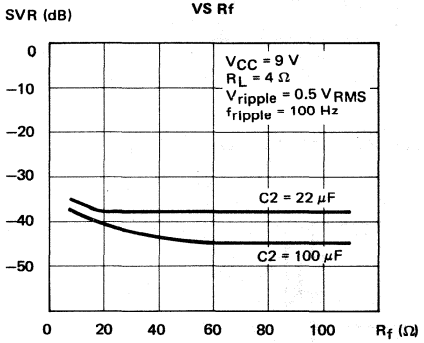
DISTORTION VS OUTPUT POWER



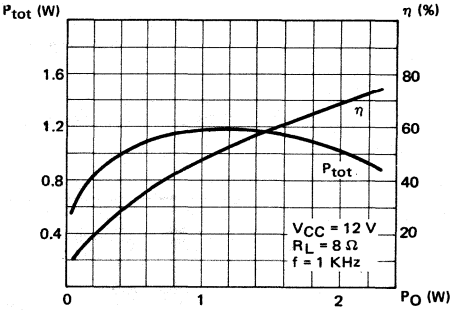
DISTORTION VS OUTPUT POWER



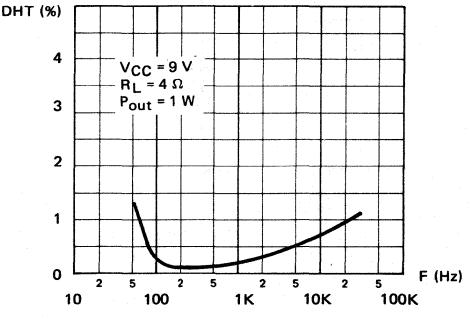
SUPPLY VOLTAGE RIPPLE REJECTION VS Rf



TOTAL DISSIPATED POWER VS OUTPUT POWER



DISTORTION VS FREQUENCY



DISTORTION VS FREQUENCY

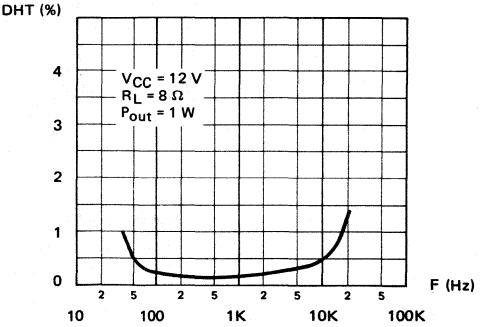


FIGURE 1 – MEASUREMENT DIAGRAM

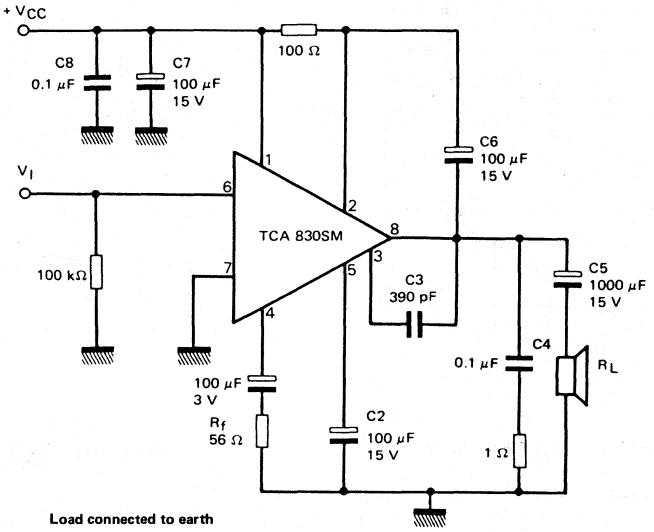
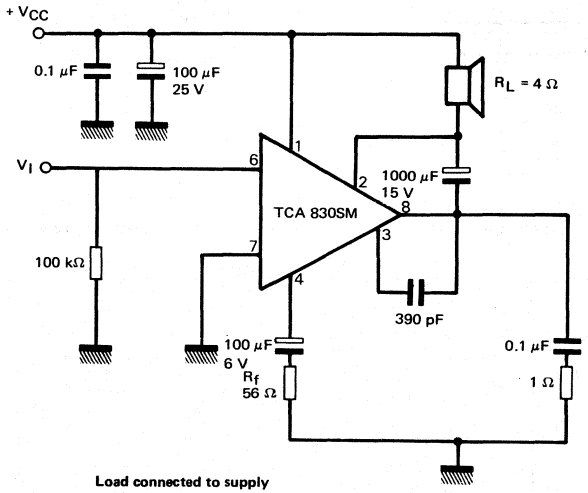


FIGURE 2 – APPLICATION DIAGRAM WITH LOAD CONNECTED TO+ VCC



PHYSICAL DIMENSIONS

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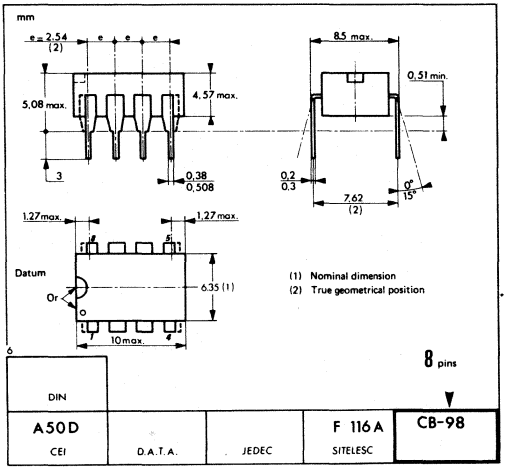
PLASTIC PACKAGE



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NOTES

Printed in France

THOMSON COMPONENTS
SEMICONDUCTEURS

TEA2025B

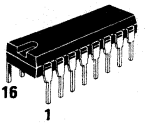
STEREO AUDIO AMPLIFIER

Dual or BTL connection modes.
Few external components.
Works with low supply voltage : 3 V.
High channel separation.
No schock noise when switch on or off.
Maximum voltage gain of 45 dB (adjustable with external resistor).
Soft clipping.
Thermal protection

- $3\ V \leqslant V_{CC} \leqslant 12\ V$
- $P = 2 \times 1\ W$, $V_{CC} = 6\ V$, $R_L = 4\Omega$
- $P = 2 \times 2.3\ W$, $V_{CC} = 9\ V$, $R_L = 4\ \Omega$
- $P = 2 \times 0.1\ W$, $V_{CC} = 3\ V$, $R_L = 4\ \Omega$

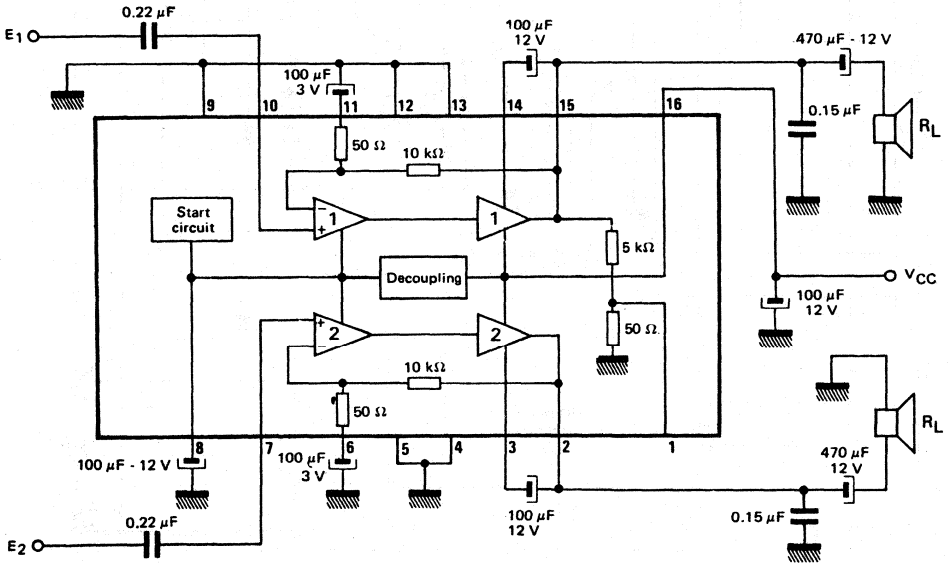
STEREO AUDIO AMPLIFIER

CASE CB-79



PLASTIC PACKAGE

APPLICATION AND TEST CIRCUIT (DUAL MODE)



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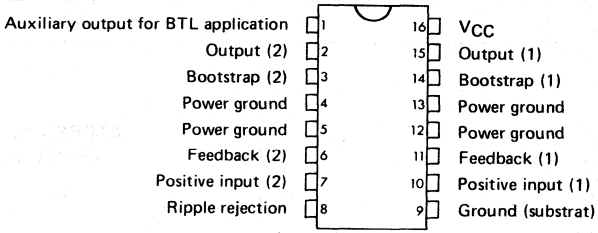
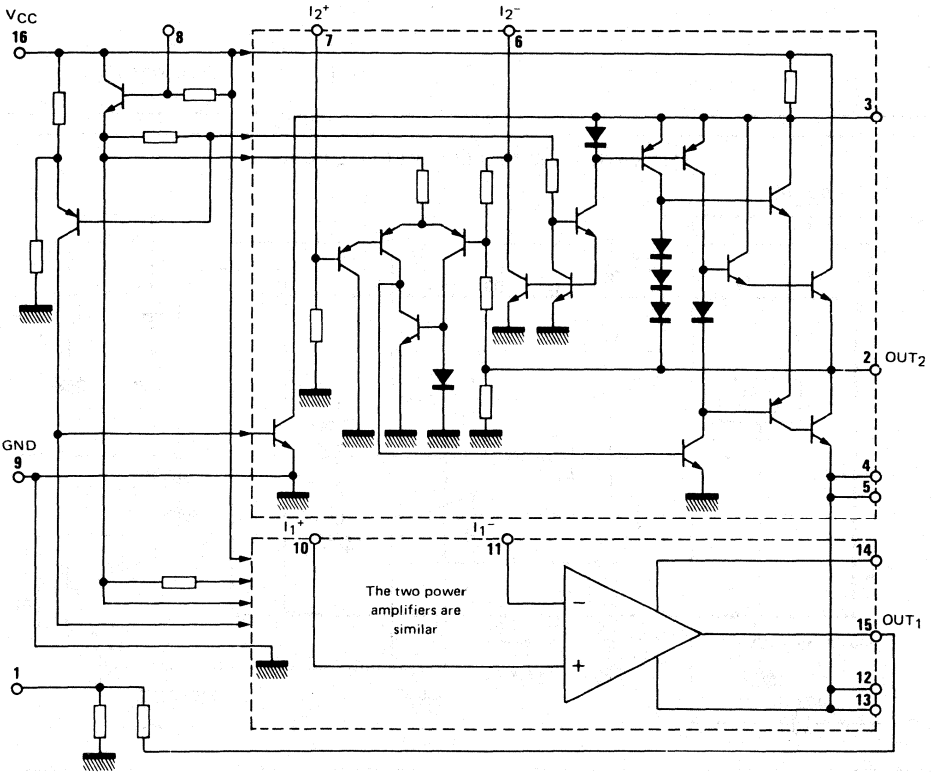
PIN ASSIGNMENT



ELECTRICAL DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	15	V
Output peak current	I_O	1.5	A
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	- 40 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-case thermal resistance	$R_{th(j-c)}$	15	°C/W
Junction-ambient thermal resistance (See note)	$R_{th(j-a)}$	60	°C/W

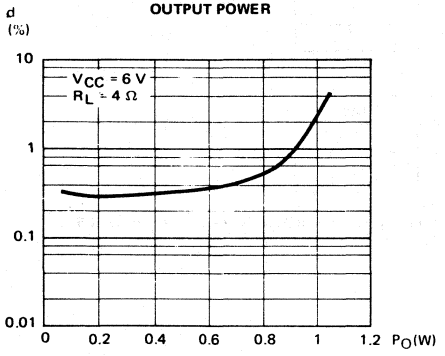
Note : The $R_{th(j-a)}$ is measured on devices bonded on a 10 x 5 x 0.15 cm glass-epoxy substrate with a 35 μm thick copper surface of 5 cm^2.

ELECTRICAL OPERATING CHARACTERISTICS

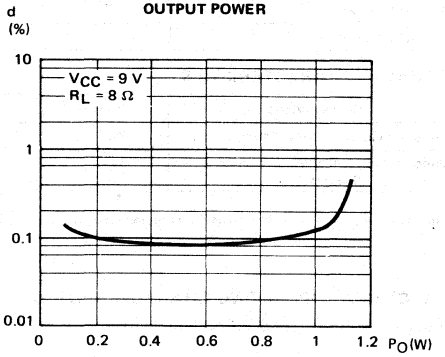
T_{amb} = 25°C, V_{CC} = 9 V, dual mode (unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3	–	12	V
Quiescent current	I_{CC}	–	40	50	mA
Quiescent output voltage	V_O	–	4.5	–	V
Voltage gain	A_V				dB
Dual mode		43	45	47	
BTL mode		49	51	53	
Voltage gain difference	ΔA_V	–	–	± 1	dB
Input impedance	R_I	–	30	–	kΩ
Output power (f = 1 KHz ; d = 10 %)	P_O				
Dual mode - per channel					W
V_{CC} = 9 V : R_L = 4 Ω		1.7	2.3	–	
R_L = 8 Ω		–	1.3	–	
V_{CC} = 6 V : R_L = 4 Ω		0.7	1	–	
R_L = 8 Ω		–	0.6	–	
V_{CC} = 3 V : R_L = 4 Ω		–	0.1	–	
BTL mode					
V_{CC} = 9 V : R_L = 8 Ω		–	4.7	–	
V_{CC} = 6 V : R_L = 4 Ω		–	2.8	–	
Distortion (V_{CC} = 9 V ; R_L = 4 Ω ; f = 1 KHz ; P_o = 250 mW)	d				%
Dual mode		–	0.3	1.5	
BTL mode		–	0.5	–	
Supply voltage rejection (R_G = 0, A_V = 45 dB, V_{ripple} = 150 mV RMS, f_{ripple} = 100 Hz)	SVR	40	46	–	dB
Input noise voltage (A_V = 200, Bandwidth : 20 Hz to 20 KHz)	V_n				μV
R_G = 0		–	1.5	3	
R_G = 10 kΩ		–	3	6	
Cross-talk (R_G = 10 kΩ ; f = 1 KHz ; R_L = 4 Ω ; P_o = 1 W)	C_T	40	55	–	dB

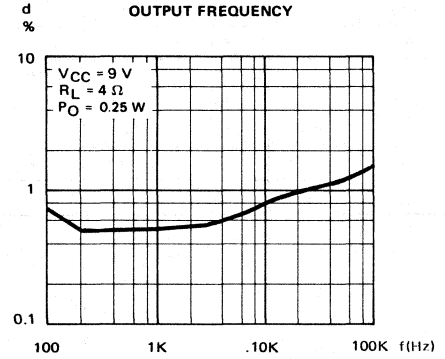
TYPICAL DISTORTION VERSUS OUTPUT POWER



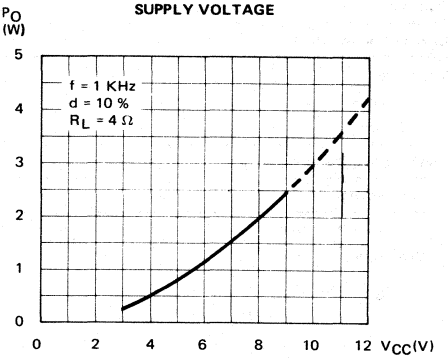
TYPICAL DISTORTION VERSUS OUTPUT POWER



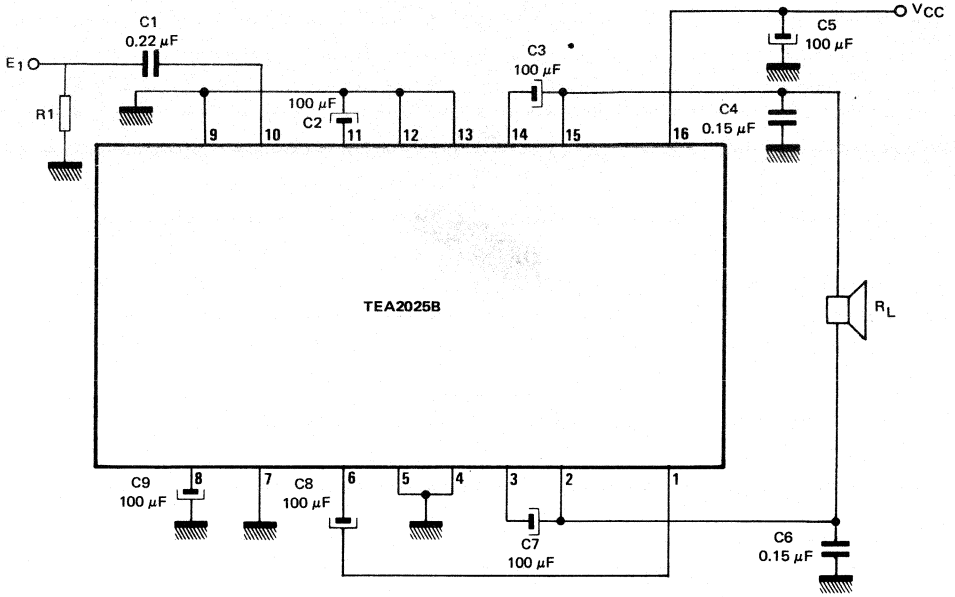
TYPICAL DISTORTION VERSUS OUTPUT FREQUENCY



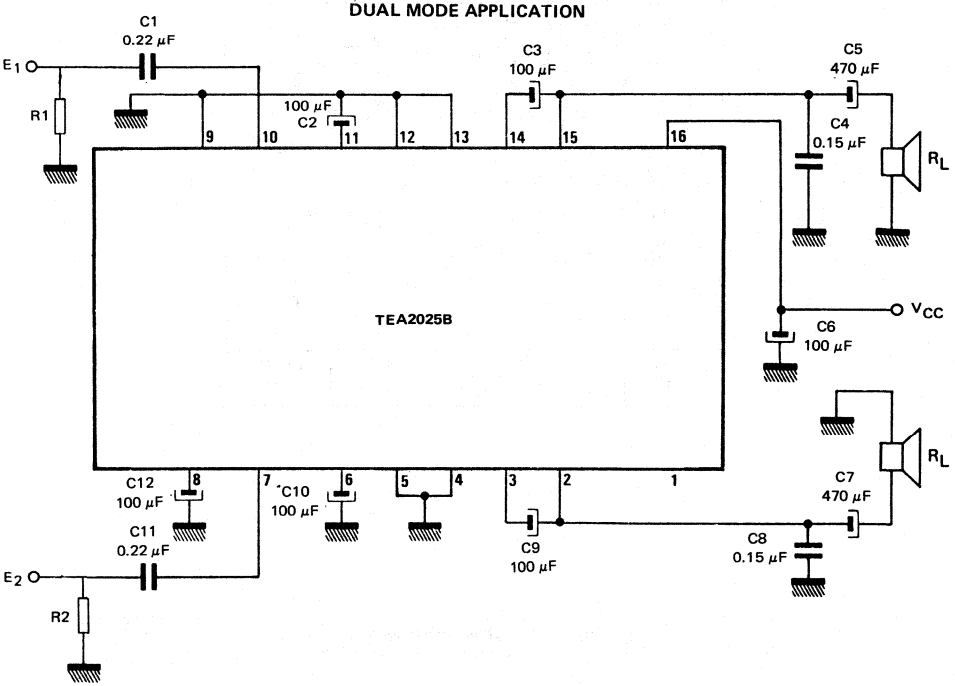
DUAL MODE OUTPUT POWER/VERSUS SUPPLY VOLTAGE



BTL MODE APPLICATION

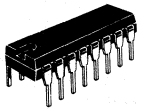


DUAL MODE APPLICATION

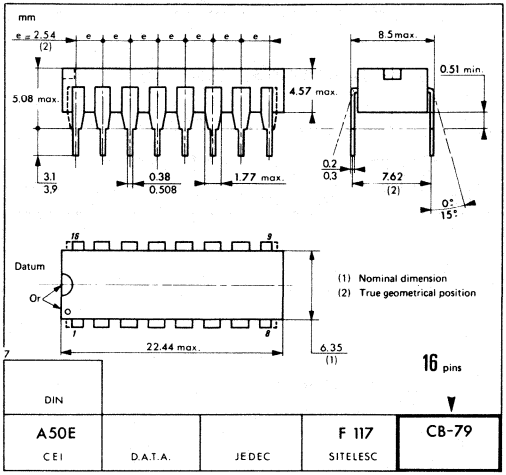


PHYSICAL DIMENSIONS

CASE CB - 79



PLASTIC PACKAGE



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THOMSON COMPONENTS SEMICONDUCTEURS

TDA2003

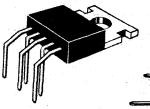
10 W CAR RADIO AUDIO AMPLIFIER

The TDA 2003 has improved performance with the same pin configuration as the TDA 2002. The additional features of TDA 2002; very low number of external components, ease of assembly, space and cost saving, are maintained. The device provides a high output current capability (up to 3.5 A) very low harmonic and cross-over distortion.
Completely safe operation is guaranteed due to protection against DC and AC short circuit between all pins and ground, thermal over-range, load dump voltage surge up to 40 V, polarity inversion and fortuitous open ground.

10 W CAR RADIO AUDIO AMPLIFIER

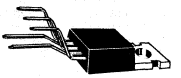
CASE

CB-367



TDA2003 H

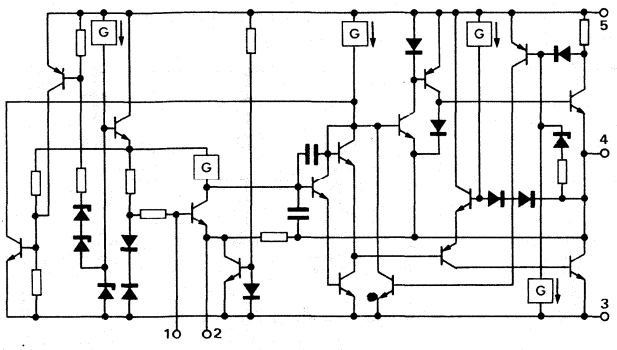
CB-360



TDA2003V

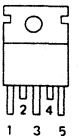
PLASTIC PACKAGE

BLOCK DIAGRAM

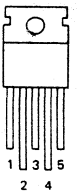


PIN ASSIGNMENT

CB 367



CB-360



1 Non inverting input
2 Inverting input
3 Ground
4 Output
5 Supply voltage

Tab is connected to pin 3

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak supply voltage (50 ms)	V_{CC}	40	V
DC supply voltage	V_{CC}	28	V
Operating supply voltage	V_{CC}	18	V
Output peak current (repetitive)	I_O	3.5	A
Output peak current (no repetitive)	I_O	4.5	A
Power dissipation (T_{case} = 90 °C)	P_{tot}	20	W
Storage and junction temperature	$T_j - T_{stg}$	− 40 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-case thermal resistance	$R_{th(j-c)}$	3 max.	°C/W

STATIC CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 14.4 V; (see figure 1) (Unless otherwise stated)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{CC}	8	–	18	V
Quiescent output voltage	Pin 4	V_O	6.1	6.9	7.7	V
Quiescent drain current	Pin 5	I_{CC}	–	44	50	mA

DYNAMIC CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 14.4 V; A_V = 40 dB; (see figure 2) (Unless otherwise stated)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Output power (d = 10 %; f = 1kHz)	P_O				V
R_L = 4 Ω		5.5	6	–	
R_L = 2 Ω		9	10	–	
R_L = 3.2 Ω		–	7.5	–	
R_L = 1.6 Ω		–	12	–	
Input saturation voltage	V_I	300	–	–	mV

FIG. 1 – DC TEST CIRCUIT

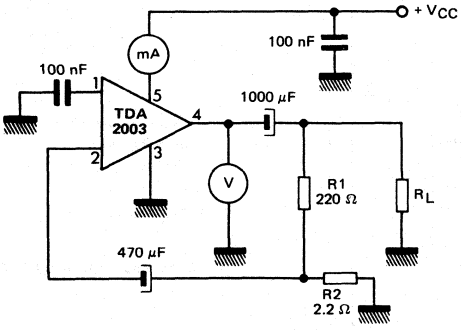
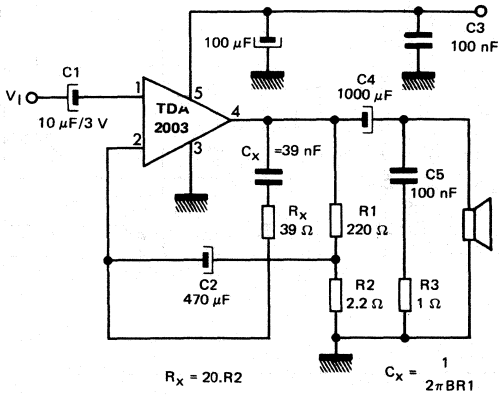


FIG. 2 – AC TEST CIRCUIT



ELECTRICAL OPERATING CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input sensitivity	S				mV
$f = 1$ kHz; $P_O = 0.5$ W; $R_L = 4\ \Omega$		–	14	–	
$P_O = 6$ W; $R_L = 4\ \Omega$		–	55	–	
$P_O = 0.5$ W; $R_L = 2\ \Omega$		–	10	–	
$P_O = 10$ W; $R_L = 2\ \Omega$		–	50	–	
Bandwidth (– 3 dB)	B				Hz
$P_O = 1$ W; $R_L = 4\ \Omega$			40 to 15.000		
Harmonic distortion	d				%
$0.05\ W \leqslant P_O \leqslant 4.5\ W$; $R_L = 4\ \Omega$; $f = 1$ kHz		–	0.15	–	
$0.05\ W \leqslant P_O \leqslant 7.5\ W$; $R_L = 2\ \Omega$; $f = 1$ kHz		–	0.15	–	
Input resistance ($f = 1$ kHz) Pin 1	R_I	70	150	–	kΩ
Voltage gain ($R_L = 4\ \Omega$; $f = 1$ kHz)	A_V				dB
Open loop		–	80	–	
Closed loop		39.5	40	40.5	
Input noise voltage	V_n				μV
B (– 3 dB) = 10 to 25.000 Hz; B (– 20 dB) = 4 to 27.000 Hz		–	1	5	
Input noise current	i_n				pA
B (– 3 dB) = 10 to 25.000 Hz; B (– 20 dB) = 4 to 27.000 Hz		–	60	200	
Efficiency	η				%
$f = 1$ kHz; $P_O = 6$ W; $R_L = 4\ \Omega$		–	69	–	
$P_O = 10$ W; $R_L = 2\ \Omega$		–	65	–	
Supply voltage rejection	SVR				dB
$f = 100$ Hz; $V_{ripple} = 0.5$ V; $R_G = 10$ kΩ; $R_L = 4\ \Omega$		30	36	–	

TYPICAL CHARACTERISTICS

FIG. 3 – QUIESCENT OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE

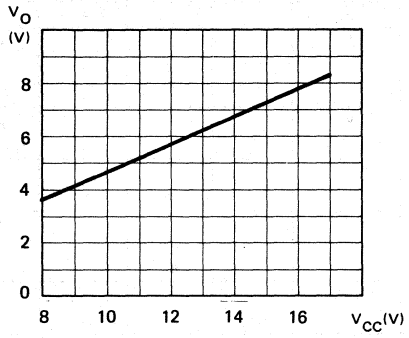


FIG. 4 – QUIESCENT DRAIN CURRENT VERSUS SUPPLY VOLTAGE

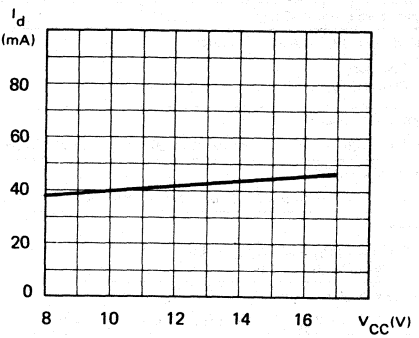


FIG. 5 – OUTPUT POWER VERSUS SUPPLY VOLTAGE

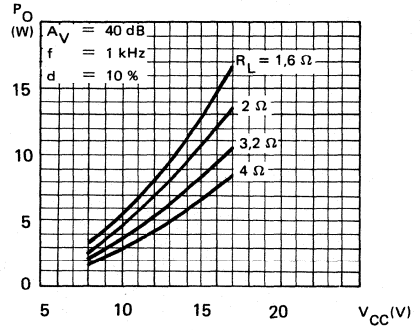
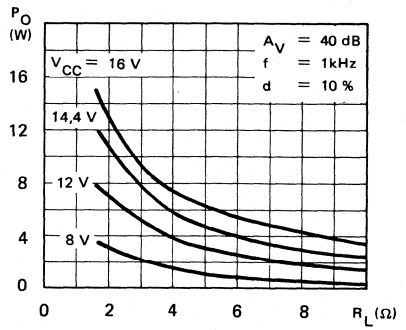


FIG. 6 – OUTPUT POWER VERSUS R_L



TYPICAL CHARACTERISTICS (continued)

FIG. 7 – GAIN VERSUS INPUT SENSITIVITY

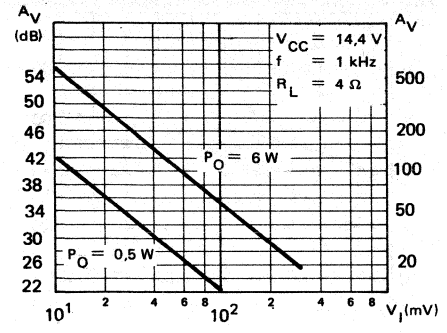


FIG. 8 – GAIN VERSUS INPUT SENSITIVITY

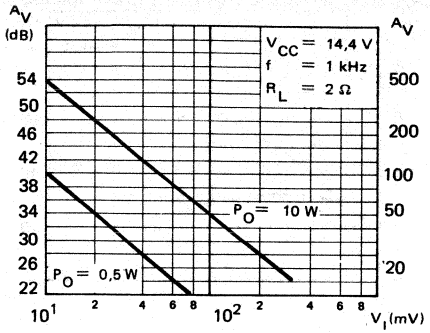


FIG. 9 – DISTORTION VERSUS OUTPUT POWER

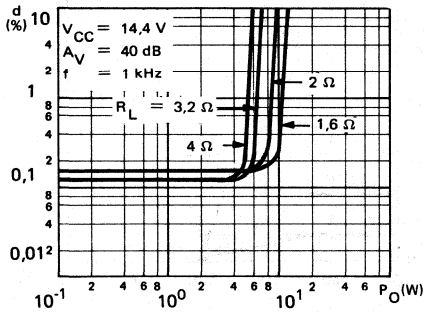


FIG. 10 – DISTORTION VERSUS FREQUENCY

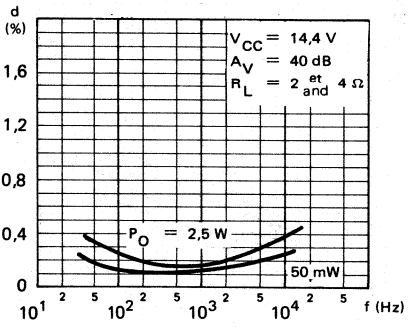


FIG. 11 – SUPPLY VOLTAGE REJECTION VERSUS VOLTAGE GAIN

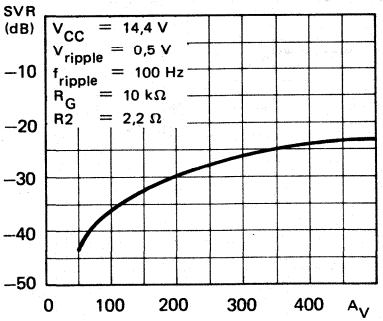
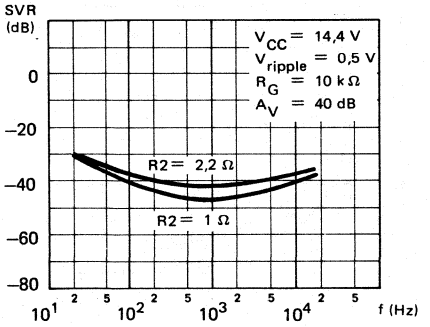


FIG. 12 – SUPPLY VOLTAGE REJECTION VERSUS FREQUENCY



TYPICAL CHARACTERISTICS (continued)

FIG. 13 – POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER (R_L = 4 Ω)

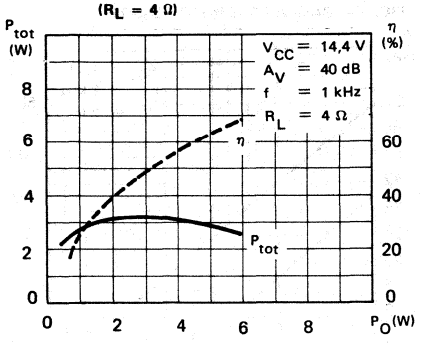


FIG. 14 – POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER (R_L = 2 Ω)

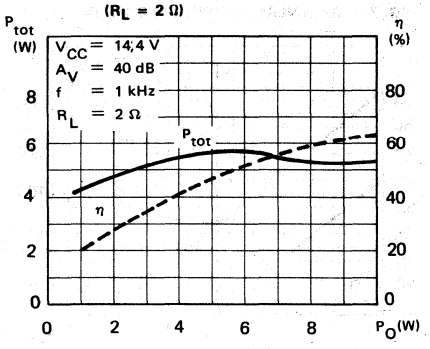


FIG. 15 – MAXIMUM POWER DISSIPATION VERSUS SUPPLY VOLTAGE (SINE WAVE OPERATION)

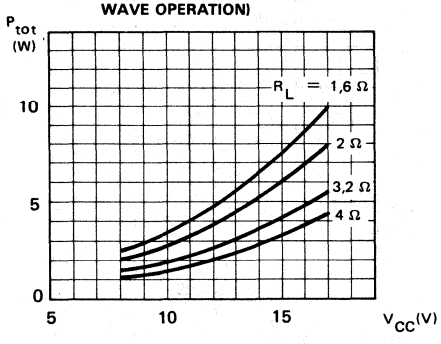


FIG. 16 – MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

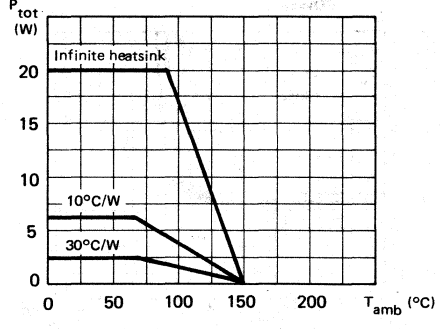


FIG. 17 – TYPICAL VALUES OF CAPACITOR (C_x) FOR DIFFERENT VALUES OF FREQUENCY RESPONSE (B)

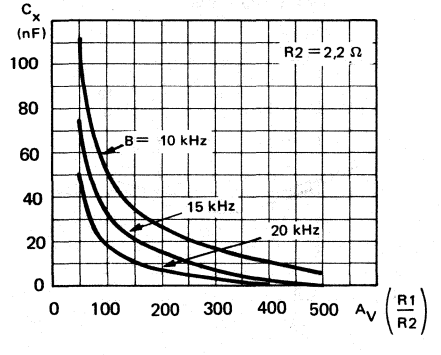
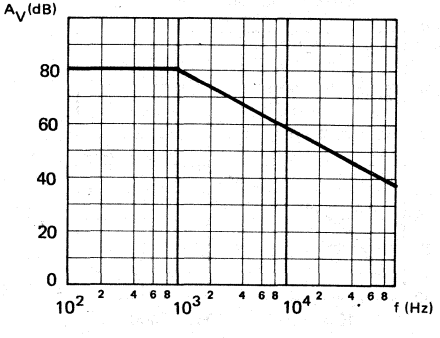


FIG. 18 – OPEN LOOP VOLTAGE GAIN VERSUS FREQUENCY



APPLICATION INFORMATION

FIG. 19 – TYPICAL APPLICATION CIRCUIT

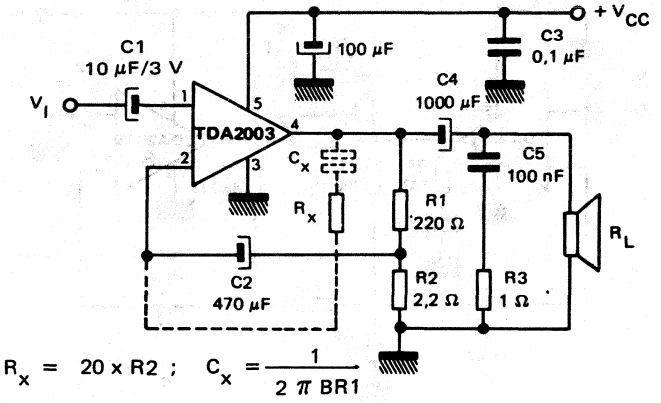
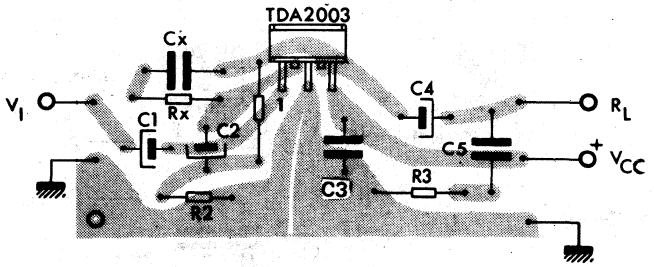
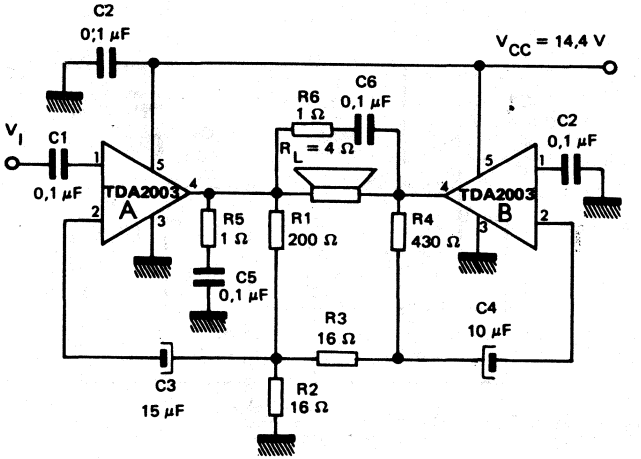


FIG. 20 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 19 (1/1 SCALE)



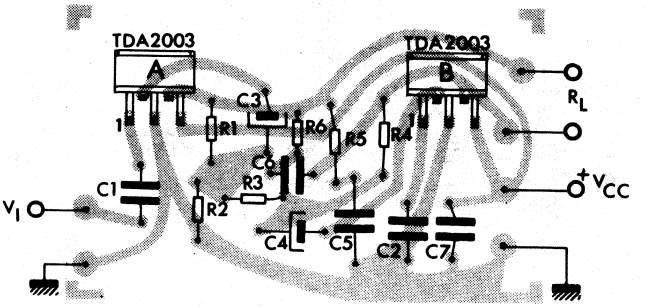
APPLICATION INFORMATION (continued)

FIG. 21 – 20 W BRIDGE CONFIGURATION APPLICATION CIRCUIT*



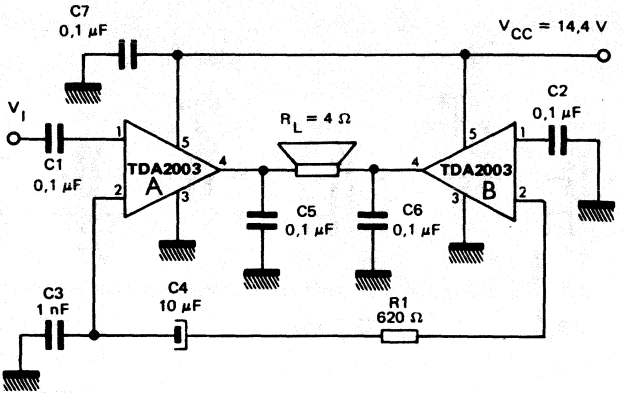
The values of the capacitors C3 and C4 are different to optimize the SVR (Typ. 40 dB)

FIG. 22 – PC BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 21 (1/1 SCALE)



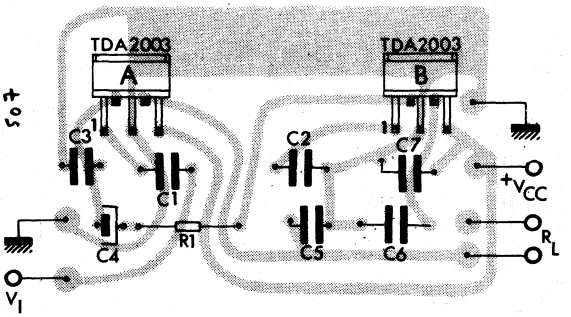
APPLICATION INFORMATION (continued)

FIG. 23 – LOW COST BRIDGE CONFIGURATION CIRCUIT (P_O = 18 W)*



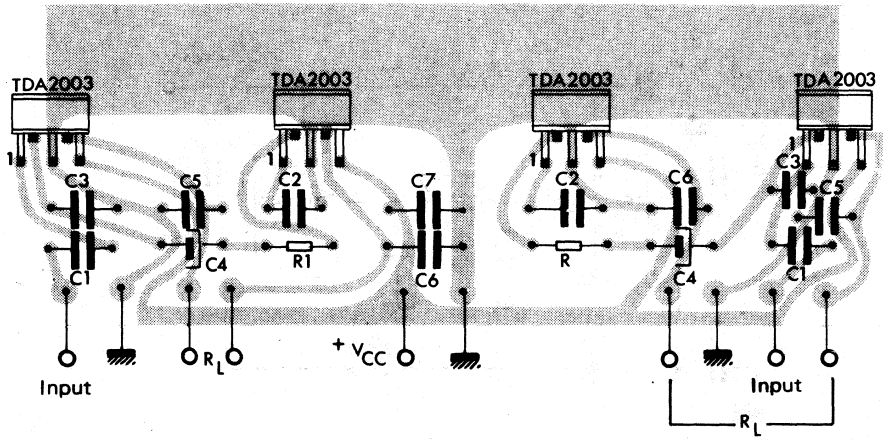
In this application the devices can support a short-circuit between every side of the loudspeaker and ground.

FIG. 24 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 23 (1/1 SCALE)



APPLICATION INFORMATION (continued)

FIG. 25 – P.C. BOARD AND COMPONENT LAYOUT FOR THE LOW COST BRIDGE AMPLIFIER OF FIG. 23 STEREO VERSION (1:1 SCALE)



BUILT-IN PROTECTION SYSTEMS

LOAD DUMP VOLTAGE SURGE

The TDA2003 has a circuit which enables is to withstand a voltage pulse train, on pin 5, of the type shown in fig. 26.

If the supply voltage peaks to more than 40 V, then an LC filter must be inserted between the supply and pin 5, in order to assure that the pulses at pin 5 will be held within the limits shown in fig. 26.

A suggested LC network is shown in fig. 27. With this network, a train of pulses with amplitude up to 120 V and width 2 ms can be applied at point A.

Figure 26

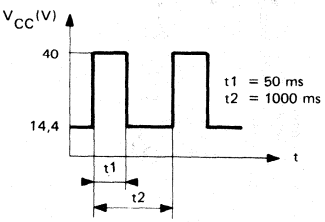
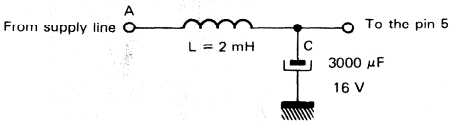


Figure 27



SHORT-CIRCUIT (AC AND DC CONDITIONS)

The TDA2003 can withstand a permanent short-circuit on the output for a supply voltage up to 16 V.

POLARITY INVERSION

High current (up to 5 A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 1 A fuse (normally connected in series with the supply). This feature is added to avoid destruction if, during fitting to the car, a mistake on the connection of the supply is made.

OPEN GROUND

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA2003 protection diodes are included to avoid any damage.

INDUCTIVE LOAD

A protection diode is provided between pin 4 and 5 (see the internal schematic diagram) to allow use of the TDA2003 with inductive loads. In particular, the TDA2003 can drive a coupling transformer for audio modulation.

DC VOLTAGE

The maximum operating DC voltage on the TDA2003 is 18 V. However the device can withstand a DC voltage up to 28 V with to damage. This could occur during winter if two batteries are series connected to crank the engine.

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1 – An overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2 – The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_O (and therefore P_{tot}) and I_d are reduced (figs. 28 and 29).

FIG. 28 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE

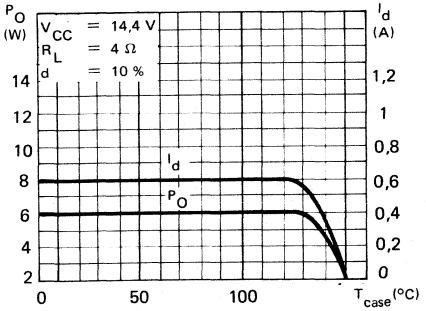
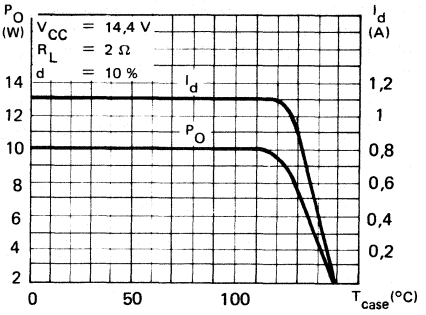


FIG. 29 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE



PRATICAL CONSIDERATIONS

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	10 μF	Input DC decoupling		Noise at switch-on, switch-off
C2	470 μF	Ripple rejection		Degradation of SVR
C3	0,1 μF	Supply bypassing		Danger of oscillation
C4	1000 μF	Output coupling to load		Higher low frequency cutoff
C5	0,1 μF	Frequency stability		Danger of oscillation at high frequencies with inductive loads
C_x	$\cong \frac{1}{2\pi\ BR1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
R1	$(A_V - 1) \bullet R2$	Setting of gain		Increase of drain current
R2	2,2 Ω	Setting of gain and SVR	Degradation of SVR	
R3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_x	$\cong$ 20 R2	Upper frequency cutoff	Poor high frequency attenuation	Danger of oscillation

PRINTED CIRCUIT BOARD

The layout shown in figure 20 is recommended. If different layours are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

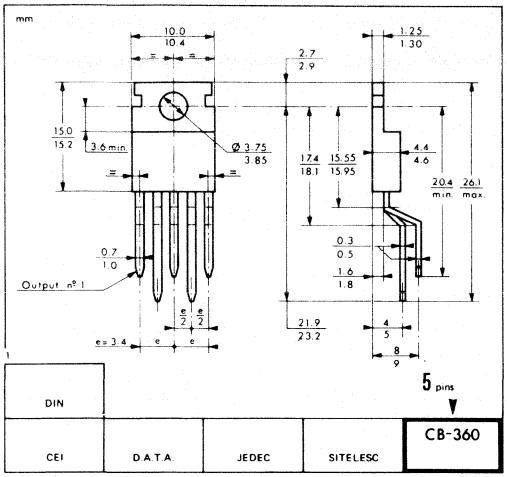
ASSEMBLY SUGGESTION

The device does not require insulation between the package and the heatsink. Pin lenght should be as short as possible. The soldering temperature must not exceed 260 °C for 12 seconds.

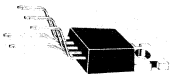
APPLICATION SUGGESTION

The recommended component values are those shown in the application circuits of fig. 19. Different values can be used. The following table is intended to aid the car-radio designer.

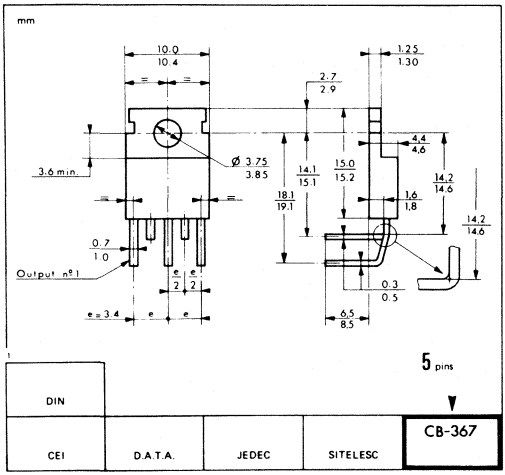
PHYSICAL DIMENSIONS



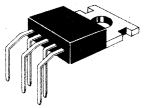
CB-360



PLASTIC PACKAGE



CB-367



PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TDA2006

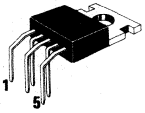
10 W AUDIO POWER AMPLIFIER

The TDA 2006 is a monolithic integrated circuit in CB-360 or CB-367 package intended for use in audio amplifier.
Typically it provides 12 W ouput power (d = 10 %) at ± 12 V on a 4 Ω load, and 8 W on a 8 Ω.
The TDA 2006 provides high output (up to 2,5 A) and has very low harmonic and cross over distortion.
The device incorporates a short-circuit protection which automatically limits the dissipated power so as to keep the working point of the output transistors within their safe operating area.
A conventional thermal shut down system is also included.

10 W AUDIO POWER AMPLIFIER

CASES

CB-367



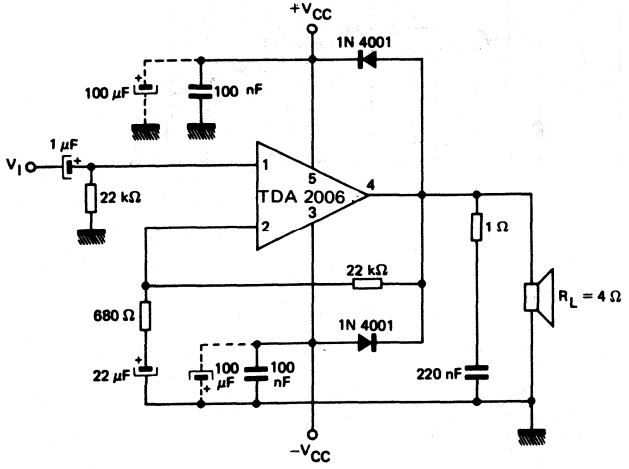
TDA2006 H

CB-360

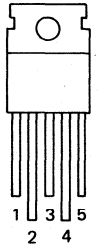
TDA2006 V

PLASTIC PACKAGE

TEST AND APPLICATION CIRCUIT



PIN ASSIGNMENT



1 Non inverting input
2 Inverting input
3 − V_{CC}
4 Output
5 + V_{CC}

Tab is connected to pin 3

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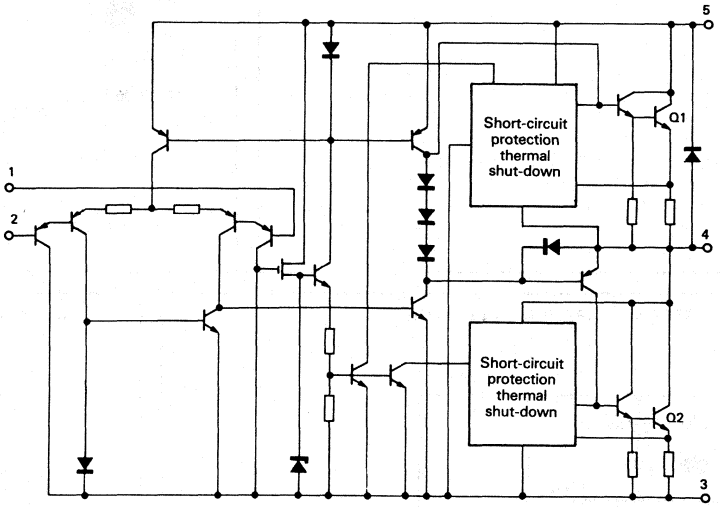
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	± 15	V
Input voltage	V_I	V_{CC}	
Differential input voltage	V_{ID}	± 12	V
Output peak current (internally limited)	I_O	3	A
Power dissipation (T_{case} = 90 °C)	P_{tot}	20	W
Junction temperature	Tj	− 40 to + 150	°C
Storage temperature	T_{stg}	− 40 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-case thermal resistance (max)	$R_{th(j-c)}$	3	°C/W

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{CC} = ± 12 V; T_{amb} = 25 °C (refer to the test circuit) (Unless otherwise stated)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	± 6	–	± 15	V
Quiescent drain current (V_{CC} = ± 15 V)	I_{CC}	–	40	80	mA
Bias current (V_{CC} = ± 15 V)	I_B	–	0.2	3	μA
Input offset voltage (V_{CC} = ± 15 V)	V_{IO}	–	± 8	–	mV
Input offset current (V_{CC} = ± 15 V)	I_{IO}	–	± 80	–	nA
Output offset voltage (V_{CC} = ± 15 V)	V_O	–	± 10	± 100	mV
Output power (d = 10 %; Av = 30 dB; f = 1 kHz) R_L = 4 Ω R_L = 8 Ω	P_O	 – 6	 12 8	 – –	W
Harmonic distortion 0.1 W ⩽ P_O ⩽ 8 W; R_L = 4 Ω; A_V = 30 dB; f = 1 kHz 0.1 W ⩽ P_O ⩽ 4 W; R_L = 8 Ω; A_V = 30 dB; f = 1 kHz	d	 – –	 0.2 0.1	 – –	%
Input sensitivity (A_V = 30 dB; f = 1 kHz) P_O = 10 W; R_L = 4 Ω P_O = 6 W; R_L = 8 Ω	S	 – –	 200 220	 – –	mV
Bandwidth (– 3 dB) A_V = 30 dB; P_O = 8 W; R_L = 4 Ω	B	10 to 140.000			Hz
Input resistance Pin 1	R_I	0.5	5	–	MΩ
Voltage gain (f = 1 kHz) Open loop Closed loop	A_V	 – 29.5	 75 30	 – 30.5	dB
Input noise voltage (R_L = 4 Ω) Test equipment bandwith (– 3 dB) = 10 to 25.000 Hz	V_n	 –	 3	 10	μV
Input noise current (R_L = 4 Ω) Test equipment bandwith (– 3 dB) = 10 to 25.000 Hz	i_n	 –	 80	 200	pA
Supply voltage rejection ratio R_L = 4 Ω; A_V = 30 dB; R_G = 22 kΩ; V_{ripple} = 0.5 V_{eff} f_{ripple} = 100 Hz	SVR	 40	 50	 –	dB
Drain current P_O = 12 W; R_L = 4 Ω P_O = 8 W; R_L = 8 Ω	I_{CC}	 – –	 845 490	 – –	mA
Thermal shut-down case temperature (P_{tot} = 9 W)	T_{case}	110	–	–	°C

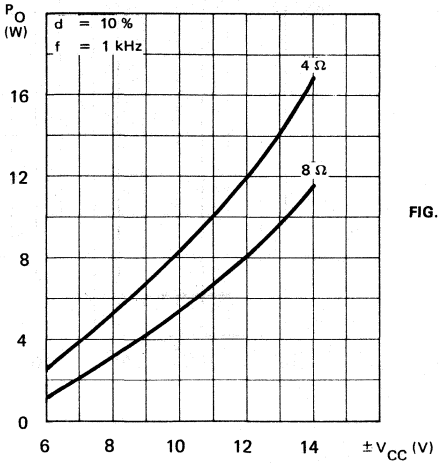


FIG. 1 — TYPICAL OUTPUT POWER VERSUS SUPPLY VOLTAGE

FIG. 2 – DISTORTION VERSUS OUTPUT POWER

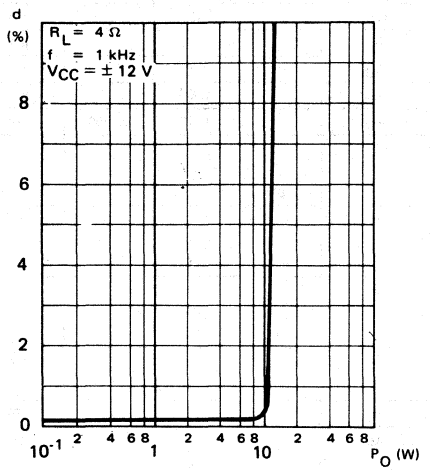


FIG. 3 – TYPICAL DISTORTION VERSUS OUTPUT POWER

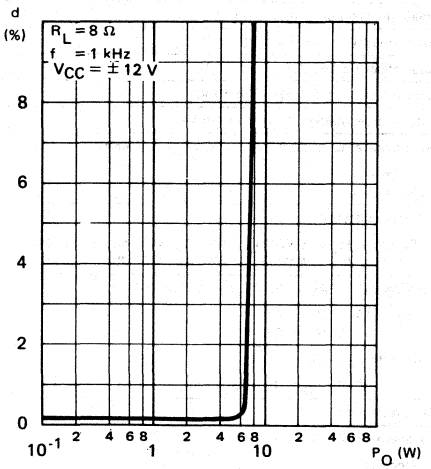


FIG. 4 – TYPICAL DISTORTION VERSUS FREQUENCY

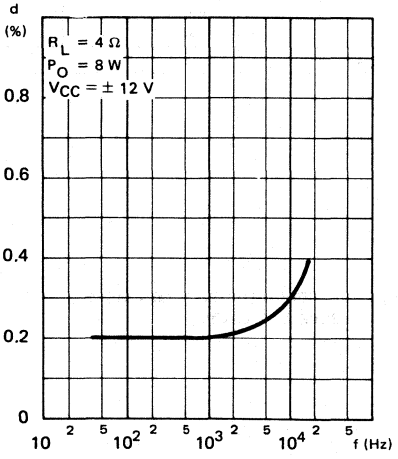


FIG. 5 – TYPICAL DISTORTION VERSUS FREQUENCY

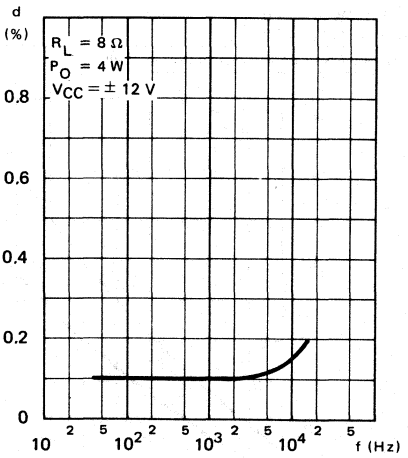


FIG. 6 – TYPICAL SENSITIVITY VERSUS OUTPUT POWER

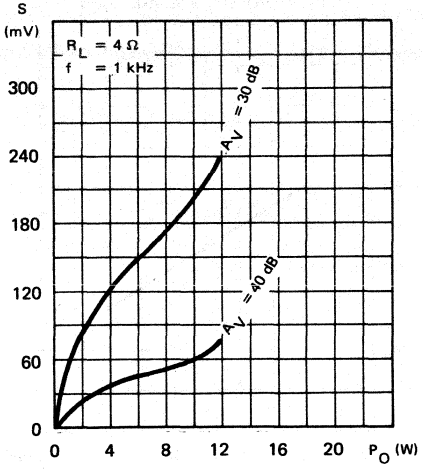


FIG. 7 – TYPICAL SENSITIVITY VERSUS OUTPUT POWER

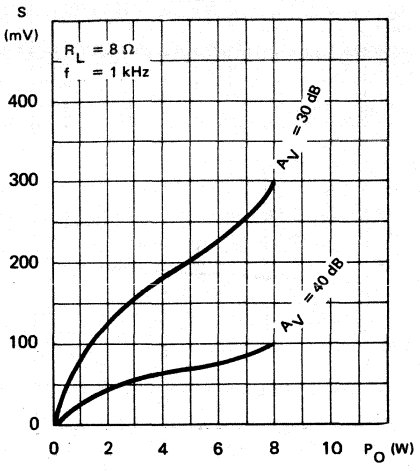


FIG. 8 – FREQUENCY RESPONSE WITH DIFFERENT VALUES OF THE ROLLOFF CAPACITOR C8 (see Fig. 14)

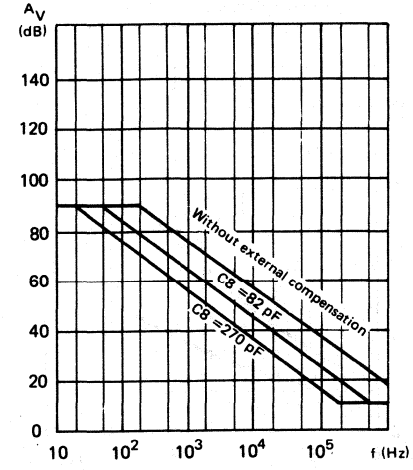


FIG. 9 – TYPICAL VALUE OF C8 VERSUS VOLTAGE GAIN FOR DIFFERENT BANDWIDTHS (see Fig. 14)

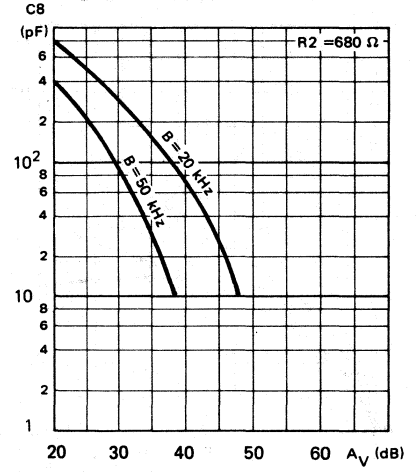


FIG. 10 – QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE

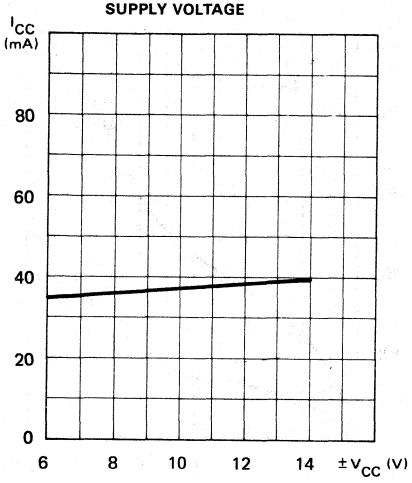


FIG. 11 – SUPPLY VOLTAGE REJECTION RATIO VERSUS VOLTAGE GAIN

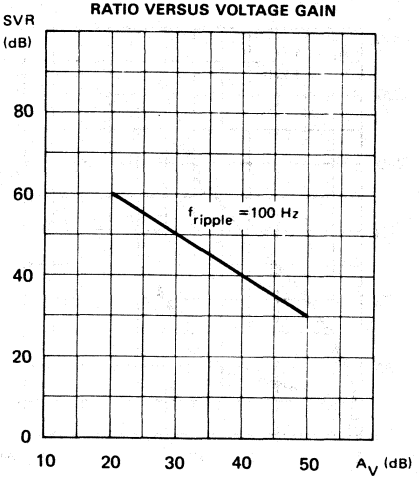


FIG. 12 – POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER

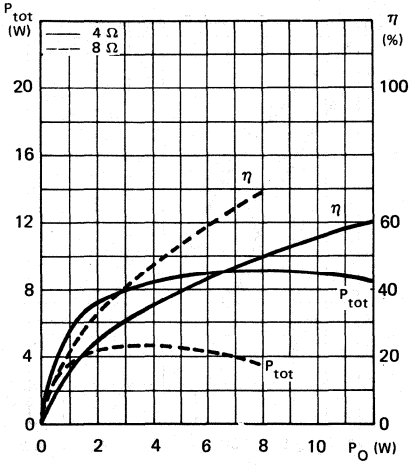


FIG. 13 – MAXIMUM POWER DISSIPATION VERSUS SUPPLY VOLTAGE (sine wave operation)

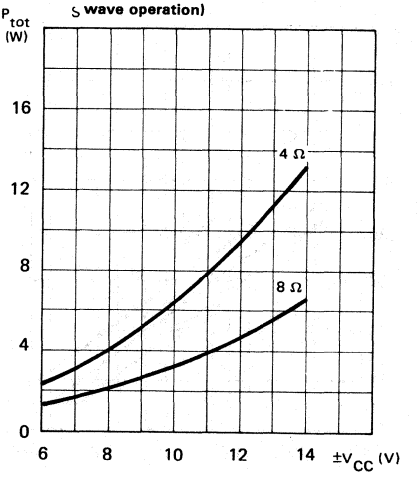
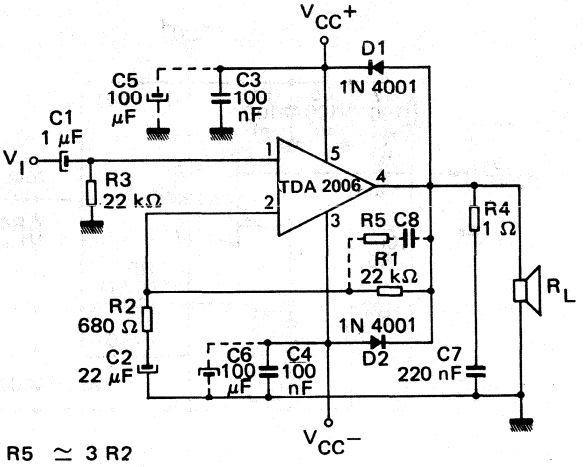


FIG. 14 – TYPICAL AMPLIFIER WITH SPLIT POWER SUPPLY



R5 ≃ 3 R2
C8 = See Figure 9

FIG. 15 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 14

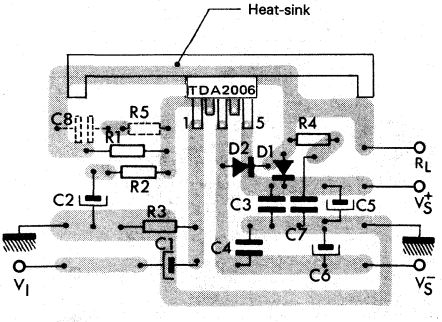


FIG. 16 – TYPICAL AMPLIFIER WITH SINGLE POWER SUPPLY

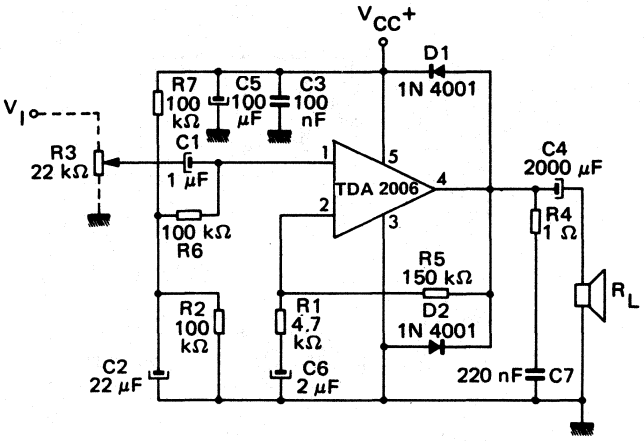


FIG. 17 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 15

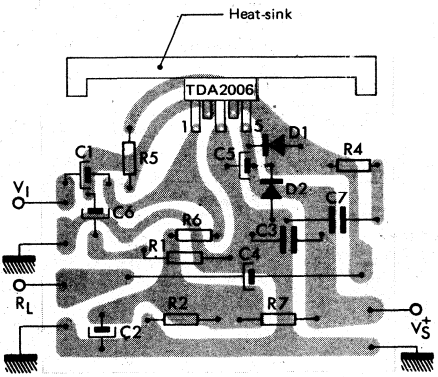
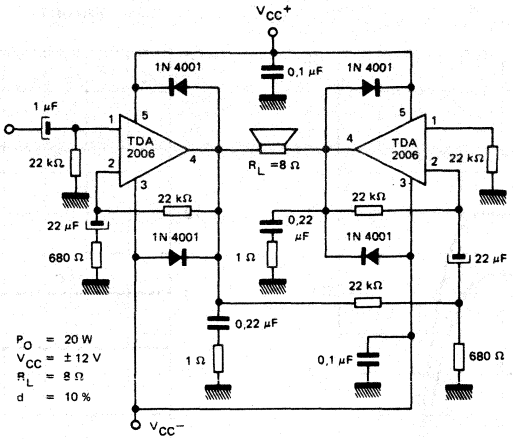


FIG. 18 – TYPICAL BRIDGE AMPLIFIER CONFIGURATION WITH SPLIT POWER SUPPLY



SHORT-CIRCUIT PROTECTION

The TDA 2006 has an internal circuit which limits the currents of the output transistors.

Figure 19 shows that the maximum output current is a function of the collector emitter voltage.

Hence, the output transistors work within their safe operating area (figure 20).

This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2006 is thus protected against temporary over-loads or short-circuit. Should the short-circuit exist for a longer time, the thermal shut-down protection keeps the junction temperature within safe limits.

FIG. 19 – MAXIMUM OUTPUT CURRENT VERSUS VOLTAGE (V_{CE}) ACROSS EACH OUTPUT TRANSISTOR

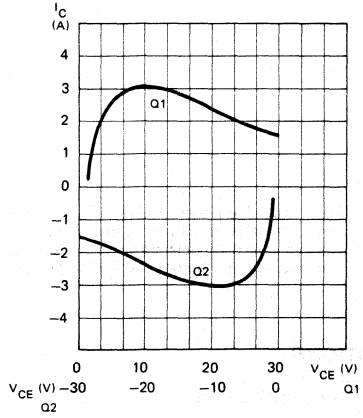
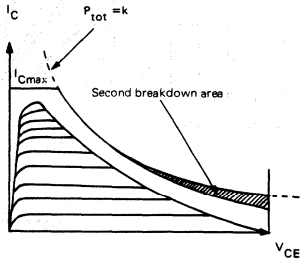


FIG. 20 – SAFE OPERATIONS AREA AND COLLECTOR CHARACTERISTIC OF THE PROTECTED POWER TRANSISTOR



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1 – An overload on the output, even if it is permanent, or an above limit ambient temperature can be easily supported since the junction temperature cannot be higher than 150 °C.

2 – The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150 °C, the thermal shut-down simply reduces the power dissipation and the current consumption.

FIG. 21 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE

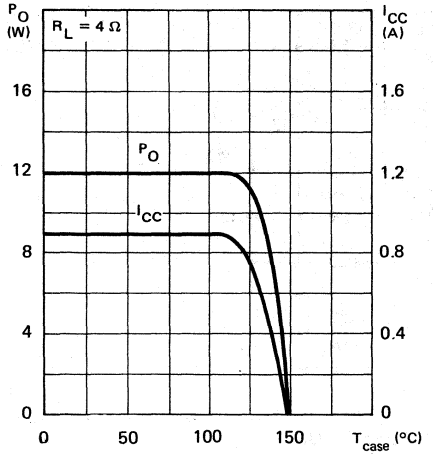
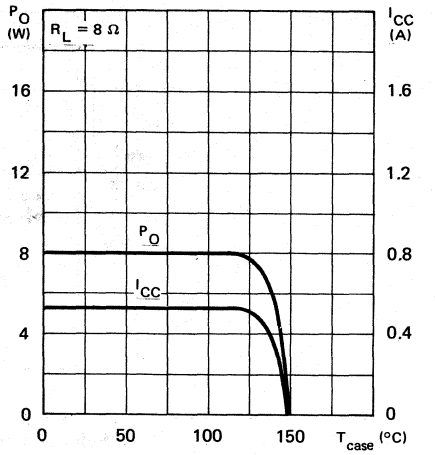


FIG. 22 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE



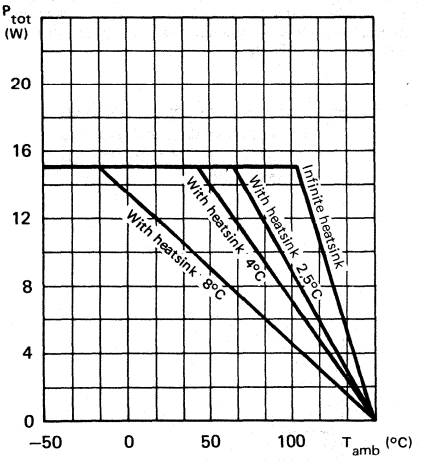


FIG. 23 – MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); figure 23 shows this dissipable power as a function of ambient temperature for different thermal resistances.

PRACTICAL CONSIDERATIONS

PRINTED CIRCUIT BOARD

The layout in figure 17 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

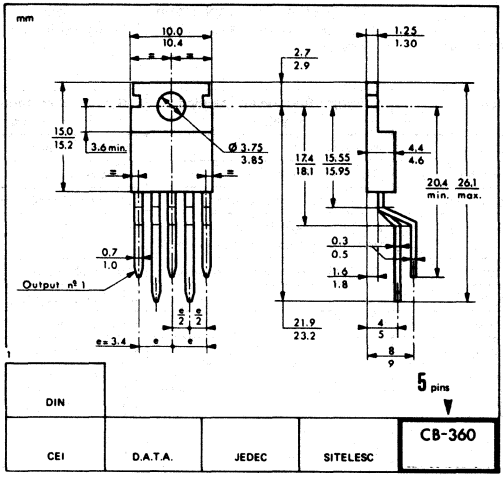
ASSEMBLY SUGGESTION

No electrical isolation needs to be used between the package and the heatsink with single supply voltage configuration.

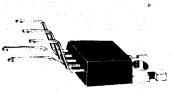
EXTERNAL COMPONENTS

The recommended values of the external components are those shown on application circuit of figure 16. Different values can be used. The following table can help the designer.

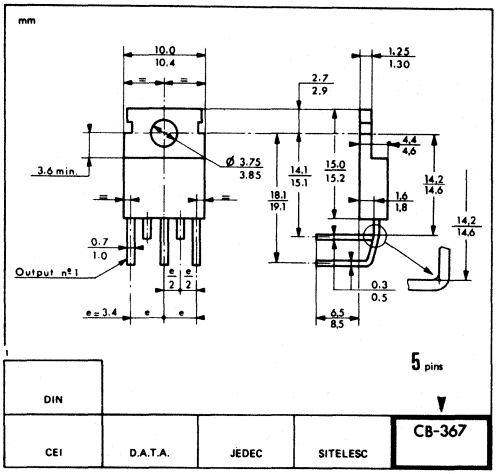
Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22 kΩ	Closed loop gain setting	Increase of gain	Decrease of gain
R2	680 Ω	Closed loop gain setting	Decrease of gain	Increase of gain
R3	22 kΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R4	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R5	≅ 3 R2	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C1	1 μF	Input DC decoupling		Increase of low frequencies cutoff
C2	22 μF	Inverting DC decoupling		Increase of low frequencies cutoff
C3, C4	0,1 μF	Supply voltage bypass		Danger of oscillation
C5, C6	100 μF	Supply voltage bypass		Danger of oscillation
C7	0,22 μF	Frequency stability		Danger of oscillation
C8	$\cong \frac{1}{2\pi\ BR1}$	Upper frequency cutoff	Small bandwidth	Larger bandwidth
D1, D2	1N 4001		To protect the device against output voltage spikes	



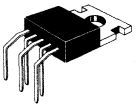
CASE CB-360



V SUFFIX
PLASTIC PACKAGE



CASE CB-367



H SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

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THOMSON COMPONENTS MICONDUCTEURS

TDA2030

14 W HI-FI AUDIO POWER AMPLIFIER

The TDA2030 is a monolithic integrated circuit in CB-360 or CB-367 package intended for use in audio amplifier.
Typically it provides 14 W ouput power (d = 0.5 %) at ± 14 V/4 Ω; at ± 14 V the guaranteed output power is 12 W on a 4 Ω load and 8 W on a 8 Ω (DIN 45500).
The TDA 2030 provides high output current (up to 3 A) and has very low harmonic and cross over distortion.
This device incorporates a short-circuit protection which automatically limits the dissipated power so as to keep the working point of the output transistors within their safe operating area.
A conventional thermal shut down system is also included.

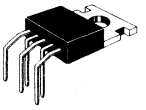
14 W HI-FI AUDIO POWER AMPLIFIER

CASES

CB-360

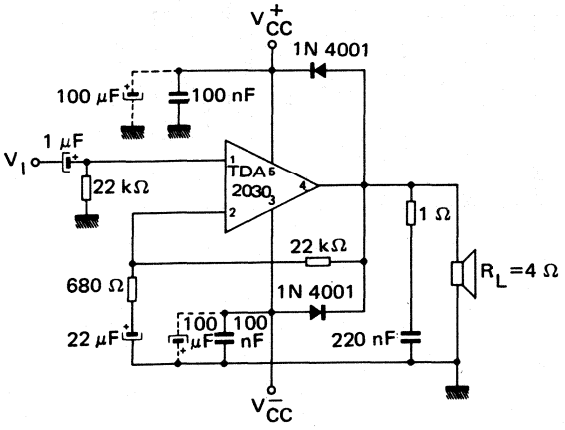
V SUFFIX
PLASTIC PACKAGE

CB-367

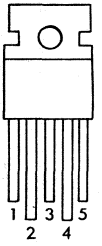


H SUFFIX
PLASTIC PACKAGE

TEST AND APPLICATION CIRCUIT



PIN ASSIGNMENT



1 Non inverting input
2 Inverting input
3 V_{CC} −
4 Output
5 V_{CC} +

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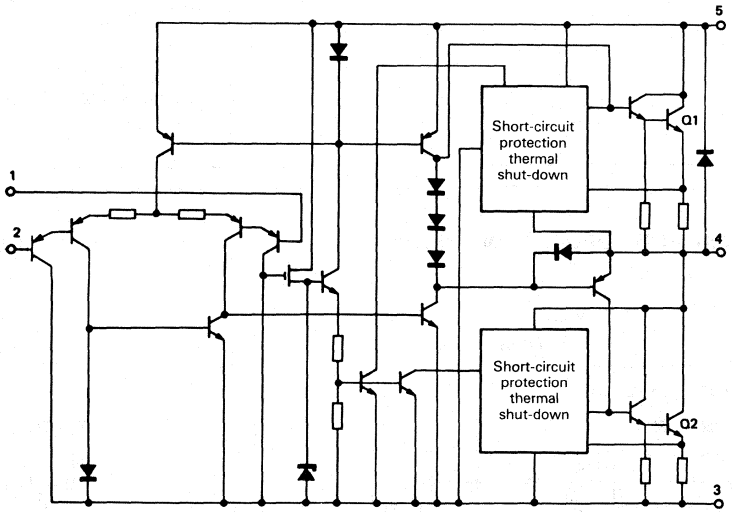
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	± 18	V
Input voltage	V_I	V_{CC}	
Differential input voltage	V_{ID}	± 15	V
Output peak current (internally limited)	I_O	3.5	A
Power dissipation T_{case} = 90 °C	P_{tot}	20	W
Operating junction temperature range	Tj	− 40 to + 150	°C
Storage temperature	T_{stg}	− 40 to + 150	°C

THERMAL CHARACTERISTICS

Test conditions	Symbol	Value	Unit
Maximum junction-case thermal resistance	$R_{th(j-c)}$	3	°C/W

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{CC} = ± 14 V; T_{amb} = 25 °C (refer to the test circuit) (Unless otherwise stated)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	± 6	–	± 18	V
Quiescent drain current (V_{CC} = ± 18 V)	I_{CC}	–	40	60	mA
Bias current (V_{CC} = ± 18 V)	I_B	–	0.2	2	μA
Input offset voltage (V_{CC} = ± 18 V)	V_{IO}	–	± 2	± 20	mV
Input offset current (V_{CC} = ± 18 V)	I_{IO}	–	± 20	± 200	nA
Output offset voltage (V_{CC} = ± 18 V)	V_O	–	± 2.5	± 22	mV
Output power	P_O				W
d = 0.5 %; A_V = 30 dB; 40 Hz ⩽ f ⩽ 15 kHz					
R_L = 4 Ω		12	14	–	
R_L = 8 Ω		8	9	–	
d = 10 %; A_V = 30 dB; f = 1 kHz					
R_L = 4 Ω		–	18	–	
R_L = 8 Ω		–	11	–	
Harmonic distortion	d				%
0.1 W ⩽ P_O ⩽ 12 W; R_L = 4 Ω; A_V = 30 dB; 40 Hz ⩽ f ⩽ 15 kHz		–	0.2	0.5	
0.1 W ⩽ P_O ⩽ 8 W; R_L = 8 Ω; A_V = 30 dB; 40 Hz ⩽ f ⩽ 15 kHz		–	0.1	0.5	
Input sensitivity (A_V = 30 dB; f = 1 kHz)	S				mV
P_O = 12 W; R_L = 4 Ω		–	215	–	
P_O = 8 W; R_L = 8 Ω		–	250	–	
Bandwidth (– 3 dB)	B				Hz
A_V = 30 dB; P_O = 12 W; R_L = 4 Ω			10 to 140.000		
Input resistance Pin 1	R_I	0.5	5	–	MΩ
Voltage gain (f = 1 kHz)	A_V				dB
Open loop		–	90	–	
Closed loop		29.5	30	30.5	
Input noise voltage (R_L = 4 Ω)	V_n				μV
Test equipment bandwith (– 3 dB) = 10 to 25.000 Hz		–	3	10	
Input noise current (R_L = 4 Ω)	i_n				pA
Test equipment bandwith (– 3 dB) = 10 to 25.000 Hz		–	80	200	
Supply voltage rejection ratio	SVR				dB
R_L = 4 Ω; A_V = 30 dB; R_G = 22 kΩ; V_{ripple} = 0.5 V_{eff} f_{ripple} = 100 Hz		40	50	–	
Drain current	I_{CC}				mA
P_O = 14 W; R_L = 4 Ω		–	900	–	
P_O = 9 W; R_L = 8 Ω		–	515	–	
Thermal shut-down case temperature (P_{tot} = 12 W)	T_{case}	110	–	–	°C

FIG. 1 – TYPICAL OUTPUT POWER VERSUS SUPPLY VOLTAGE

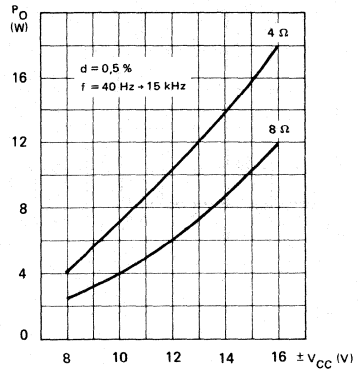


FIG. 2 – TYPICAL OUTPUT POWER VERSUS SUPPLY VOLTAGE

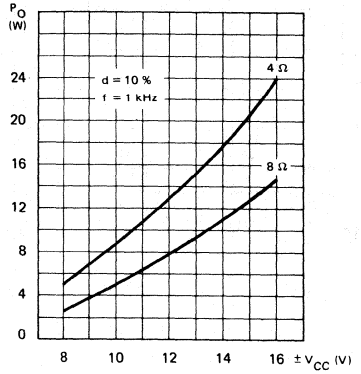


FIG. 3 – TYPICAL DISTORTION VERSUS OUTPUT POWER

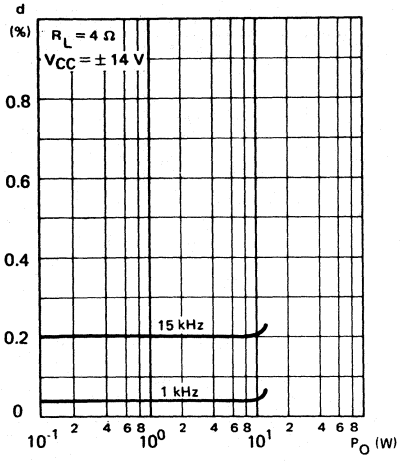


FIG. 4 – TYPICAL DISTORTION VERSUS OUTPUT POWER

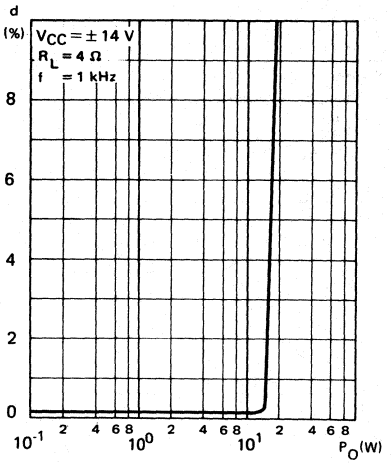


FIG. 5 – TYPICAL DISTORTION VERSUS OUTPUT POWER

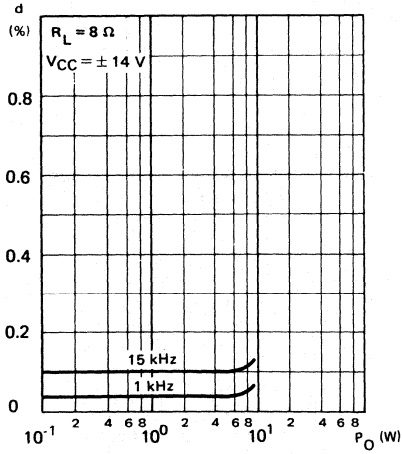


FIG. 6 – TYPICAL DISTORTION VERSUS OUTPUT POWER

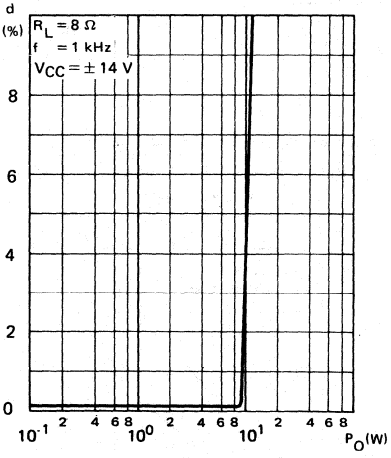


FIG. 7 – TYPICAL DISTORTION VERSUS FREQUENCY

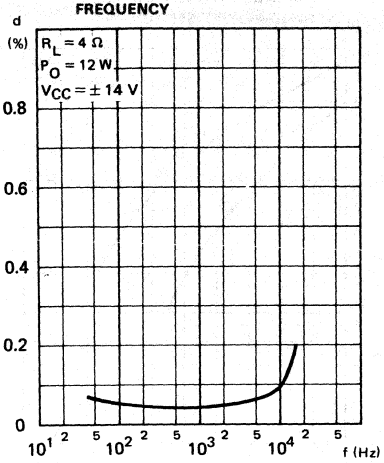


FIG. 8 – TYPICAL DISTORTION VERSUS FREQUENCY

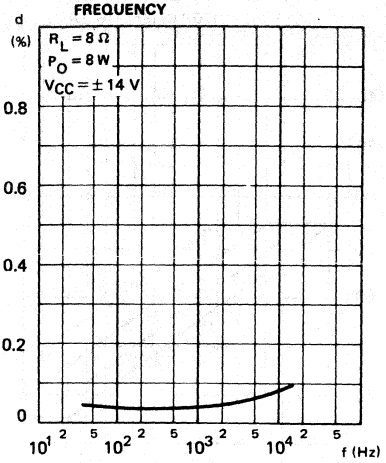


FIG. 9 – TYPICAL SENSITIVITY VERSUS OUTPUT POWER

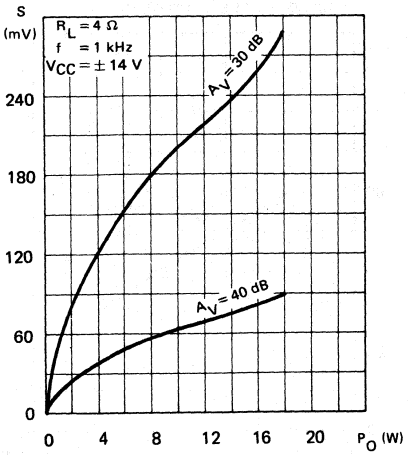


FIG. 10 – TYPICAL SENSITIVITY VERSUS OUTPUT POWER

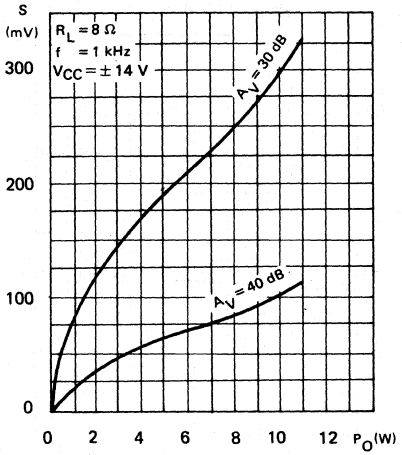


FIG. 11 – FREQUENCY RESPONSE WITH DIFFERENT VALUES OF THE ROLLOFF CAPACITOR C8 (SEE FIG. 17)

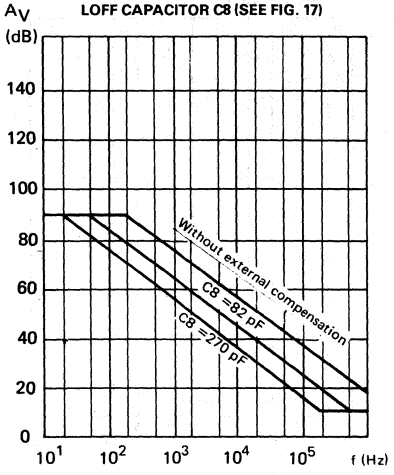


FIG. 12 – TYPICAL VALUE OF C8 VERSUS VOLTAGE GAIN FOR DIFFERENT BANDWIDTHS (SEE FIG. 17)

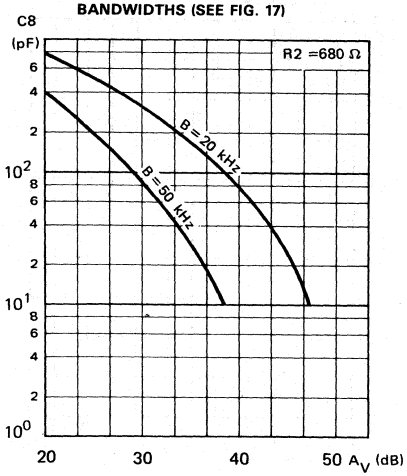


FIG. 13 – QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE

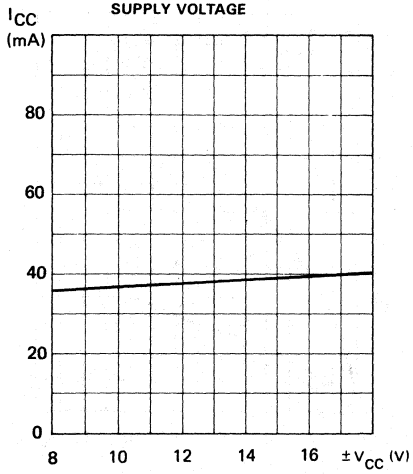


FIG. 14 – SUPPLY VOLTAGE REJECTION RATIO VERSUS VOLTAGE GAIN

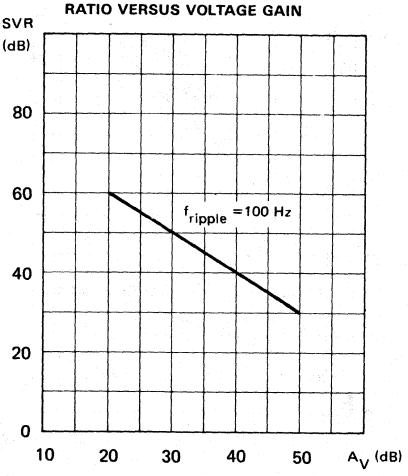


FIG. 15 – POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER

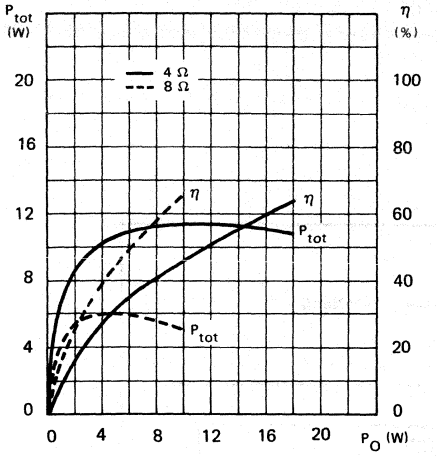


FIG. 16 – MAXIMUM POWER DISSIPATION VERSUS SUPPLY VOLTAGE (SINE WAVE OPERATION)

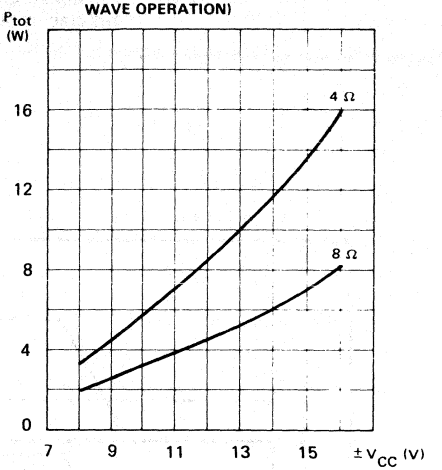
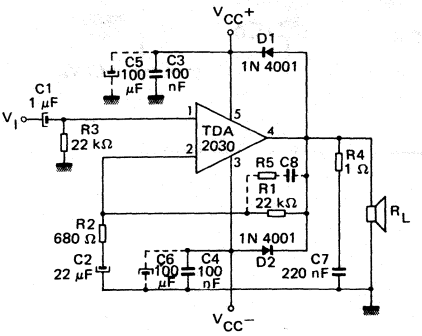


FIG. 17 – TYPICAL AMPLIFIER WITH SPLIT POWER SUPPLY



R5 ≃ 3 R2
C8 = See figure 12

FIG. 18 – TYPICAL AMPLIFIER WITH SINGLE POWER SUPPLY

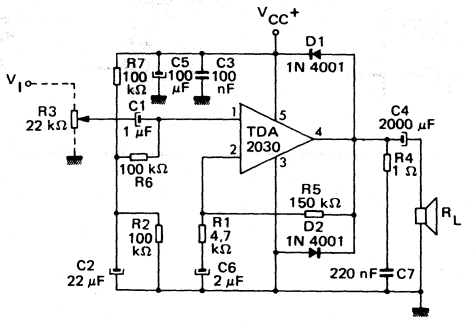


FIG. 19 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 17

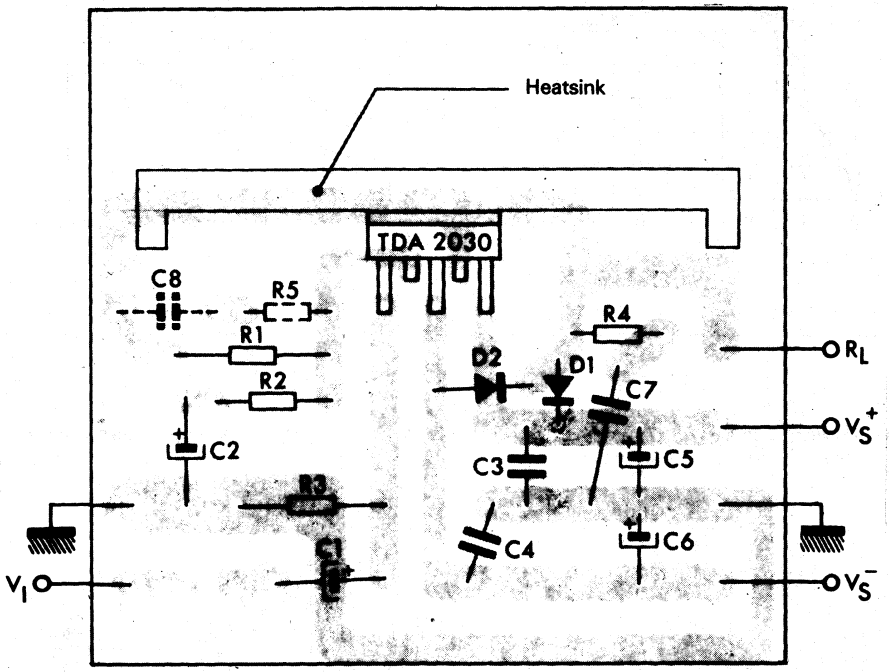


FIG. 20 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 18

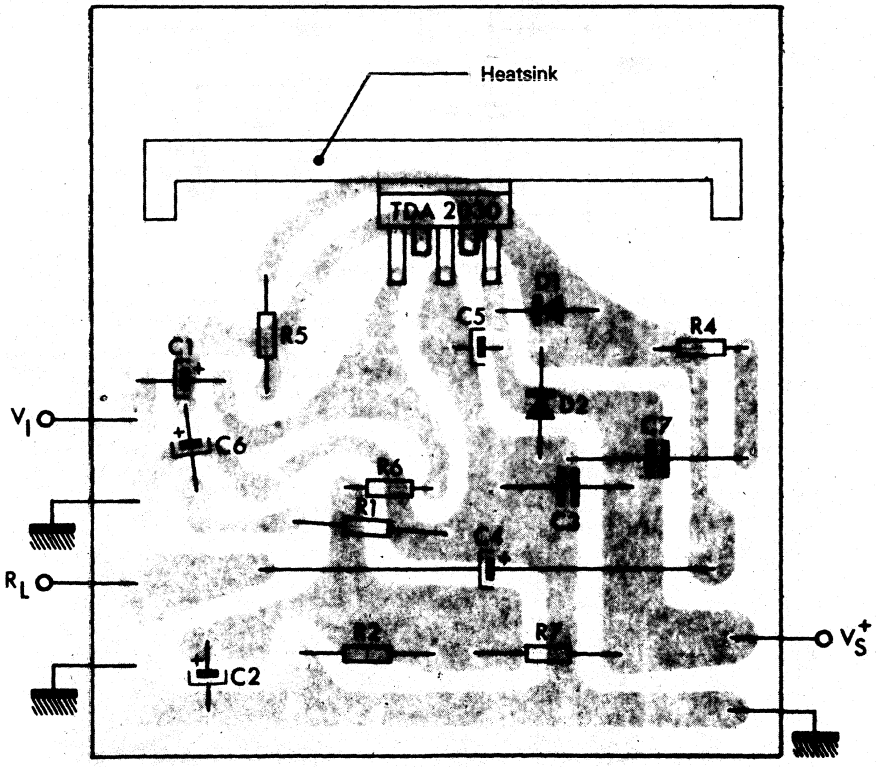
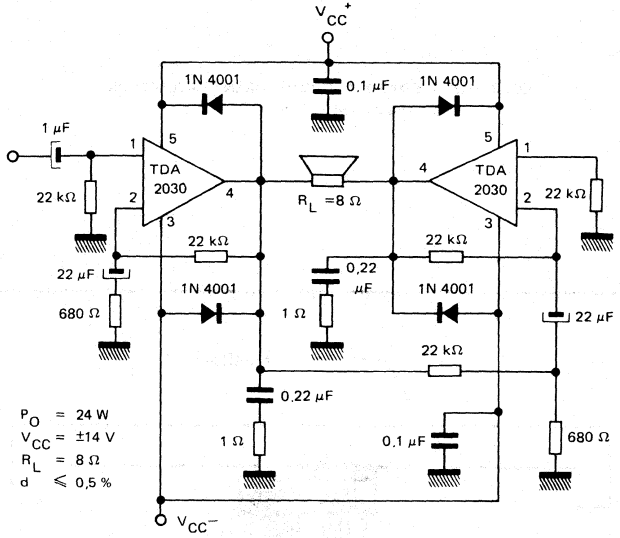


FIG. 21 – TYPICAL BRIDGE AMPLIFIER CONFIGURATION WITH SPLIT POWER SUPPLY



SHORT-CIRCUIT PROTECTION

The TDA 2030 has an internal circuit which limits the currents of the output transistors.

Figure 22 shows that the maximum output current is a function of the collector emitter voltage.

Hence, the output transistors work within their safe operating area (figure 23).

This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2030 is thus protected against temporary over-loads or short-circuit. Should the short-circuit exist for a longer time, the thermal shut-down protection keeps the junction temperature within safe limits.

FIG. 22 – MAXIMUM OUTPUT CURRENT VERSUS VOLTAGE (V_{CE}) ACROSS EACH OUTPUT TRANSISTOR

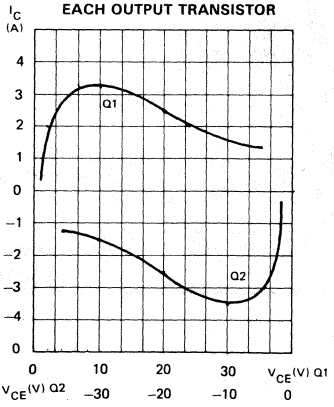
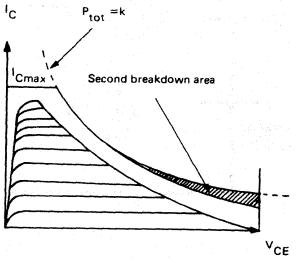


FIG. 23 – SAFE OPERATIONS AREA AND COLLECTOR CHARACTERISTICS OF THE PROTECTED POWER TRANSISTOR



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1 – An overload on the output (even if it is permanent) or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150 °C.

2 – The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150 °C, the thermal shut-down simply reduces the power dissipation and the current consumption.

FIG. 24 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE (R_L = 4 Ω)

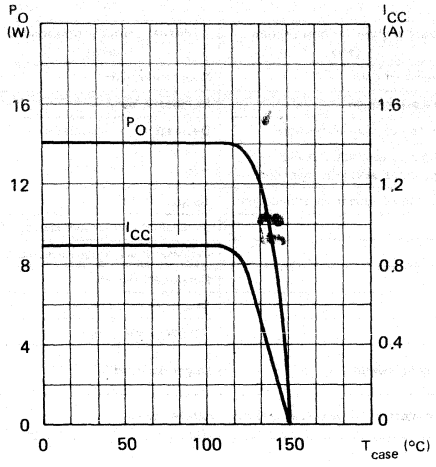


FIG. 25 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE (R_L = 8 Ω)

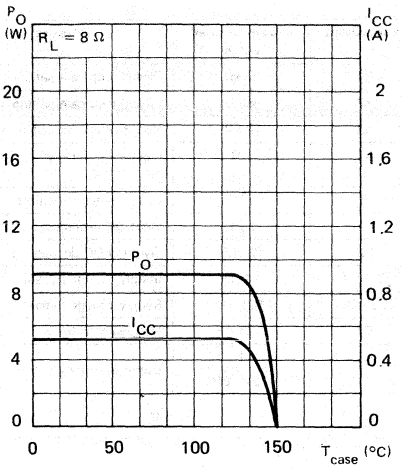
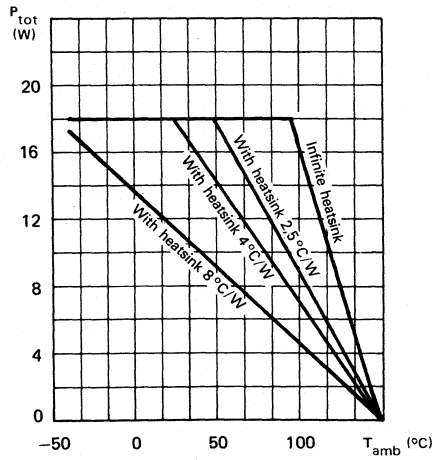


FIG. 26 – MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); figure 26 shows this dissipable power as a function of ambient temperature for different thermal resistance.

PRACTICAL CONSIDERATIONS

PRINTED CIRCUIT BOARD

The layout in figure 19 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

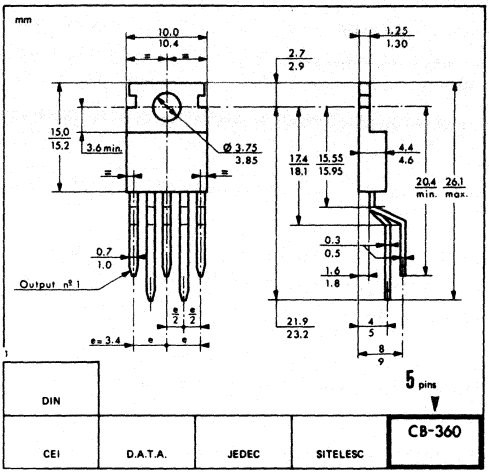
ASSEMBLY SUGGESTION

No electrical isolation needs to be used between the package and the heatsink with single supply voltage configuration.

EXTERNAL COMPONENTS

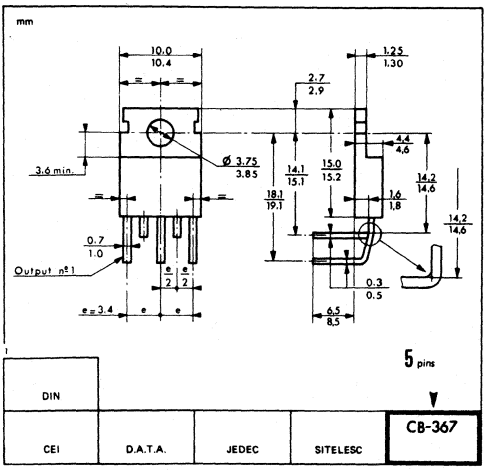
The recommended values of the external components are those shown on application circuit of figure 17. Different values can be used. The following table can help the designer.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22 kΩ	Closed loop gain setting	Increase of gain	Decrease of gain
R2	680 Ω	Closed loop gain setting	Decrease of gain	Increase of gain
R3	22 kΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R4	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R5	≅ 3 R2	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C1	1 μF	Input DC decoupling		Increase of low frequencies cutoff
C2	22 μF	Inverting DC decoupling		Increase of low frequencies cutoff
C3, C4	0.1 μF	Supply voltage bypass		Danger of oscillation
C5, C6	100 μF	Supply voltage bypass		Danger of oscillation
C7	0.22 μF	Frequency stability		Danger of oscillation
C8	$\cong \frac{1}{2\pi\ BR1}$	Upper frequency cutoff	Small bandwidth	Larger bandwidth
D1, D2	1N 4001		To protect the device against output voltage spikes	

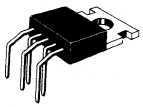


CASE CB-360

V SUFFIX
PLASTIC PACKAGE



CASE CB-367



H SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

Printed in France

TDA2030A42

14 W HI-FI AUDIO POWER AMPLIFIER

The TDA2030A42 is a monolithic integrated circuit in CB-360 or CB-367 package intended for use in audio amplifier .
Typically it provides 14 W ouput power (d = 0.5 %) at ± 14 V/4 Ω; at ± 14 V the guaranteed output power is 12 W on a 4 Ω load and 8 W on a 8 Ω (DIN 45500).
The TDA 2030 A42 provides high output current (up to 3 A) and has very low harmonic and cross over distortion.
This device incorporates a short-circuit protection which automatically limits the dissipated power so as to keep the working point of the output transistors within their safe operating area.
A conventional thermal shut down system is also included.
With V_{CC} max = 42 V the TDA2030A42 is adviced for non-regulated supply applications.

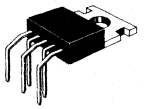
14 W HI-FI AUDIO POWER AMPLIFIER

CASES

CB-360

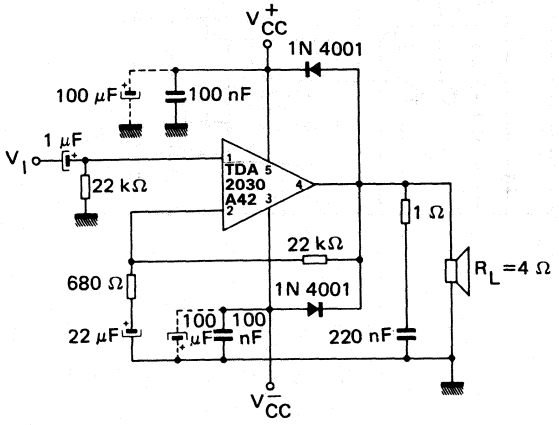
V SUFFIX
PLASTIC PACKAGE

CB-367

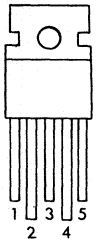


H SUFFIX
PLASTIC PACKAGE

TEST AND APPLICATION CIRCUIT



PIN ASSIGNMENT



1 Non inverting input
2 Inverting input
3 V_{CC} −
4 Output
5 V_{CC} +

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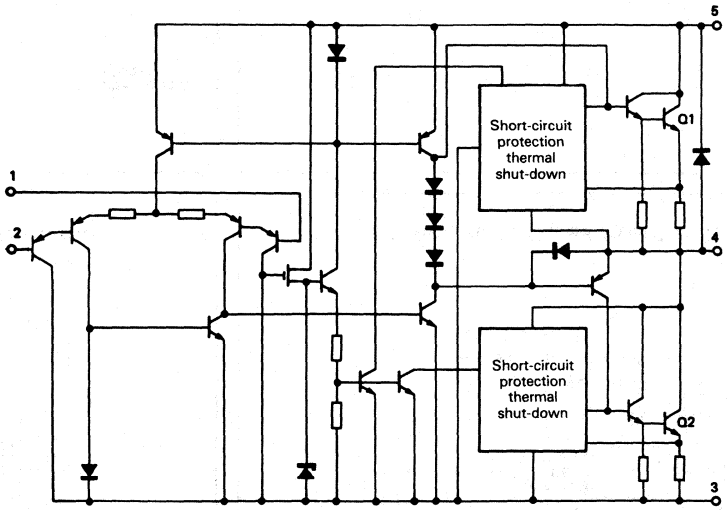
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	± 21	V
Input voltage	V_I	V_{CC}	
Differential input voltage	V_{ID}	± 15	V
Output peak current (internally limited)	I_O	3.5	A
Power dissipation T_{case} = 90 °C	P_{tot}	20	W
Operating junction temperature range	T_j	— 40 to + 150	°C
Storage temperature	T_{stg}	— 40 to + 150	°C

THERMAL CHARACTERISTICS

Test conditions	Symbol	Value	Unit
Maximum junction-case thermal resistance	$R_{th(j-c)}$	3	°C/W

SCHEMATIC DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = ± 14 V; T_{amb} = 25 °C unless otherwise specified (refer to the test circuit)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	± 6	–	± 18	V
Quiescent drain current (V_{CC} = ± 21 V)	I_{CC}	–	60	105	mA
Bias current (V_{CC} = ± 18 V)	I_B	–	0.2	2	μA
Input offset voltage (V_{CC} = ± 18 V)	V_{IO}	–	± 2	± 20	mV
Input offset current (V_{CC} = ± 18 V)	I_{IO}	–	± 20	± 200	nA
Output offset voltage (V_{CC} = ± 18 V)	V_O	–	± 2.5	± 22	mV
Output power	P_O				W
d = 0.5 %; A_V = 30 dB; 40 Hz ⩽ f ⩽ 15 kHz					
R_L = 4 Ω		12	14	–	
R_L = 8 Ω		8	9	–	
d = 10 %; A_V = 30 dB; f = 1 kHz					
R_L = 4 Ω		–	18	–	
R_L = 8 Ω		–	11	–	
Harmonic distortion	d				%
0.1 W ⩽ P_O ⩽ 12 W; R_L = 4 Ω; A_V = 30 dB; 40 Hz ⩽ f ⩽ 15 kHz		–	0.2	0.5	
0.1 W ⩽ P_O ⩽ 8 W; R_L = 8 Ω; A_V = 30 dB; 40 Hz ⩽ f ⩽ 15 kHz		–	0.1	0.5	
Input sensitivity (A_V = 30 dB; f = 1 kHz)	S				mV
P_O = 12 W; R_L = 4 Ω		–	215	–	
P_O = 8 W; R_L = 8 Ω		–	250	–	
Bandwidth (– 3 dB)	B				Hz
A_V = 30 dB; P_O = 12 W: R_L = 4 Ω			10 to 140.000		
Input resistance Pin 1	R_I	0.5	5	–	MΩ
Voltage gain (f = 1 kHz)	A_V				dB
Open loop		–	90	–	
Closed loop		29.5	30	30.5	
Input noise voltage (R_L = 4 Ω)	V_n				μV
Test equipment bandwith (– 3 dB) = 10 to 25.000 Hz		–	3	10	
Input noise current (R_L = 4 Ω)	i_n				pA
Test equipment bandwith (– 3 dB) = 10 to 25.000 Hz		–	80	200	
Supply voltage rejection ratio	SVR				dB
R_L = 4 Ω; A_V = 30 dB; R_G = 22 kΩ; V_{ripple} = 0.5 V_{eff} f_{ripple} = 100 Hz		40	50	–	
Drain current	I_{CC}				mA
P_O = 14 W; R_L = 4 Ω		–	900	–	
P_O = 9 W; R_L = 8 Ω		–	515	–	
Thermal shut-down case temperature (P_{tot} = 12 W)	T_{case}	110	–	–	°C

FIG. 1 – TYPICAL OUTPUT POWER VERSUS SUPPLY VOLTAGE

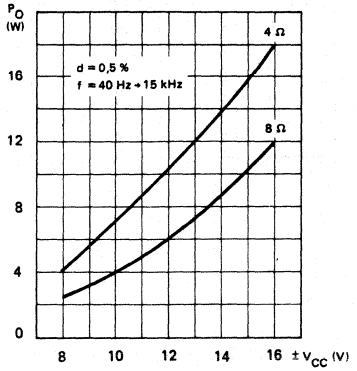


FIG. 2 – TYPICAL OUTPUT POWER VERSUS SUPPLY VOLTAGE

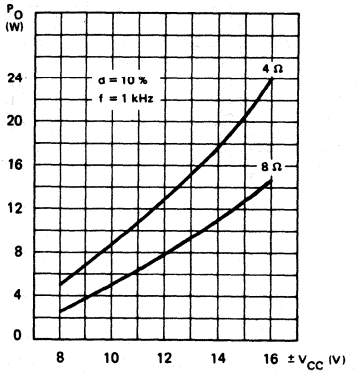


FIG. 3 – TYPICAL DISTORTION VERSUS OUTPUT POWER

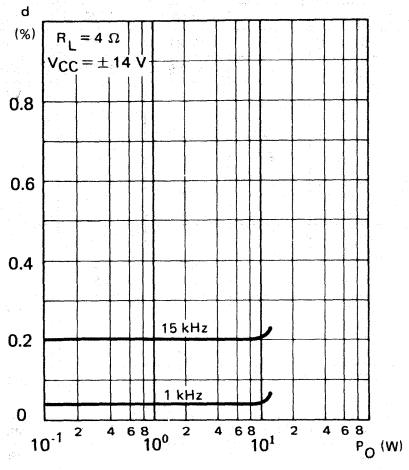


FIG. 4 – TYPICAL DISTORTION VERSUS OUTPUT POWER

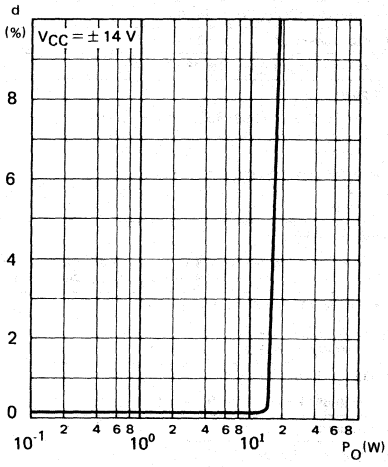


FIG. 5 – TYPICAL DISTORTION VERSUS OUTPUT POWER

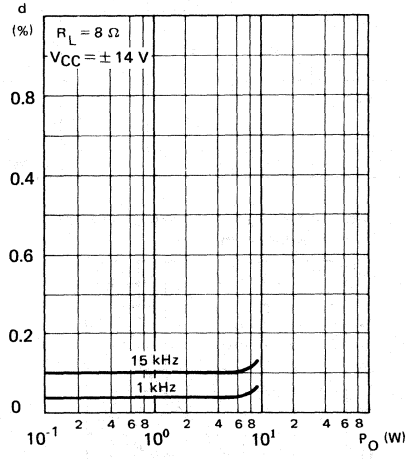


FIG. 6 – TYPICAL DISTORTION VERSUS OUTPUT POWER

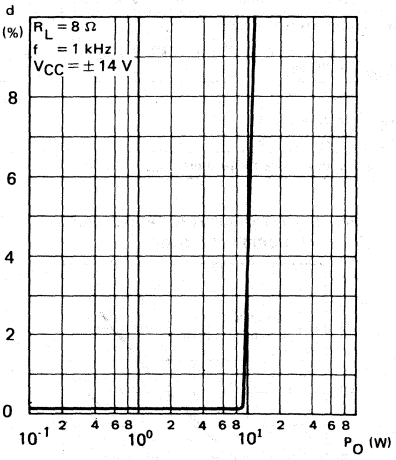


FIG. 7 – TYPICAL DISTORTION VERSUS FREQUENCY

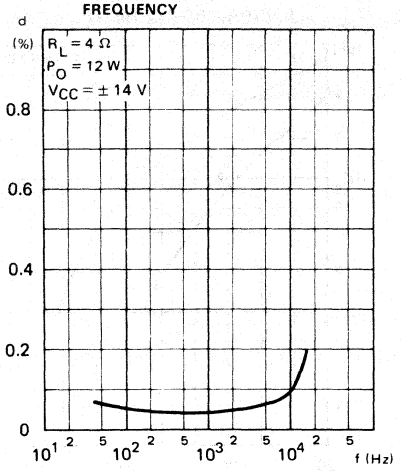


FIG. 8 – TYPICAL DISTORTION VERSUS FREQUENCY

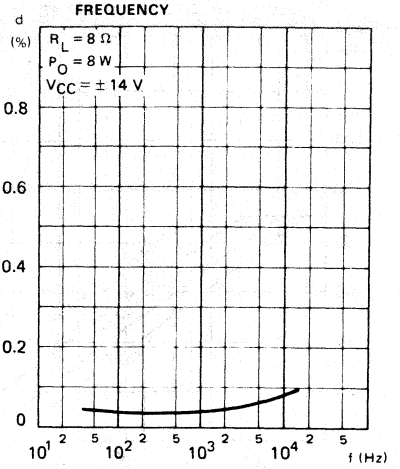


FIG. 9 – TYPICAL SENSITIVITY VERSUS OUTPUT POWER

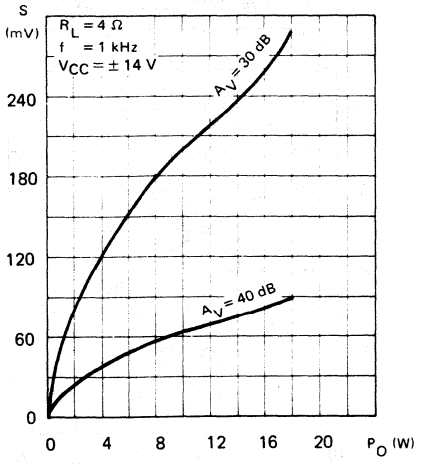


FIG. 10 – TYPICAL SENSITIVITY VERSUS OUTPUT POWER

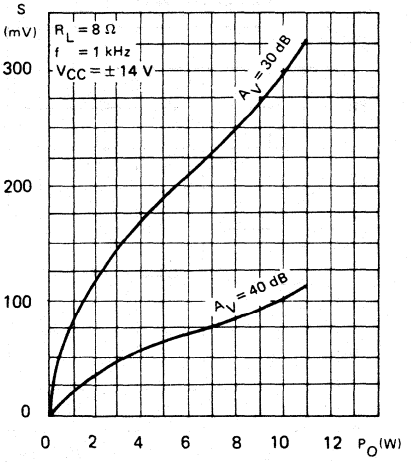


FIG. 11 – FREQUENCY RESPONSE WITH DIFFERENT VALUES OF THE ROLLOFF CAPACITOR C8 (SEE FIG. 17)

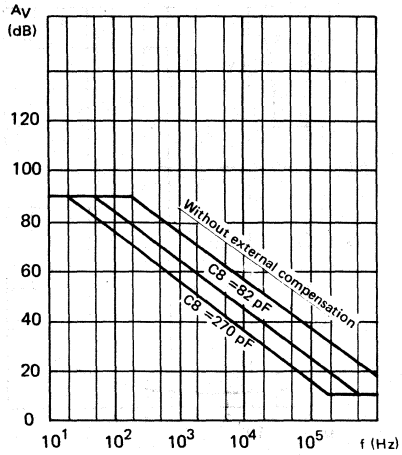


FIG. 12 – TYPICAL VALUE OF C8 VERSUS VOLTAGE GAIN FOR DIFFERENT BANDWIDTHS (SEE FIG. 17)

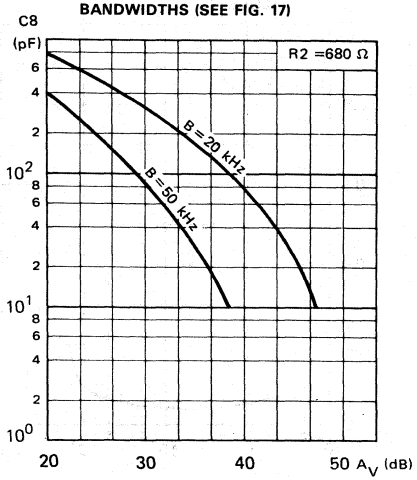


FIG. 13 – QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE

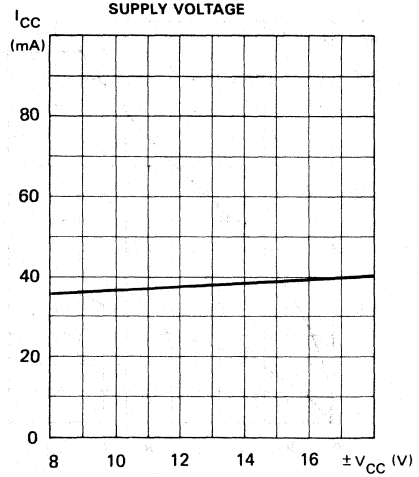


FIG. 14 – SUPPLY VOLTAGE REJECTION RATIO VERSUS VOLTAGE GAIN

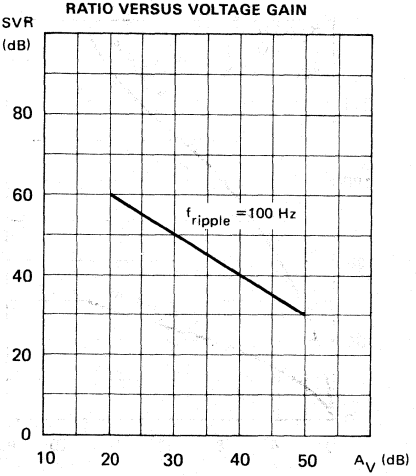


FIG. 15 – POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER

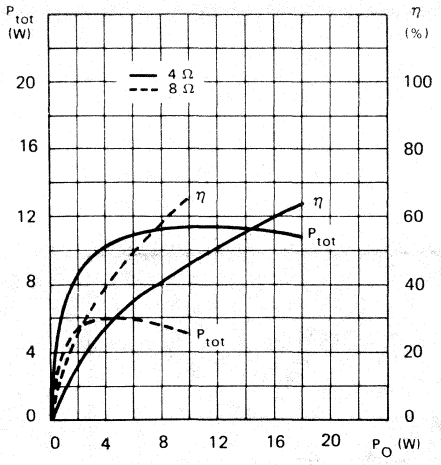


FIG. 16 – MAXIMUM POWER DISSIPATION VERSUS SUPPLY VOLTAGE (SINE WAVE OPERATION)

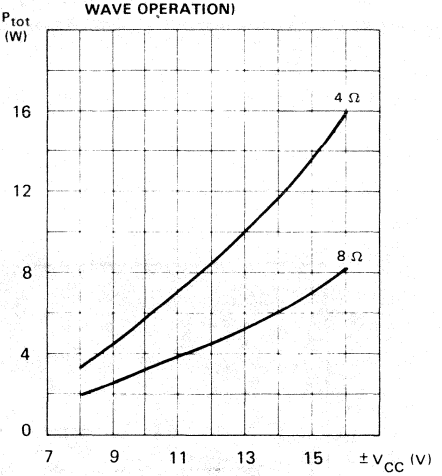
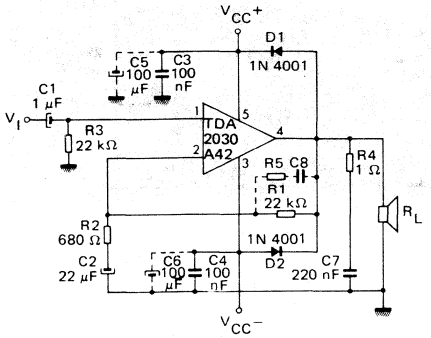


FIG. 17 – TYPICAL AMPLIFIER WITH SPLIT POWER SUPPLY



R5 ≃ 3 R2
C8 = See figure 12

FIG. 18 – TYPICAL AMPLIFIER WITH SINGLE POWER SUPPLY

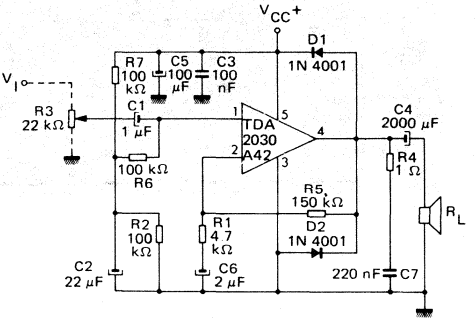


FIG. 19 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 17

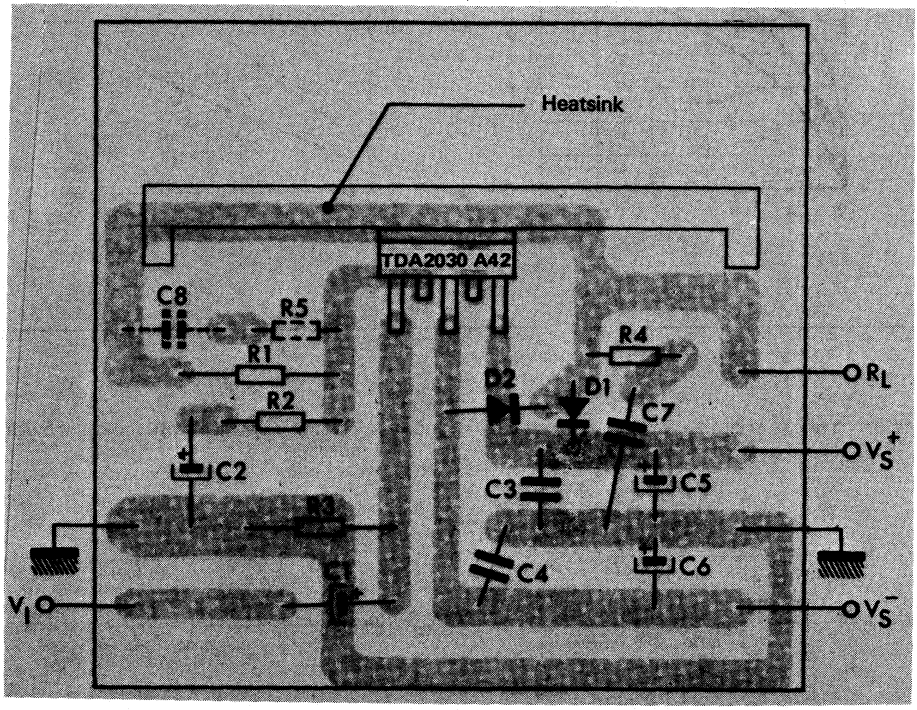


FIG. 20 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 18

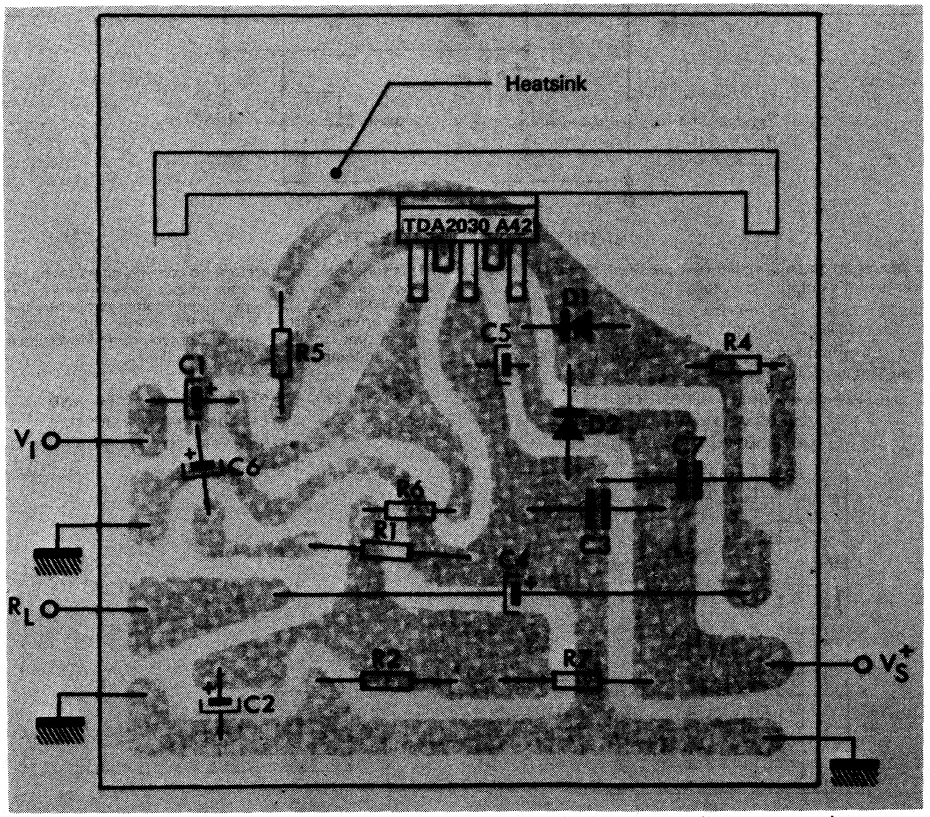
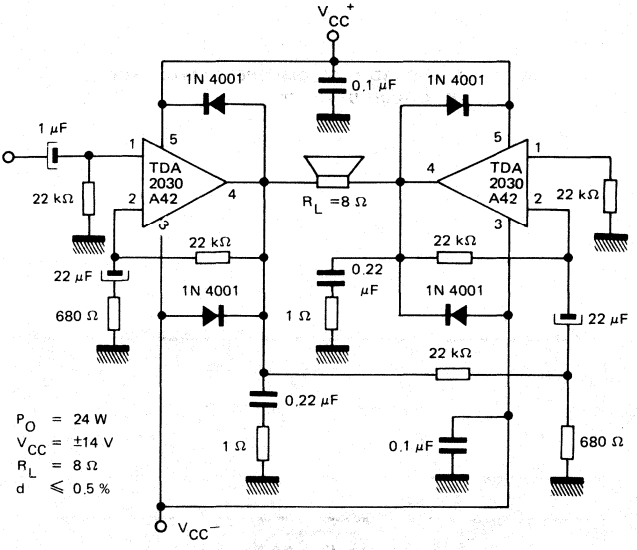


FIG. 21 – TYPICAL BRIDGE AMPLIFIER CONFIGURATION WITH SPLIT POWER SUPPLY



SHORT-CIRCUIT PROTECTION

The TDA 2030 A42 has an internal circuit which limits the currents of the output transistors.

Figure 22 shows that the maximum output current is a function of the collector emitter voltage.

Hence, the output transistors work within their safe operating area (figure 23).

This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2030 A42 is thus protected against temporary overloads or short-circuit. Should the short-circuit exist for a longer time, the thermal shut-down protection keeps the junction temperature within safe limits.

FIG. 22 – MAXIMUM OUTPUT CURRENT VERSUS VOLTAGE (V_{CE}) ACROSS EACH OUTPUT TRANSISTOR

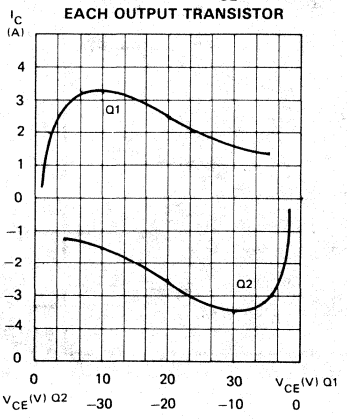
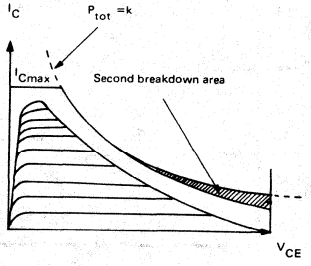


FIG. 23 – SAFE OPERATIONS AREA AND COLLECTOR CHARACTERISTICS OF THE PROTECTED POWER TRANSISTOR



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1 – An overload on the output (even if it is permanent) or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150 °C.

2 – The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150 °C, the thermal shut-down simply reduces the power dissipation and the current consumption.

FIG. 24 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE (R_L = 4 Ω)

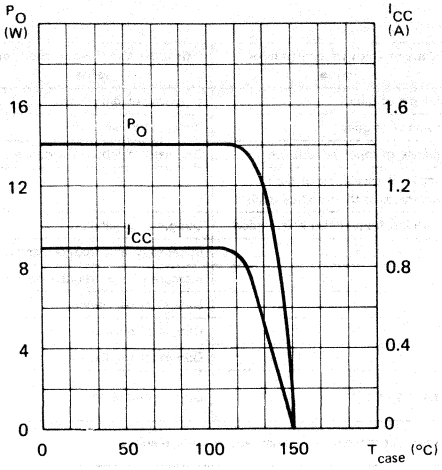


FIG. 25 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE (R_L = 8 Ω)

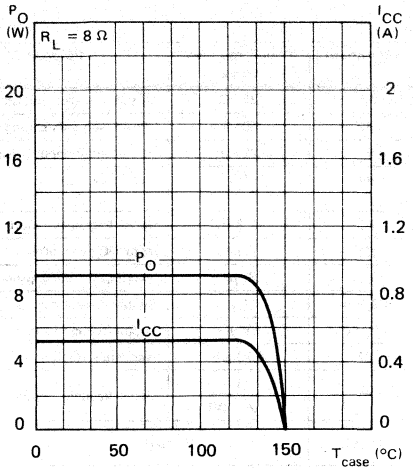
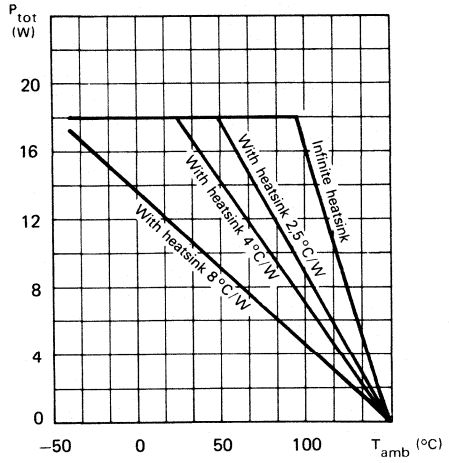


FIG. 26 – MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); figure 26 shows this dissipable power as a function of ambient temperature for different thermal resistance.

PRACTICAL CONSIDERATIONS

PRINTED CIRCUIT BOARD

The layout in figure 19 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

ASSEMBLY SUGGESTION

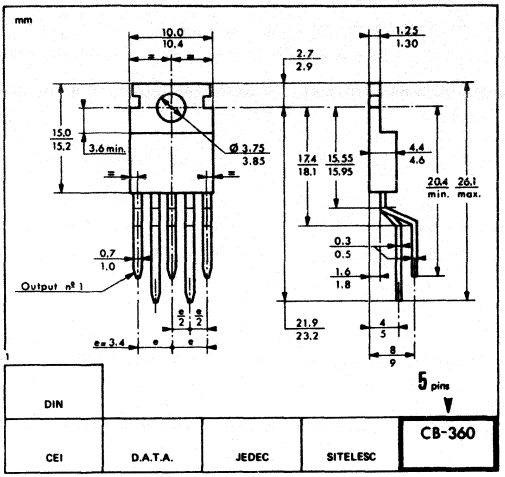
No electrical isolation needs to be used between the package and the heatsink with single supply voltage configuration.

EXTERNAL COMPONENTS

The recommended values of the external components are those shown on application circuit of figure 17. Different values can be used. The following table can help the designer.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22 kΩ	Closed loop gain setting	Increase of gain	Decrease of gain
R2	680 Ω	Closed loop gain setting	Decrease of gain	Increase of gain
R3	22 kΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R4	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R5	≅ 3 R2	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C1	1 μF	Input DC decoupling		Increase of low frequencies cutoff
C2	22 μF	Inverting DC decoupling		Increase of low frequencies cutoff
C3, C4	0,1 μF	Supply voltage bypass		Danger of oscillation
C5, C6	100 μF	Supply voltage bypass		Danger of oscillation
C7	0,22 μF	Frequency stability		Danger of oscillation
C8	$\cong \frac{1}{2\pi\ BR1}$	Upper frequency cutoff	Small bandwidth	Larger bandwidth
D1, D2	1N 4001		To protect the device against output voltage spikes	

PHYSICAL DIMENSIONS



CASE CB-360

V SUFFIX
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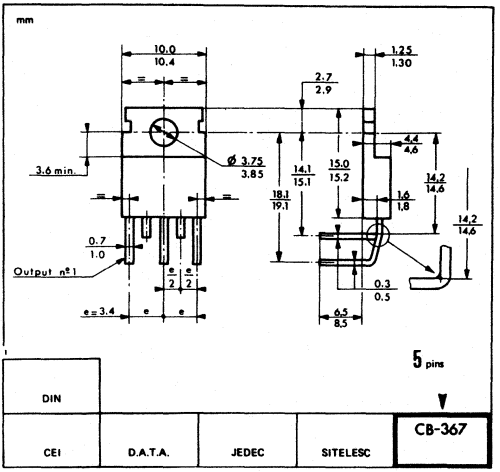
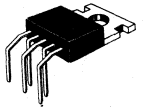


CASE CB-367



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NOTES

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TDA2040

22 W HI-FI AUDIO POWER AMPLIFIER

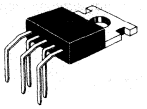
The TDA2040 is a monolithic integrated circuit in CB-360 or CB-367 package specially intended for use as audio High Fidelity amplifier.

It provides a typical 22 W output power (d = 0.5 %) at V_{CC} ± 16 V/4 Ω

The TDA 2040 provides high output current and has very low harmonic and cross-over distortion. An internal circuitry protects the output power stage against over heating (thermal shut-down system), and short-circuit, limiting automatically the dissipated power so as to keep the working point of the output transistors within their safe operating area.

22 W HIFI AUDIO POWER AMPLIFIER

CASES **CB-367**



H SUFFIX
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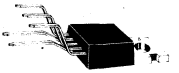
CB-360



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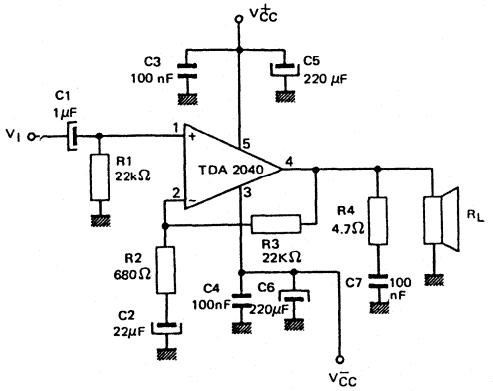
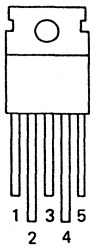
APPLICATION CIRCUIT



PIN ASSIGNMENT



1 - Non inverting input
2 - Inverting input
3 - V_{CC}–
4 - Output
5 - V_{CC} +

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	± 20	V
Input voltage	V_I	V_{CC}	V
Differential input voltage	V_{ID}	± 15	V
Output peak current (internally limited)	I_O	4	A
Total power dissipation ($T_{case} = 75°C$)	P_{tot}	25	W
Junction temperature	T_j	− 40 to + 150	°C
Storage temperature	T_{stg}	− 40 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Maximum junction-case thermal resistance	$R_{th(j-c)}$	3	°C/W

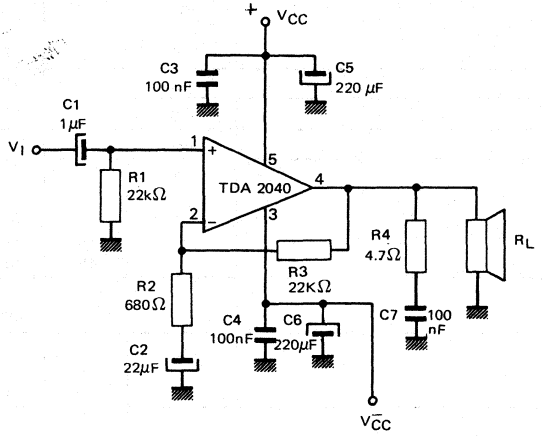
ELECTRICAL OPERATING CHARACTERISTICS

$V_{CC} = \pm 16$ V $T_{amb} = +25°C$ unless otherwise specified (refer to the test circuit)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	±2.5		±20	V
Quiescent drain current	I_{CC}				
$V_{CC} = \pm 4.5$ V		–	–	30	mA
$V_{CC} = \pm 20$ V		–	45	100	mA
Input bias current	I_{IB}	–	0.3	1	μA
Input offset voltage	V_{IO}	–	±2	±20	mV
Input offset voltage	I_{IO}	–	–	±200	nA
Output power	P_O				
d = 0.5 % $T_{case} = +60°C$					
f = 1 kHz, $R_L = 4\ \Omega$		20	22	–	W
$R_L = 8\ \Omega$		–	12	–	W
f = 15 kHz $R_L = 4\ \Omega$		15	18	–	W
Bandwith (– 3 dB)	B				
$P_o = 1$ W, $R_L = 4\ \Omega$		–	100	–	kHz
Voltage gain	A_V				
F = 1 kHz open loop		–	80	–	dB
closed loop		29.5	30	30.5	dB
Harmonic distorsion	d				
$R_L = 4\ \Omega$, $P_o = 0.1$ to 10 W					
f = 1 kHz		–	0.03	–	%
40 Hz ≤ f ≤ 15 kHz		–	0.08	–	%
Input noise voltage	V_n				
B = curve A		–	2	–	μV
B = 22 Hz to 22 kHz		–	3	–	μV
Input noise current	I_n				
B = curve A		–	50	–	pA
B = 22 Hz to 22 kHz		–	80	–	pA
Input resistance (pin 1)	R_I	0.5	5	–	MΩ
Supply voltage rejection ratio	S_{VR}				
$R_L = 4\ \Omega$ $A_V = 30$ dB					
$R_G = 22$ kΩ f = 100 Hz					
Vripple = 0.5 Vrms		40	48	–	dB
Efficiency	η				
F = 1 kHz, $P_o = 22$ W - $R_L = 4\ \Omega$		–	63	–	%
$P_o = 12$ W - $R_L = 8\ \Omega$		–	66	–	%
Thermal shut-down junction temperature	T_j	–	145	–	°C

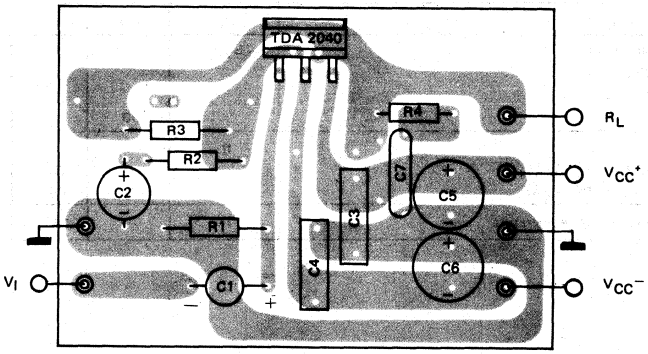
APPLICATION INFORMATION

SPLIT POWER SUPPLY



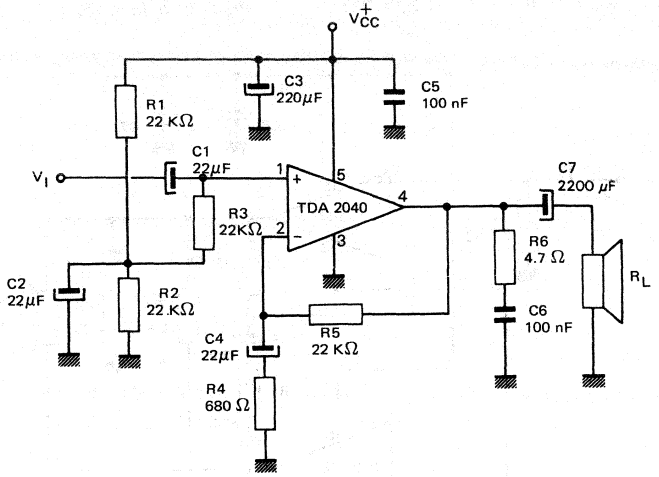
V_{CC} = ± 16 V R_L = 4 Ω P_O = 22 W (typique) (d : 0.5%)

P.C. BOARD AND COMPONENTS LAYOUT



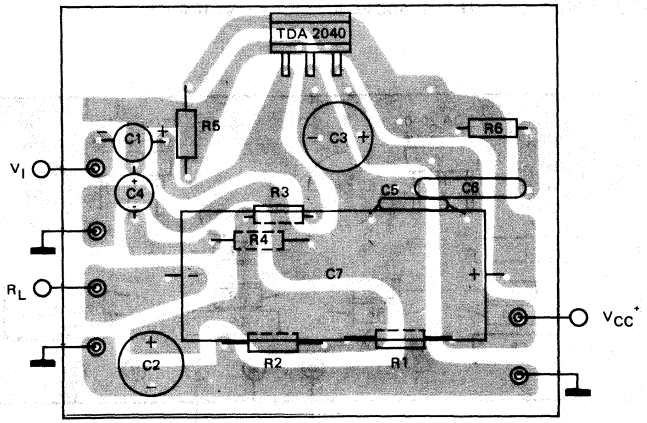
APPLICATION INFORMATION

AMPLIFIER WITH SINGLE POWER SUPPLY



$V_{CC}^+ = 32$ V $\quad R_L = 4\Omega$ $\quad P_O = 22$ W (typique) (d : 0.5%)

P.C. BOARD AND COMPONENTS LAYOUT FOR ABOVE APPLICATION CIRCUIT

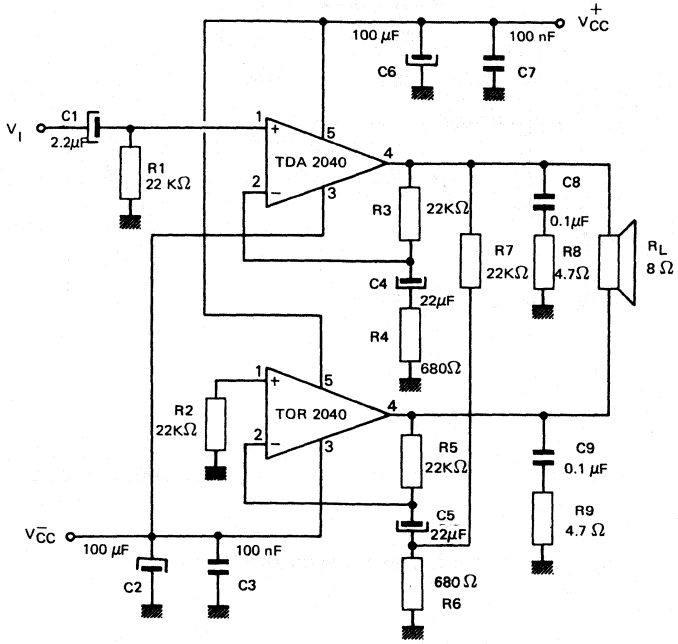


note : with highly inductive loads protection diodes may be necessary.

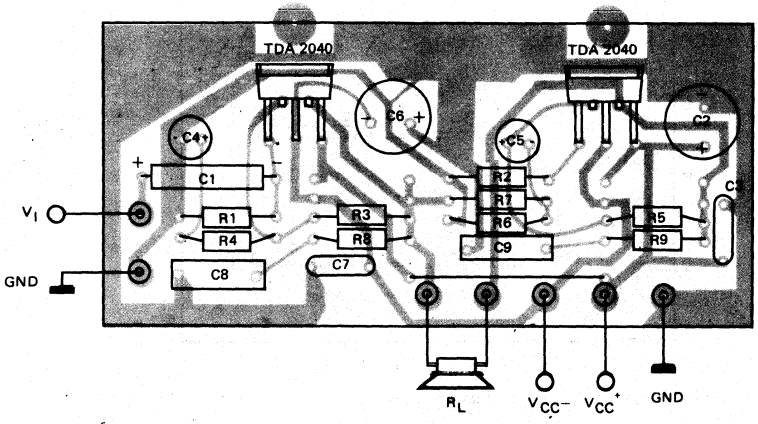
APPLICATION INFORMATION

30 W BRIDGE AMPLIFIER WITH SPLIT POWER SUPPLY

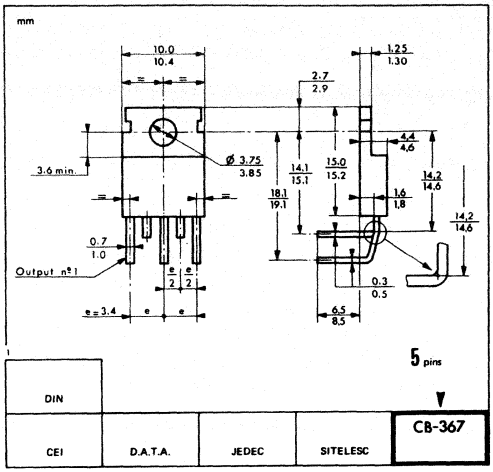
V_{CC} = ± 16 V R_L = 8 Ω P_O > 30 W (d : 0.5%)



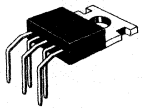
P.C. BOARD AND COMPONENTS LAYOUT FOR ABOVE APPLICATION CIRCUIT



PHYSICAL DIMENSIONS



CB-367



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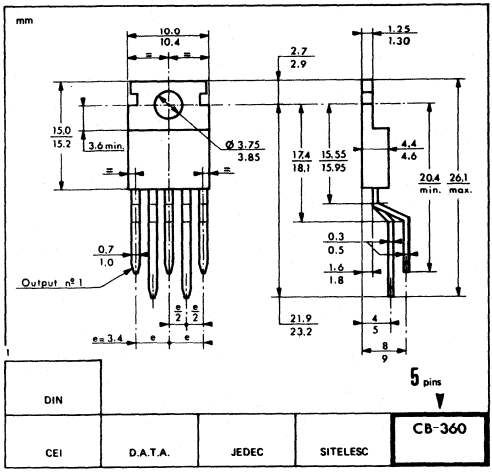

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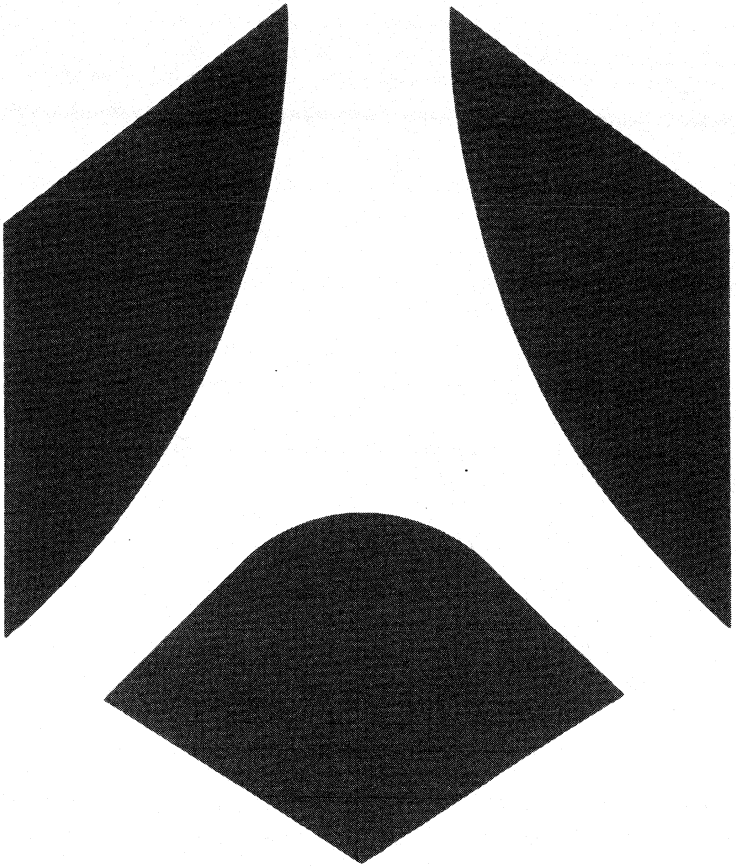
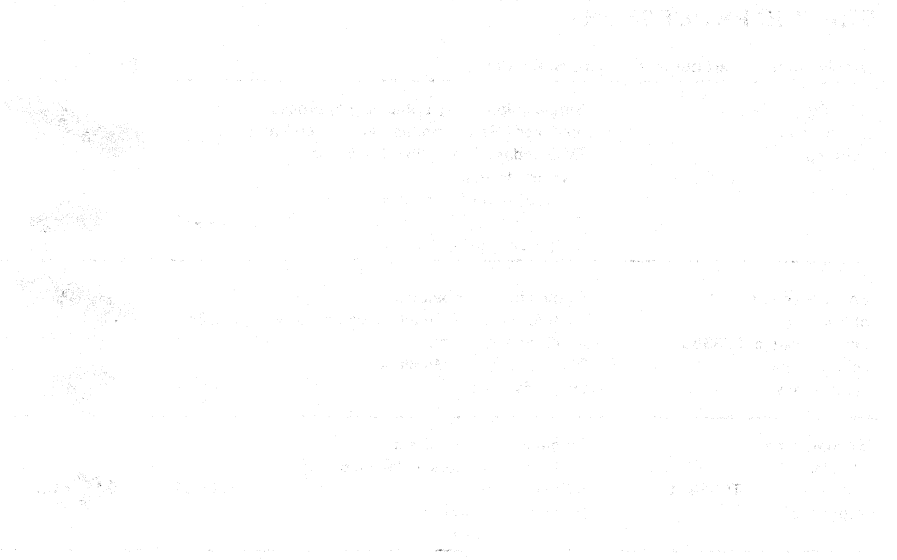


Graphic processors

GRAPHIC PROCESSORS

Application	Part number	Characteristics		Package	Page
CRT Controller for low cost terminals	EF9345	- Single chip semi-graphic display processor for Color CRT Controller low cost terminals - TV Standard Compatible 50/60 Hz - 2 screen formats: 25 (or 21) row 80 or 40 characters - On chip characters generator. - Single 5V supply.	DIL40 PLCC44	 	3-5
Enchancement of low cost and mid-range color graphics applications	EF9369	- Single chip color palette - 16 different colors, each selected out of 4096 preset values - Dot rate up to 30 Mdots/s - Single 5V supply	DIL28 PLCC28	 	3-51
Enchancement of color graphics applications	TS68494	- Single chip color palette - 256 different colors, selected out of 4096 values - Serial port controller - Single 5V supply	PLCC44		3-67



THOMSON COMPONENTS SEMICONDUCTEURS

EF9345

SINGLE CHIP SEMI-GRAPHIC DISPLAY PROCESSOR

The EF9345, new advanced color CRT controller, in conjunction with an additional standard memory package allows full implementation of the complete display control unit of a color or monochrome low-cost terminal, thus significantly reducing IC cost and PCB space.

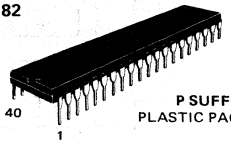
- Single chip low-cost color CRT controller
- TV standard compatible (50 Hz or 60 Hz)
- 2 screen formats :
  25 (or 21) rows of 40 characters
  25 (or 21) rows of 80 characters
- On-chip 128 alphanumeric and 128 semi-graphic character generator three standard options available for alphanumeric sets.
- Easy extension of user defined alphanumeric or semi-graphic sets (> 1 K characters).
- 40 characters/row attributes :
  Foreground and background color, double height, double width, blinking, reverse, underlining, conceal, insert, accentuation of lower case characters.
- 80 characters/row attributes :
  Underlining, blinking, reverse, color select.
- Programmable roll-up, roll down, and cursor display
- On-chip R, G, B, I video shift registers
- Easy synchronization with external video source : on-chip phase comparator.
- Address/data multiplexed bus directly compatible with standard microcomputers such as 6801, 6301, 8048, 8051.
- Addressing space : 16 K x 8 of general purpose private memory.
- Easy use of any low cost memory components : ROM, SRAM, DRAM
- Upward compatible with EF9340/41 chip set.

HMOS2

SINGLE CHIP SEMI-GRAPHIC DISPLAY PROCESSOR

CASES

CB-182

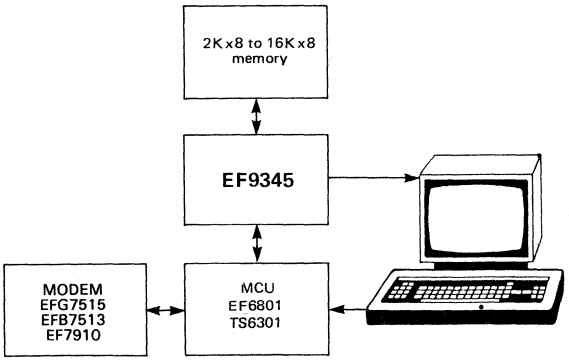


P SUFFIX
PLASTIC PACKAGE

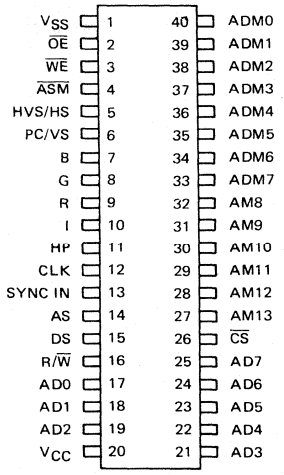
CB-521

FN SUFFIX
SURPICOP
(PLASTIC CHIP-CARRIER)

TYPICAL APPLICATION
Low cost personal terminal



PIN ASSIGNMENT



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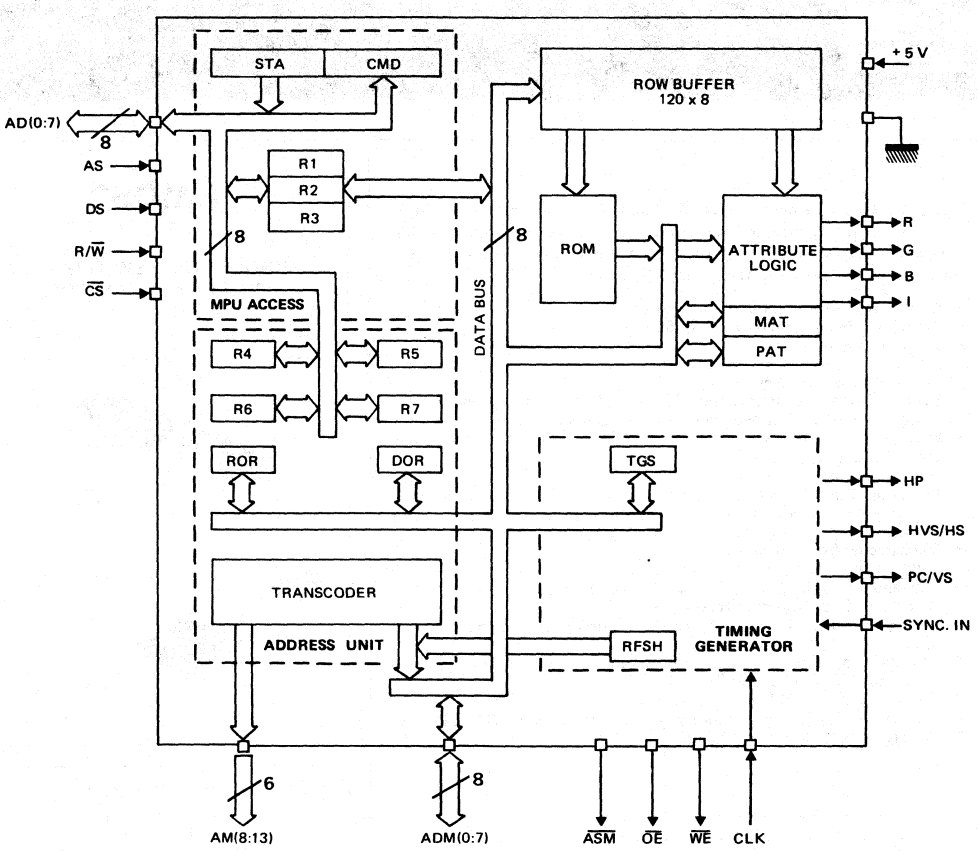
BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}*	- 0.3 to 7.0	V
Input voltage	V_{in}*	- 0.3 to 7.0	V
Operating temperature range	T_A	0 to 70	°C
Storage temperature range	T_{stg}	- 55 to 150	°C
Max power dissipation	P_{Dm}	0.75	W

*With respect to V_{SS}

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

ELECTRICAL OPERATING CHARACTERISTICS

(V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70°C))

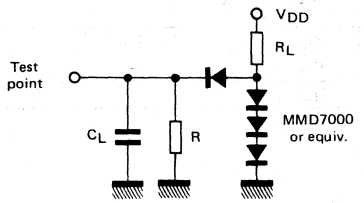
Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Input low voltage	V_{IL}	- 0.3	–	0.8	V
Input high voltage CLK other inputs	V_{IH}	2.2 2	— —	V_{CC} V_{CC}	V —
Input leakage current	I_{in}	–	–	10	µA
Output high voltage (I_{load} = - 500 µA)	V_{OH}	2.4	–	–	V
Output low voltage I_{load} = 4 mA ; AD(0:7), ADM(0:7), AM(8:13) I_{load} = 1 mA ; other outputs	V_{OL}	0.4	–	–	V
Power dissipation	P_D	–	250	–	mW
Input capacitance	C_{in}	–	–	15	pF
Three state (off state) input current	I_{TSI}	–	–	10	µA

MEMORY INTERFACE

V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C.
Clock : f_{in} = 12 MHz ; duty cycle 40 to 60 % ; t_r, t_f < 5 ns
Reference levels : V_{IL} = 0.8 V and V_{IH} = 2 V, V_{OL} = 0.4 V and V_{OH} = 2.4 V.

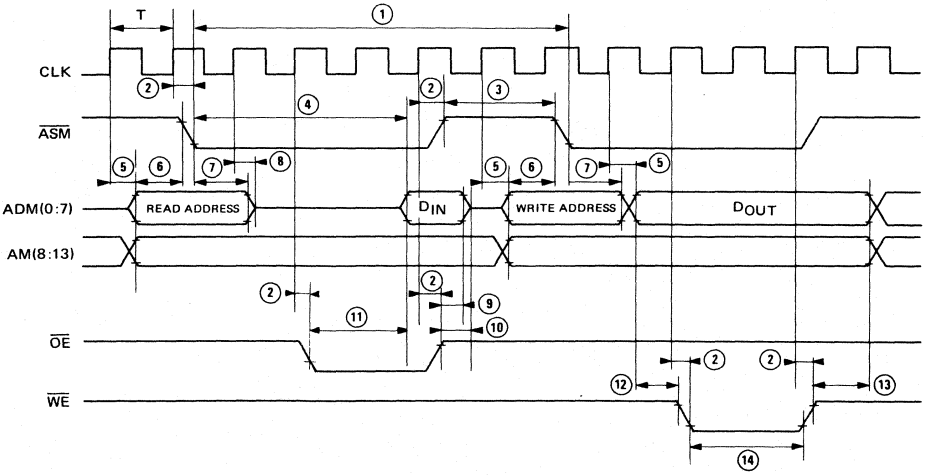
Ident. number	Characteristic	Symbol	Min	Typ	Max	Unit
1	Memory cycle time	t_{ELEL}	–	500	–	ns
2	Output delay time from CLK rising edge (ASM, OE, WE)	t_D	–	–	60	ns
3	ASM high pulse width	t_{EHEL}	120	–	–	ns
4	Memory access time from ASM low	t_{ELDV}	–	–	290	ns
5	Output delay time from CLK rising edge (ADM(0:7), AM(8:13))	t_{DA}	–	–	80	ns
6	Address setup time to ASM	t_{AVEL}	30	–	–	ns
7	Address hold time from ASM	t_{ELAX}	55	–	–	ns
8	Address off time	t_{CLAZ}	–	–	80	ns
9	Memory hold time	t_{GHDX}	10	–	–	ns
10	Data off time from OE	t_{OZ}	–	–	60	ns
11	Memory OE access time	t_{GLDV}	–	–	150	ns
12	Data setup time (write cycle)	t_{QVWL}	30	–	–	ns
13	Data hold time (write cycle)	t_{WHQX}	30	–	–	ns
14	WE pulse width	t_{WLWH}	110	–	–	ns

Test load



	ADM(0:7), AM(8:13) AD(0:7)	Other outputs
C	100 pF	50 pF
R_L	1 KΩ	3.3 KΩ
R	4.7 KΩ	4.7 KΩ

MEMORY INTERFACE TIMING DIAGRAM



MICROPROCESSOR INTERFACE

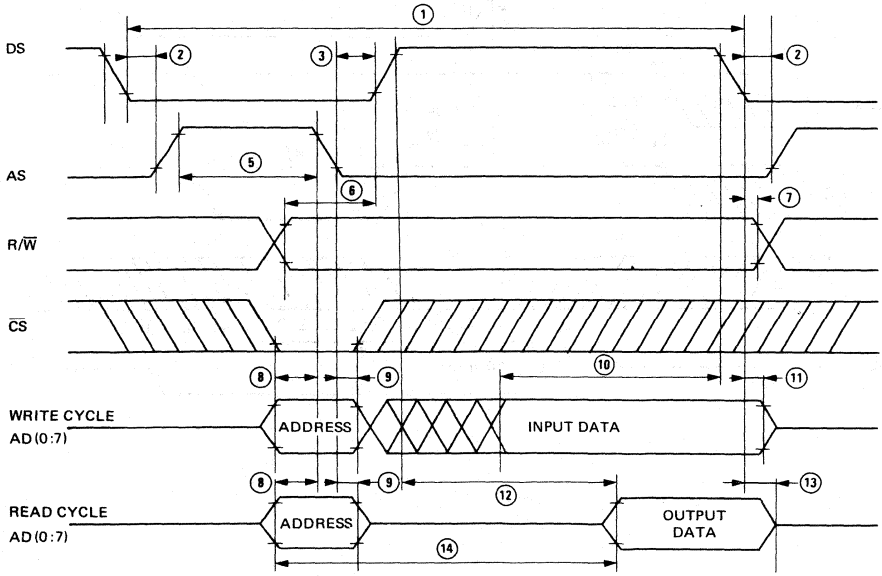
EF9345 is MOTEL compatible. It automatically selects the processor type by using AS input to latch to state of the DS input.
No external logic is needed to adapt bus control signals from most of the common multiplexed bus microprocessors.

EF9345	6801/6805CT	INTEL Family
	timing 1	timing 2
AS	AS	ALE
DS	DS, E, ϕ 2	$\overline{RD}$
R/$\overline{W}$	R/$\overline{W}$	$\overline{WR}$

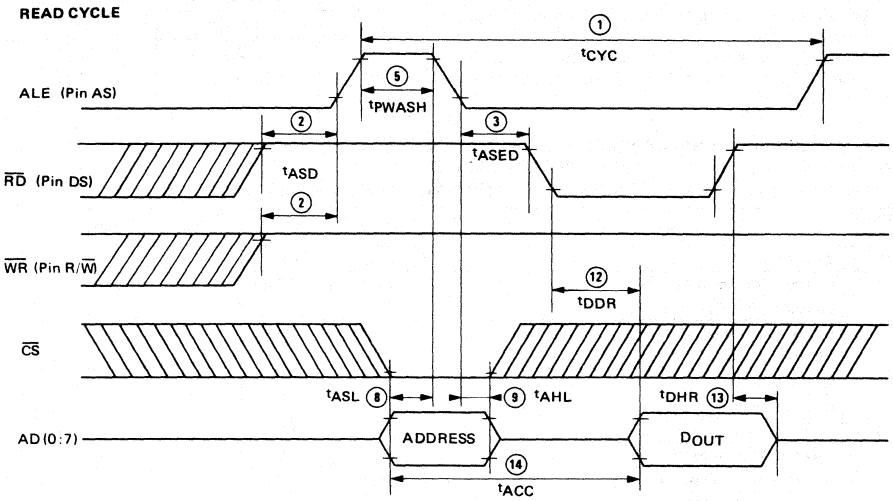
MICROPROCESSOR INTERFACE TIMING AD(0:7), AS, DS, R/$\overline{W}$, $\overline{CS}$
$V_{CC} = 5.0 \pm 5\ \%$, $T_A = 0°$ to $+70°C$, $C_L = 100$ pF on AD(0:7)
Reference levels : $V_{IL} = 0.8$ V and $V_{IH} = 2$ V on all inputs ; $V_{OL} = 0.4$ V and $V_{OH} = 2.4$ V on all outputs.

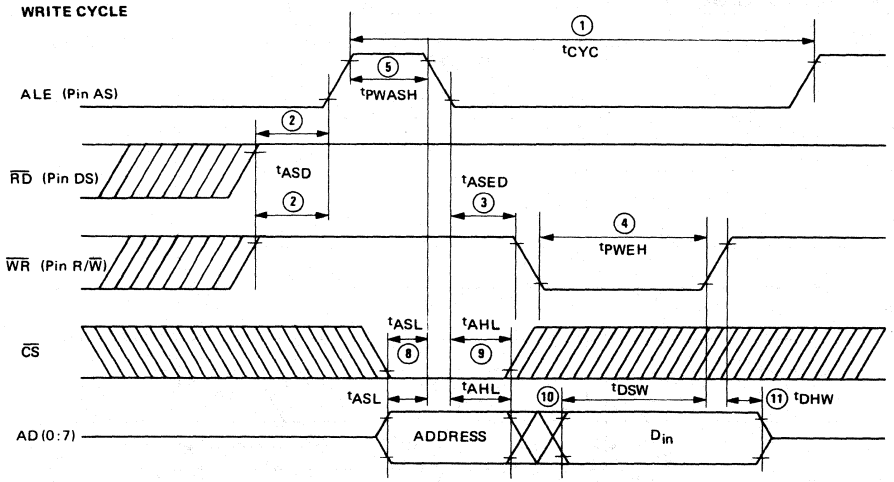
Ident. number	Characteristic	Symbol	Min	Typ	Max	Unit
1	Cycle time	t_{CYC}	400	–	–	ns
2	DS low to AS high (timing 1) DS high or R/$\overline{W}$ high to AS high (timing 2)	t_{ASD}	30	–	–	ns
3	AS low to DS high (timing 1) AS low to DS low or R/$\overline{W}$ low (timing 2)	t_{ASED}	30	–	–	ns
4	Write pulse width	t_{PWEH}	200	–	–	ns
5	AS pulse width	t_{PWASH}	100	–	–	ns
6	R/$\overline{W}$ to DS setup time (timing 1)	t_{RWS}	100	–	–	ns
7	R/$\overline{W}$ to DS hold time (timing 1)	t_{RWH}	10	–	–	ns
8	Address and $\overline{CS}$ setup time	t_{ASL}	20	–	–	ns
9	Address and $\overline{CS}$ hold time	t_{AHL}	20	–	–	ns
10	Data setup time (write cycle)	t_{DSW}	100	–	–	ns
11	Data hold time (write cycle)	t_{DHW}	10	–	–	ns
12	Data access time from DS (read cycle)	t_{DDR}	–	–	150	ns
13	DS inactive to high impedance state time (read cycle)	t_{DHR}	10	–	80	ns
14	Address to data valid access time	t_{ACC}	–	–	300	ns

MICROPROCESSOR INTERFACE TIMING DIAGRAM 1
(6801 / 6805CT)



MICROPROCESSOR INTERFACE TIMING DIAGRAM 2 (INTEL type)



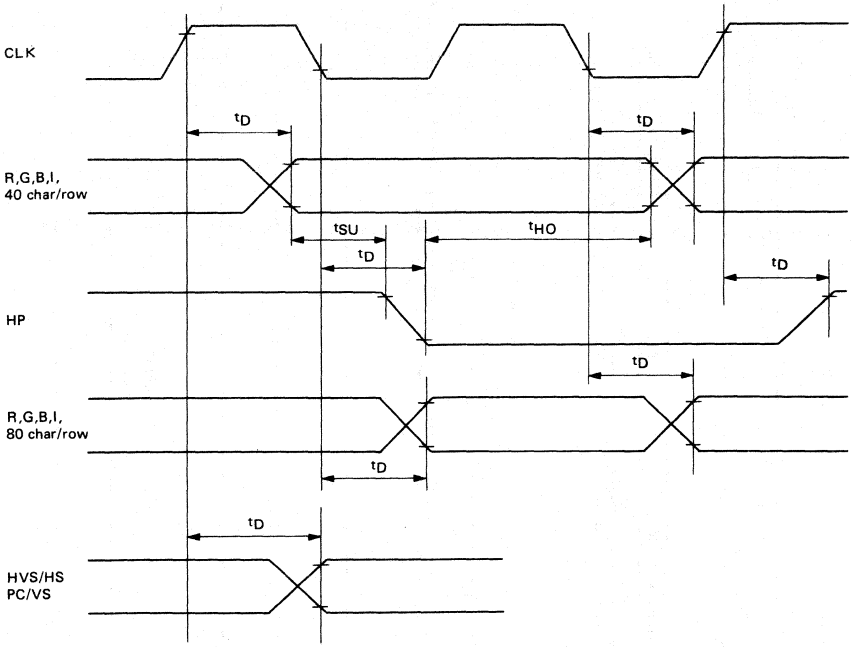


VIDEO INTERFACE R, G, B, I, HP, HVS / HS, PC / VS

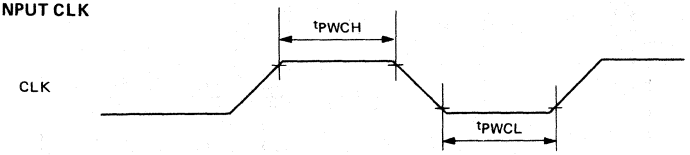
V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C, CLK duty cycle = 50 %, C_L = 50 pF

Reference levels : V_{IL} = 0.8 V and V_{IH} = 2.2 V on CLK input. V_{OL} = 0.4 V and V_{OH} = 2.4 V on all outputs.

Characteristic	Symbol	Min	Typ	Max	Unit
Set up time R, G, B, I to HP	t_{SU}	10	–	–	ns
Hold time R, G, B, I from HP	t_{HO}	50	–	–	ns
Output delay from CLK edge	t_D	–	–	60	ns



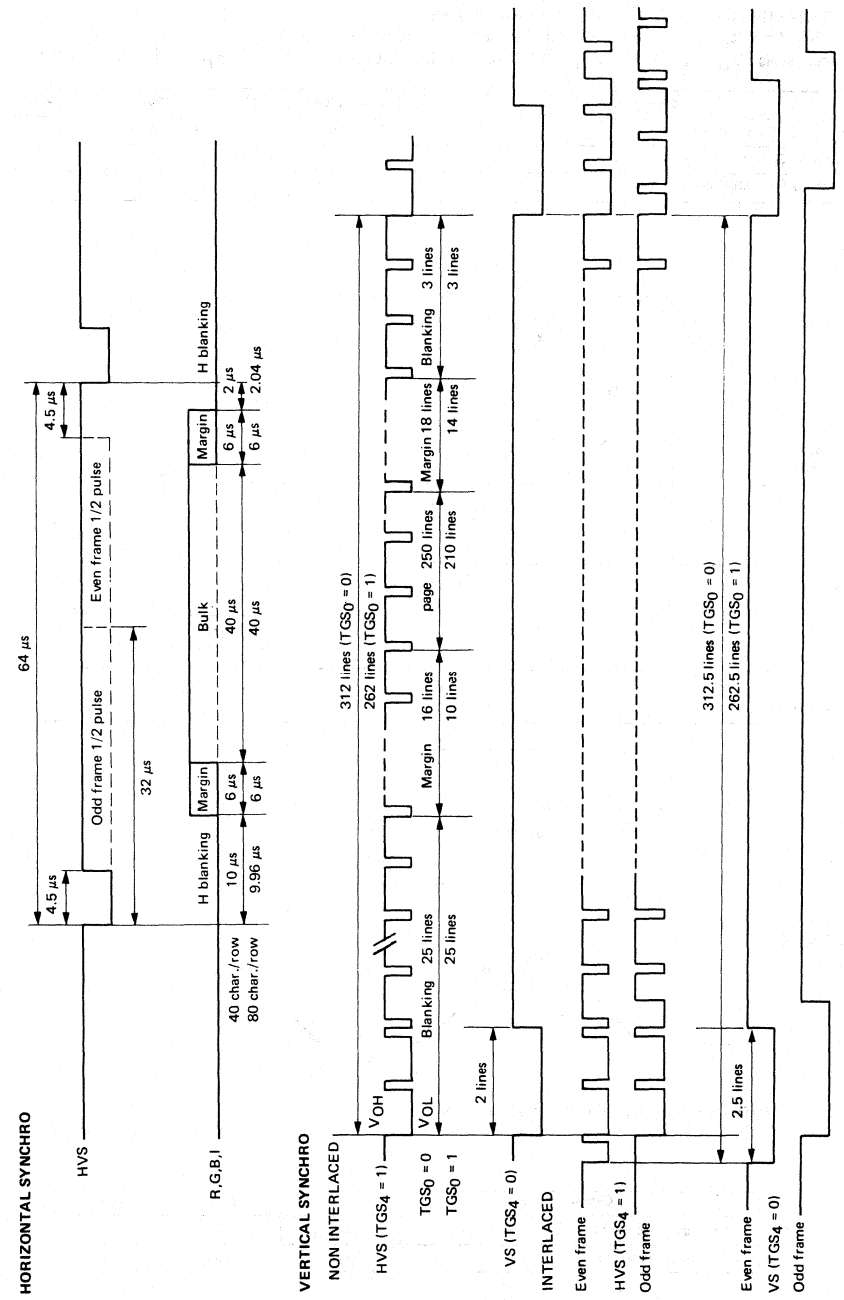
INPUT CLK



Reference level V_{IL} = 0.8 V, V_{IH} = 2.0 V

Characteristic	Symbol	Min	Unit
CLK high pulse width	t_{PWCH}	30	ns
CLK low pulse width	t_{PWCL}	30	ns

VERTICAL AND HORIZONTAL SYNCHRONIZATION OUTPUTS (CLK = 12 MHz)



EF9345 PIN DESCRIPTION

All the input/output pins are TTL compatible.

MICROPROCESSOR INTERFACE

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
AD(0:7)	I/O	17-19 21-25	Multiplexed Address/Data bus	These 8 bidirectional pins provide communication with the microprocessor system bus.
AS	I	14	Address Strobe	The falling edge of this control signal latches the address on the AD(0:7) lines, the state of the Data Strobe (DS) and Chip Select ($\overline{CS}$) into the chip.
DS	I	15	Data Strobe	When this input is strobed high by AS, the output buffers are selected while DS is low for a read cycle ($R/\overline{W} = 1$). In write cycle, data present on AD(0:7) lines are strobed by $R/\overline{W}$ low (See Timing Diagram 2). When this input is strobed low by AS, $R/\overline{W}$ gives the direction of data transfer on AD(0:7) bus. DS high strobes the data to be written during a write cycle ($R/\overline{W} = 0$) or enables the output buffers during a read cycle ($R/\overline{W} = 1$). (See Timing Diagram 1).
$R/\overline{W}$	I	16	Read / Write	This input determines whether the internal registers get written or read. A write is active low ("0").
$\overline{CS}$	I	26	Chip Select	The EF9345 is selected when this input is strobed low by AS.

MEMORY INTERFACE

ADM(0:7)	I/O	40-33	Multiplexed Address/Data bus	Lower 8 bits of memory address appear on the bus when $\overline{ASM}$ is high. It then becomes the data bus when $\overline{ASM}$ is low.
AM(8:13)	O	32-27	Memory Address bus	These 6 pins provide the high order bits of the memory address.
$\overline{OE}$	O	2	Output Enable	When low, this output selects the memory data output buffers.
$\overline{WE}$	O	3	Write Enable	This output determines whether the memory gets read or written. A write is active low ("0").
$\overline{ASM}$	O	4	Memory Address Strobe	This signal cycles continuously. Address can be latched on its falling edge.

VIDEO INTERFACE

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
R G B	O O O	7 8 9	Red Green Blue	These outputs deliver the video signal. They are low during the vertical and horizontal blanking intervals.
I	O	10	Insert	This active high output allows to insert R:G:B in an external video signal for captioning purposes, for example. It can also be used as a general purpose attribute or color.
HVS/HS	O	5	Sync. Out	This output delivers either the composite synchro (bit $TGS_4 = 1$) or the horizontal synchro signal (bit $TGS_4 = 0$).
PC/VS	O	6	Phase Comparator/ Vertical Sync	When $TGS_4 = 1$, this signal is the phase comparator output. When $TGS_4 = 0$, this output delivers the vertical synchro signal.
SYNC IN	I	13	Synchro In	This input allows vertical and/or horizontal synchronizing the EF9345 on an external signal. It must be grounded if not used.
HP	O	11	Video Clock	This output delivers a 4 MHz clock phased with the R, G, B, I signals.

OTHER PINS

CLK	I	12	Clock Input	External TTL clock input. (Nominal value : 12 MHz, duty cycle : 50 %).
V_{SS}	S	1	Power Supply	Ground.
V_{CC}	S	20	Power Supply	+ 5 V.

GENERAL OPERATION

The EF9345 is a low cost, semigraphic, CRT controller.

It is optimized for use with a low cost, monochrome or color TV type CRT (64 µs per line, 50 or 60 Hz refresh frequency).

The EF9345 displays up to 25 rows of 40 characters or 25 rows of 80 characters.

The on-chip character generator provides a 128 standard, 5 x 7, character set and standard semigraphic sets.

More user definable (8 x 10) alphanumeric or semigraphic sets may be mapped in the 16K x 8 private memory addressing space.

These user definable sets are available only in 40 characters per row format.

MICROPROCESSOR INTERFACE

The EF9345 provides an 8-bit, address/data multiplexed, microprocessor interface.

It is directly compatible with popular (6801, 6805CT, 8048, 8051, 8035...) microprocessors.

REGISTERS

The microprocessor directly accesses 8 registers :

- R0 : Command/status register
- R1, R2, R3 : Data registers
- R4, R5 } : Each of these register pairs points into the R6, R7 } private memory.

Through these registers, the microprocessor indirectly accesses the private memory and 5 more registers :

- ROR, DOR : Base address of displayed page memory and of used external character generators.
- PAT, MAT, TGS : Used to select the page attributes and format, and to program the timing generator option.

PRIVATE MEMORY

The user may partition the 16K x 8 private memory addressing space between :

- pages of character codes (2K x 8 or 3K x 8),
- external character generators,
- general purpose user area.

Many types of memory components are suitable :

- ROM, DRAM or SRAM,
- 2K x 8, 8K x 8, 16K x 4 organizations,
- Modest 500 ns cycle time and 250 ns access time is required.

40 CHARACTERS PER ROW : CHARACTER CODE FORMATS AND ATTRIBUTES

Once the 40 characters per row format has been selected, one character code format out of three must be chosen :

- 24-bit fixed format :
  All the attributes are provided in parallel.
- 8/24-bit compressed format :
  All the attributes are latched.
- 16-bit fixed format :
  Some parallel attributes, others are latched.

The 16-bit fixed format is compatible with EF9340/41 CRT controller.

Character attributes provided :

- Background and foreground color (3 bits each),
- Double height, double width,
- Blinking,
- Reverse,
- Underlining,
- Conceal,
- Insert,
- Accentuation of lower case characters
- 3 x 100 user definable character generator in memory
- 8 x 100 semi-graphic quadrichrome characters.

80 CHARACTERS PER ROW FORMAT : CHARACTER CODE FORMAT AND ATTRIBUTES

Two character code formats are provided :

- Long (12 bits) with 4 parallel attributes :
  - Blinking,
  - Underlining,
  - Reverse,
  - Color select.
- Short (8 bits) : no attributes.

TIMING GENERATOR

The whole timing is derived from a 12 MHz main clock input.

The RGB outputs are shifted at 8 MHz for the 40 character/row format and at 12 MHz for the 80 character/row.

Besides, the user may select :

- 50 Hz or 60 Hz vertical sync. frequency,
- Interlaced or not,
- Separated or composite vertical and horizontal sync. outputs.

Furthermore, a composite sync. input allows, when it is required :

- An on-chip vertical resynchronization,
- An on-chip crude horizontal resynchronization,
- An off-chip high performance horizontal resynchronization by use of a simple external VCXO controlled by the on-chip phase comparator.

MEMORY ORGANIZATION

LOGICAL AND PHYSICAL ADDRESSING

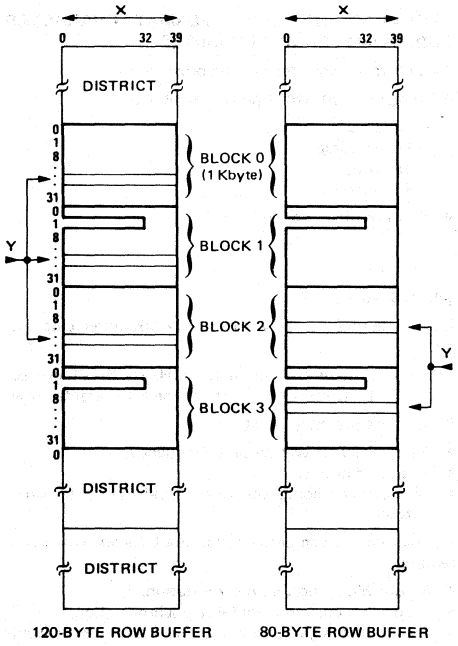
The physical 16-Kbyte addressing space is logically partitioned by EF9345 into 40-byte **buffers** (Figure 1). More precisely, a logical address is given by an X, Y, Z triplet where :

- X = (0 to 39) points to a byte inside a buffer,
- Y = (0,1 ; 8 to 31) points to a buffer inside a 1 Kbyte block,
- Z = (0 to 15) points to a **block.**

Obviously, 1 K = 2^{10} = 1024 cannot be exactly divided by 40. Consequently, any block holds 25 full buffers and a 24-byte remainder. Provided that the physical memory is a multiple of 2 Kbytes, the remainders are paired in such a way as to make available :

- a full buffer (Y = 1) in each even block,
- a partial buffer (Y = 1 ; X = 32 to 39) in each odd block.

FIGURE 1 – MEMORY ROW BUFFER



- Row buffers lay inside a district.
- At two or three successive block addresses (modulo 4).
- First block address is even.

POINTERS

Each X, Y and Z component of a logical address is binary encoded and packed in two 8-bit registers. Such a register pair is a pointer (Figure 2). EF9345 contains two pointers :

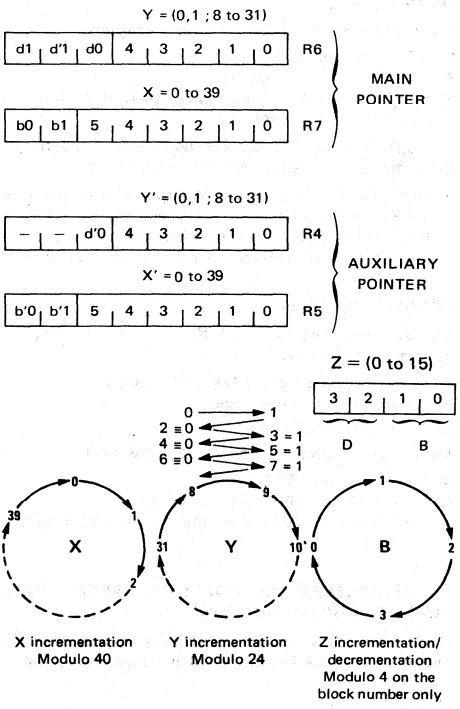
- R4, R5 : **auxiliary pointer,**
- R6, R7 : **main pointer.**

R5 and R7 have the same format. Each one holds an X component and the two LSB's of a Z component. This packing induces a partitioning of Z in 4 **districts** of 4 blocks each.

R5, R7 points to a block number in a district. R4 and R6 have a slightly different format : Each one holds a Y component and the LSB of the district number. But R6 holds both district MSB.

Figure 3 gives the logical to physical address transcoding scheme performed on chip.

FIGURE 2 – POINTER AUTO INCREMENTATION



DATA STRUCTURES IN MEMORY

A **page** is a data structure displayable on the screen up to 25 rows of characters. According to the character code format, each row on the screen is associated with 2 (or 3) 40-byte buffers. This set of 2 (or 3) buffers constitutes a row buffer (Figure 1). The buffers belonging to a **row buffer** must meet the following requirements :

- they have the same Y address,
- they have the same district number,
- they lie at 2 (or 3) successive (modulo 4) block addresses in their common district.

Consequently, a row buffer is defined by its first buffer address and its format.
A page is a set of successive row buffers :

- with the same format,
- with the same district number,
- with the same block address of first buffer. This block address must be even.
- lying at successive (modulo 24) Y addresses.

Consequently, a page should not cross a district boundary. General purpose memory area may be used but should respect the buffer or row buffer structure. See Figure 2 for pointer incrementation implied by these data structures.

MEMORY TIME SHARING (See Figure 4)

The memory interface provides a 500 ns cycle time. That is to say a 2 Mbyte/s memory bandwidth. This bandwidth is shared between :

- reading a row buffer from memory to load the internal row buffer (up to 120 bytes once each row),
- reading user defined characters slices from memory (1 byte each μs),
- indirect microprocessor read or write operation,
- refresh cycles to allow DRAM use, with no overhead.

A fixed allocation scheme implements the sharing.

Notes on Figure 4.

1. Dummy cycles are read cycles at dummy addresses.
2. RFSH cycles are read cycles performed by an 8-bit auto-incrementing counter. Low order address byte ADM(0:7) cycles through its 256 states in less than 1 ms.
3. The microprocessor may indirectly access the memory once every μs, except during the first and the last line of a row, when the internal buffer must be reloaded.

During these lines, no microprocessor access is provided for 104 μs ; this hold too when no user defined character slices are addressed.

FIGURE 4 - MEMORY CYCLE ALLOCATION

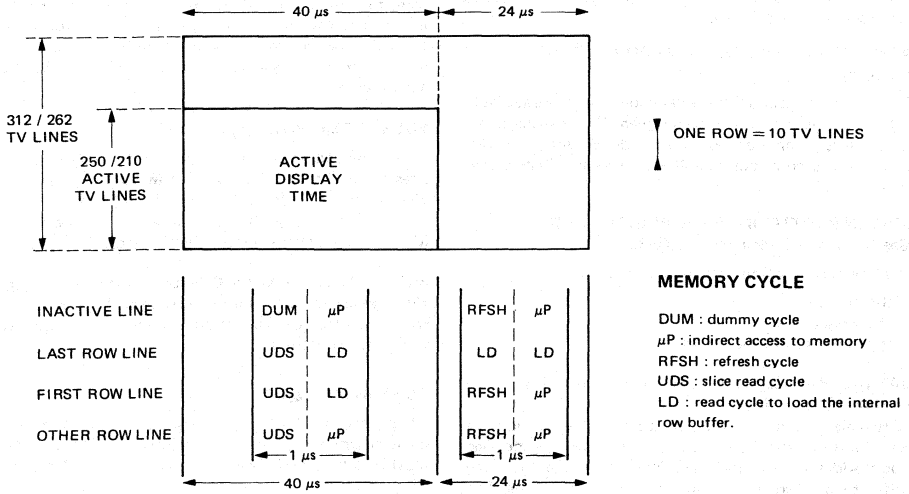
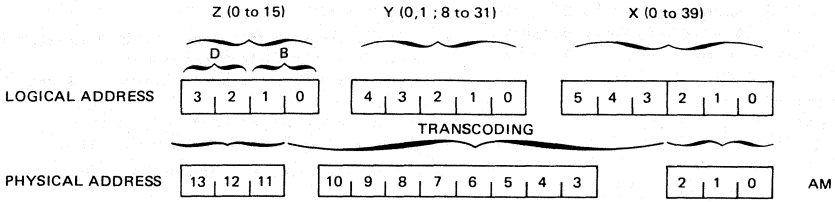


FIGURE 3 – LOGICAL TO PHYSICAL ADDRESS TRANSCODING PERFORMED ON-CHIP



X and Y CONDITION			PHYSICAL ADDRESS AM (3:10)							
			10	9	8	7	6	5	4	3
Y ⩾ 8	X5 = 0		b0	Y4	Y3	Y2	Y1	Y0	X4	X3
	X5 = 1		b0	0	0	Y2	Y1	Y0	Y4	Y3
Y < 8	Y0 = 0		b0	0	0	X5	X4	X3	0	0
	Y0 = 1	b0 = 0	X3	0	0	1	$\overline{X5}$	$\overline{X4}$	0	0
		b0 = 1	1	0	0	1	$\overline{X5}$	$\overline{X4}$	0	0

SCREEN FORMAT AND ATTRIBUTES

The screen format and attributes are programmed through 5 indirectly accessible registers : **ROR, TGS, PAT, MAT** and **DOR**. IND command allows accessing these registers. TGS is also used to select the timing generator options (see Screen Format Table).

ROW AND CHARACTER CODE FORMAT PAT_7 ; $TGS_{(6:7)}$

Two row formats and 5 character code formats are available but cannot be mixed in a given screen. DOR register interpretation is completely row format dependant and is discussed in the corresponding 40 char/row and 80 char/row section.

SCREEN PARTITION - PAGE POINTER ROR (See top of the Screen Format Table)

The screen is partitionned into 3 areas :

- the margin,
- the service row,
- the bulk of remaining rows.

$MAT_{(0:3)}$ declares the color of the margin and the value i_M of its insert attribute.
ROR register points to the page to be displayed and gives the 3 MSB's of the Z address : $Z_0 = 0$ implicitly ; the page block address must be even. YOR gives the first row buffer to be displayed at the top of the bulk area. The next row buffers to be displayed are fetched sequentially by incrementing the Y address (modulo 24). This address never gets out of the origin block. Incrementation of YOR by the microprocessor yields a roll up.

SERVICE ROW : TGS_5 - PAT_0

The service row is displayed for 10 TV lines on top of the screen and does not roll. Following TGS_5, it is fetched from the origin block at either Y = 0 or Y = 1. The Y = 1 is a partial row buffer. It can be used only with variable 40 char./row and an 8 byte attribute file. The service row may be disabled by $PAT_0 = 0$; it is then displayed as a margin extension.

BULK : TGS_0 ; $PAT_{(1:2)}$; MAT_7

It is displayed after the service row for 200 or 240 TV lines according to TGS_0. Each row buffer is usually displayed for 10 TV lines. However, $MAT_7 = 1$ doubles this figure. Then every character appears in double height (double height characters are quadrupled).

$PAT_1 = 0$ and/or $PAT_2 = 0$ disables respectively the upper 120 lines and/or the lower 80/120 lines of the bulk.
When disabled, the corresponding TV lines are displayed as a margin extension.

CURSOR $MAT_{(4:6)}$

To be displayed with the cursor attributes, a character must be pointed by the main pointer (R6, R7) and MAT_6 must be set. The cursor attributes are given by $MAT_{(4:5)}$:

- **Complementation** :
  the R, G and B of each pixel is logically negated.
  R, G, B ⟶ $\overline{R}$, $\overline{G}$, $\overline{B}$

- **Underline :**
  the underline attribute of this character is negated.
- **Flash :**
  the character is periodically displayed with, then without, its cursor attributes (50 % / 50 % ; ≃ 1 Hz).

FLASH ENABLE (PAT_6) - CONCEAL ENABLE (PAT_3)

Any character flashing attribute is a "don't care" when $PAT_6 = 0$. When $PAT_6 = 1$, a character flashes if its flashing attribute is set. It is then periodically displayed as a space (50 % / 50 % ; ≃ 0.5 Hz).

PAT_3 is a "don't care" for 80 char./row formats. When any 40 char./row format is in use :

- if $PAT_3 = 0$, the conceal attribute of any character is a don't care,
- if $PAT_3 = 1$, the conceal attribute of each character is interpreted : a concealed character appears as a space on the screen.

INSERT MODES : PAT(4:5)

During **retrace, margin and extended margin periods,** the I output pin delivers the value of the insert margin attribute. $I = i_M = MAT_4$.

During **active line** period, the I output state is controlled by the Insert Mode and i, the insert attribute of each character. The I output pin may have several uses : (See figure below) :

- As a margin/active area signal in the active area mark mode.
- As a character per character marker signal in the **character mark** mode.
- As a video mixing signal in the two remaining modes, provided that EF9345 has been vertically and horizontally synchronized with an external video source : the I pin allows mixing RGB outputs (I=1) and the external video signal (I=0). This mixing can be achieve by switching or ORing. It may occur for the complete character window **(Boxing Mode)** or only for the foreground pixels **(Inlay Mode)**.

Video outputs during active periods

INSERT MODE	CHAR. LEVEL		OUTPUTS	
	i	PIXELS (1)	I	R,G,B (2)
ACTIVE AREA MARK	–	–	1	X
CHARACTER MARK	0	–	0	X
	1	–	1	X
BOXING	0	–	0	BLACK
	1	–	1	X
INLAY	0	–	0	BLACK
	1	BACKGND	0	BLACK
		FOREGND	1	X

NOTES :
(1) PIXEL TYPE
– : Don't care

FOREGND : A foreground pixel is :

- Any pixel of a quadrichrome character,
- A pixel of a bichrome character generated from a "1" in the character generator cell.

(2) RGB OUTPUTS

X : Not affected

BLACK : forced to low level.

TIMING GENERATOR OPTIONS : TGS(0:4)

$TGS_{(0:1)}$ select the number of lines per frame :

TGS_1	TGS_0	LINES	
0	0	312	NON INTERLACED
0	1	262	
1	0	312.5	INTERLACED
1	1	262.5	

The composite incoming SYNC IN signal is separated into 2 internal signals :

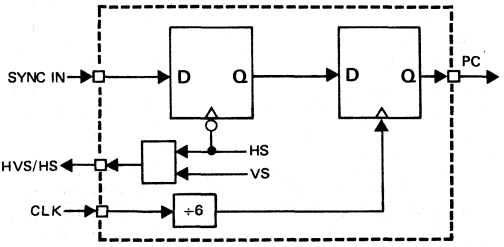
- Vertical Synchronization In (VSI),
- Horizontal Synchronization In (HSI).

TGS_3 enables VSI to reset the internal line count. SYNC IN input is sampled at the beginning of the active area of each line. When the sample transits from 1 to 0, the line count is reset at the end of the current line.

TGS_2 enables HSI to control an internal digital phase lock loop. HSI and on-chip generated HS Out are considered as in phase if their leading edges match at ± 1 clock period. When they are out of phase, the line period is lengthened by 1 clock period (≃ 80 ns).

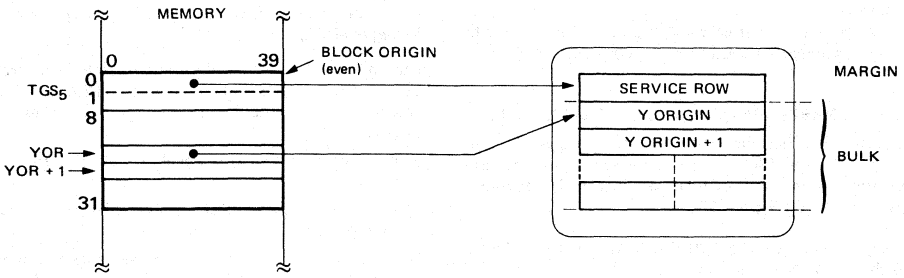
TGS_4 controls the SYNC OUT pins configuration :

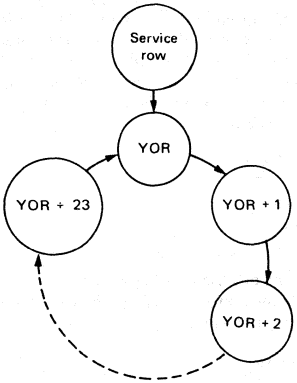
TGS_4	HVS / HS	PC / VS
1	COMPOSITE SYNC	PC
0	H SYNC OUT	V SYNC OUT

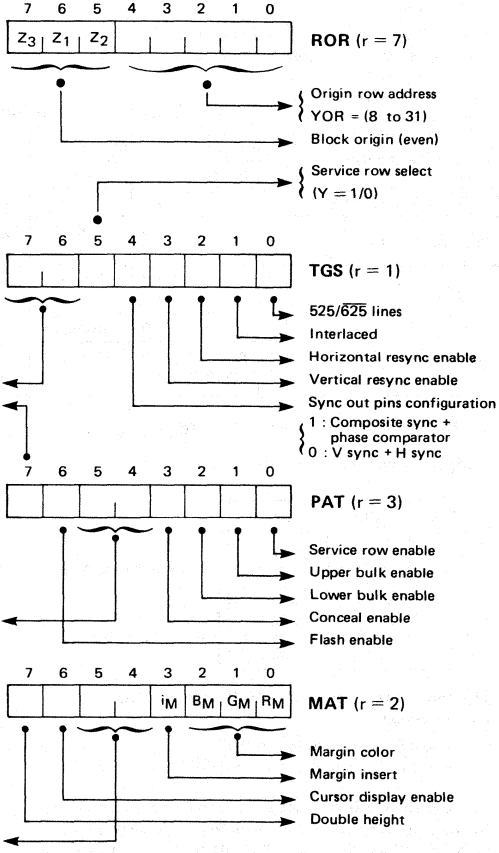


PC is the output of the on-chip phase comparator.
An external VCXO allows a smoother horizontal phase lock than the internal scheme.

SCREEN FORMAT TABLE







CHAR CODE	PAT_7	TGS_7	TGS_6
40 CHAR LONG	0	0	0
40 CHAR VAR	0	0	1
40 CHAR SHORT	1	0	0
80 CHAR LONG	0	1	1
80 CHAR SHORT	0	1	0

INSERT MODE	PAT_5	PAT_4
INLAY	0	0
BOXING	0	1
CHARACTER MARK	1	0
ACTIVE AREA MARK	1	1

CURSOR DISPLAY MODE	MAT_5	MAT_4
FIXED COMPLEMENTED	0	0
FLASH COMPLEMENTED	1	0
FIXED UNDERLINED	0	1
FLASH UNDERLINED	1	1

NOTE : PROGRAMMING BIT VALUE
1 = True
0 = False

40 CHAR/ROW CHARACTER CODES

To display pages in 40 character per row format, one out of three character code formats must be selected :

- Fixed long (24 bits) code : all parallel attributes.
- Fixed short (16 bits) code : mix of parallel and latched attributes.
- Variable (8/24 bits) code : all latched attributes.

Fixed short and variable codes are translated into fixed long codes by EF9345 during the internal row buffer loading process. The choice of the character code format is obviously a display flexibility/memory size trade off, left up to the user.

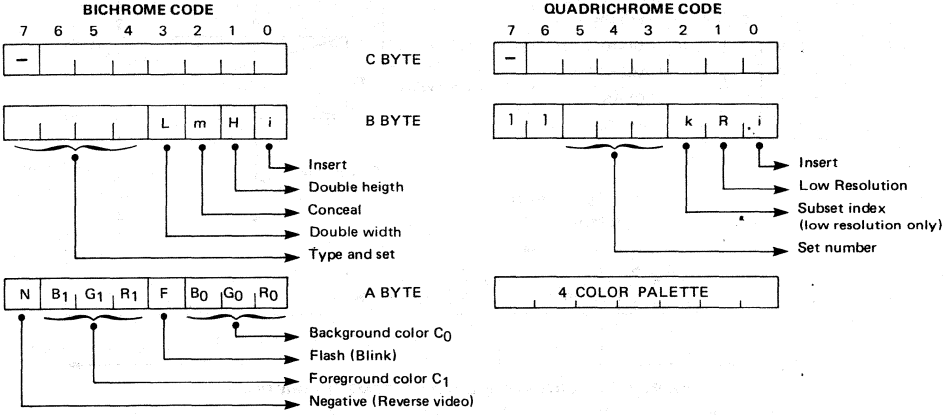
FIXED LONG CODES

This is the basic 40 char./row code. Each 8 pixels x 10 lines character window on the screen is associated with a 3-byte code in memory, namely the C, B and A bytes (Figure 5). A row on the screen is associated with a 120 byte row buffer in memory.

3-byte code structure

1. C7 is a don't care. Up to 128 characters may be addressed in each set. Each user definable set holds only 100 characters : C byte value ranges from 00 to 03 and 20 to 7F (hexa).
2. B(4:7) give the type and set number of the character.
3. All the bichrome characters have the same attributes except that alphanumerics may be underlined, semi-graphics cannot. Accentuated alphanumerics allow orthogonal accentuating of any one of the 32 lower case ROM characters with any of 8 accents (see Figure 19).

FIGURE 5 – 40 CHAR/ROW FIXED LONG CODES



TYPE AND SET CODE : B(4:7)				NUMBER OF CHARACTER PER SET	SET NAME	SET TYPE		CELL LOCATION
7	6	5	4	C(0:6)				
0	0	1	0	128 standard mosaïcs	G_{10}	SEMI-GR.	BICHROME	ON-CHIP ROM
		1	1	32 strokes	G_{11}			
	0	0	UNDERLINE	128 alphanumerics	G_0	ALPHA		
	1	0		Accentuated lower case alpha	G_{20}			
		1			G_{21}			
1	0	0		100 alpha UDS	G'_0			EXTERNAL MEMORY
	0	1	0	100 semi-graphic UDS	G'_{10}	SEMI-GR.		
		1	1	100 semi-graphic UDS	G'_{11}			
	1	X	X	8 sets of 100 quadrichrome character	Q_0 to Q_7	QUADRICHROME		

NOTA : Programming bit value
1 = True
0 = False

4. Bichrome and quadrichrome characters use two different coloring schemes.

For bichrome characters, character code byte A defines a two color set by giving directly two color values (Figure 6). The negative attribute exchanges the two values. Each bit of the slice byte selects one color value out of two.

The "A" byte in a quadrichrome character code defines an ordered 4 color set (Figure 7). When more than 4 bits are set, higher ranking bits are ignored. When less than 4 bits are set, the color set is completed with implicit "white" value. The slice byte is shifted 2 bits at once at half the dot frequency (≃ 4 MHz). Each bit pair designates one color out of the 4 color sets.

Quadrichrome characters allow displaying up to 4 different colors (instead of 2) in any 8 x 10 window at the penalty of an halved horizontal resolution.
By programming the R attribute in byte B, one may chose to keep the full vertical resolution (1 slice per line) or to halve it (each slice is repeated twice). In any case, it is possible to change the color set freely from window to window and to mix freely all the character types. So, fairly complex pictures may be displayed at low memory cost.

FIGURE 6 – COLORING WITH BICHROME CHARACTERS

B	G	R	COLOR VALUE
0	0	0	BLACK
0	0	1	RED
0	1	0	GREEN
0	1	1	YELLOW
1	0	0	BLUE
1	0	1	MAGENTA
1	1	0	CYAN
1	1	1	WHITE

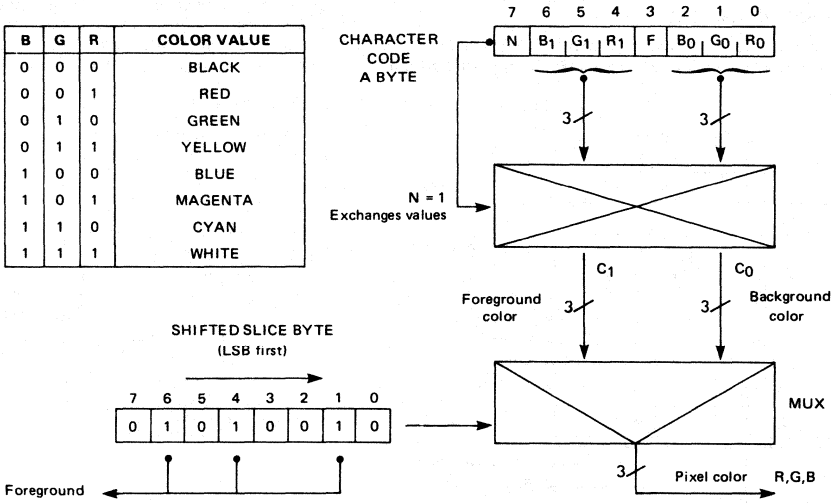
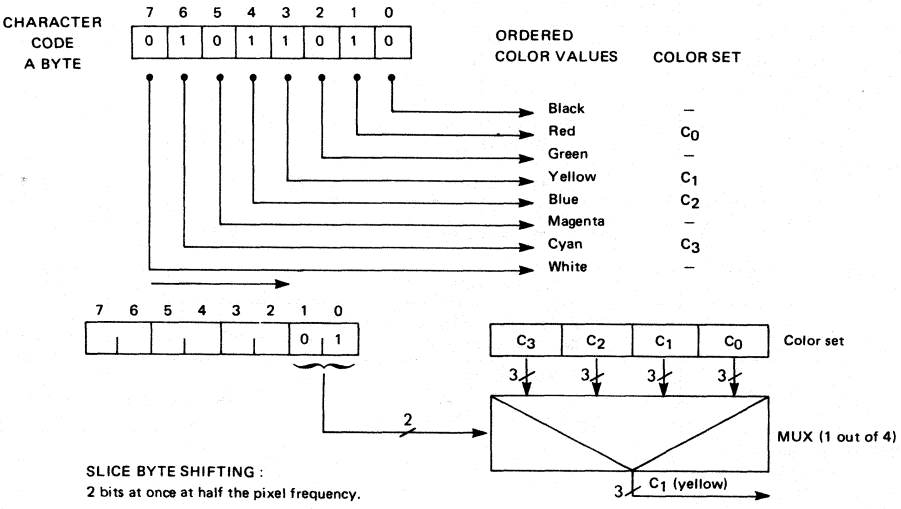


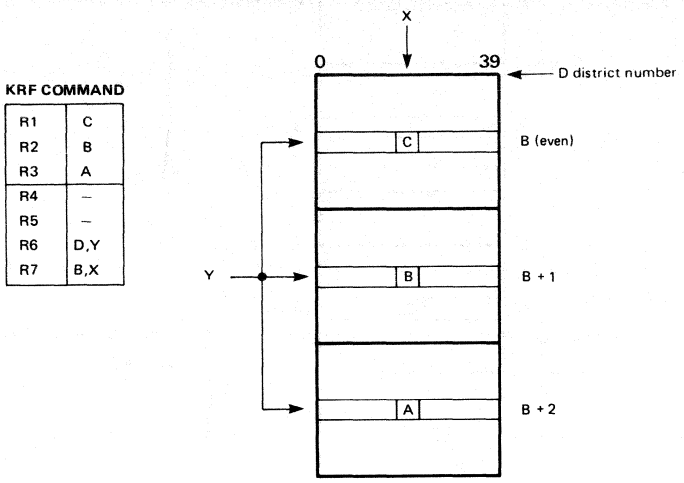
FIGURE 7 – COLORING WITH QUADRICHROME CHARACTERS



Handling long codes

The KRF command allows an easy X, Y random access or an X sequential access to/from the microprocessor from/to a memory row buffer (Figure 8).

FIGURE 8 – FIXED LONG CODES IN MEMORY 120 BYTE ROW BUFFER



VARIABLE CODES

In many cases, successive characters on screen belong to the same character set and have the same attributes. Variable codes achieve memory saving by storing B and A bytes only when it is required by exploiting the C7 bit.

C7 = 1 This is a long 3-byte code.
Character set and attribute values are completely redefined by B and A bytes.

C7 = 0 This is a short 1-byte code.
Character set and attributes value are identical to the previous code.

A further saving comes from the fact that an accentuated alphabetic character is, more often than not, followed by a not accentuated alphabetic character.
So, G_{20} or G_{21} sets are processed as one-shot escape with return to G_0. For normal operation, variable codes should obey the following rules :

- the first character code of any row (X = 0) should be long,
- a character code may be short when it has the same attributes as the previous character code and belongs to the same set.

However :

- any code belonging to G_{20} or G_{21} must be long and must be repeated if the character is double width,
- a code belonging to G_0 following a G_{20} or G_{21} code may be short.

Handling the variable codes

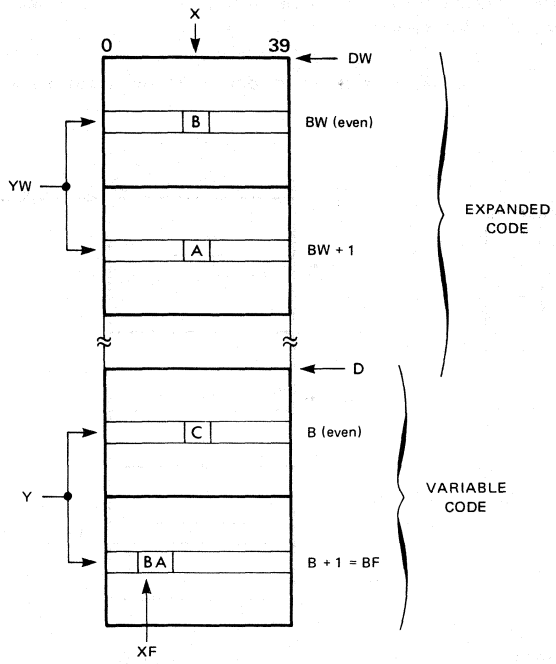
During the display process, a row of variable code should be laid in an 80/120 byte row buffer. The first buffer holds the C bytes. The second buffer holds the B, A file providing up to 20 long codes per row. (Figure 10). In the exceptionnal case when this is not enough, the second buffer overflows in the third one. Every code may then be long. Variable codes can almost always achieve a memory saving over long fixed codes and can never be worse.

The KRV command gives a very easy sequential access to/from a row buffer from/to the microprocessor. This command automatically updates the C byte and the B, A file pointers (the last one when C7 is set).

FIGURE 9 – EXPANSION/COMPRESSION MOVE

EXP and CMP commands

R1	–
R2	–
R3	–
R4	ZW, YW
R5	BF, XF
R6	D, Y
R7	B, X



Random access to a variable code is obviously not as easy. The EXP, KRE are CMP commands are designed to facilitate this task (Figure 9).

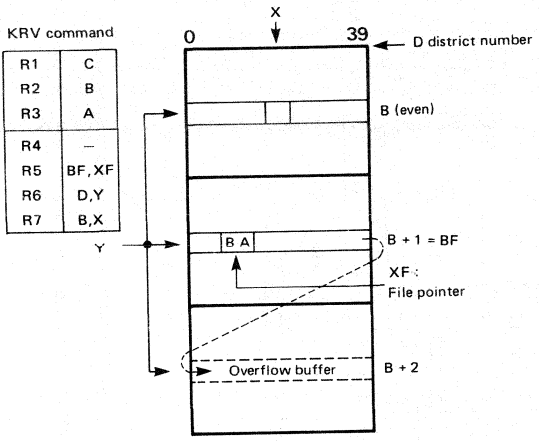
The EXP command translates a full row of variable codes into a row of expanded codes. Expanded codes are generally not displayable but very similar to the long codes.

KRE gives a random access to an expanded code and makes it appear as a regular long code.

The CMP command translates a full row of expanded code into a row of variable codes and minimizes the file size in the process.

These commands use a buffer pair as working area.

FIGURE 10 – VARIABLE CODES IN MEMORY



FIXED SHORT CODES

These fixed 16-bit codes are compatible with EF9340/41 display controllers. They achieve memory saving by another way. They may be easier to handle than variable codes. The penalty is in lesser display capabilities :

- accentuated character sets are no longer available : accentuated characters must be individually provided by the character generators,
- G'11 and quadrichrome sets cannot be reached,
- some attributes are latched and can be changed only while displaying a space (delimitor code).

The KRG command allows an easy access from/to an 80-byte row buffer in memory to/from the microprocessor (Figure 11). Figure 12 gives the fixed short to fixed long translation process which occurs for each row - while loading the internal row buffer - before display.

FIGURE 11 – FIXED SHORT CODES IN MEMORY 80 BYTE ROW BUFFER

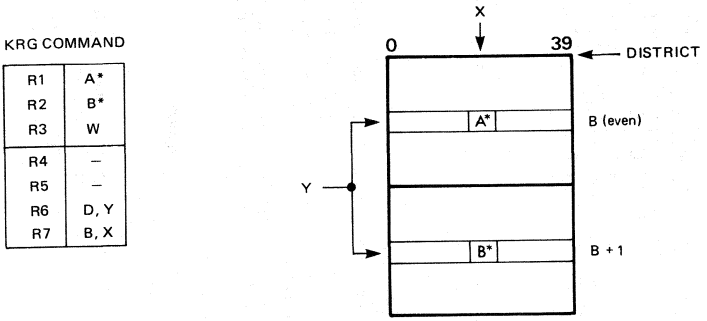
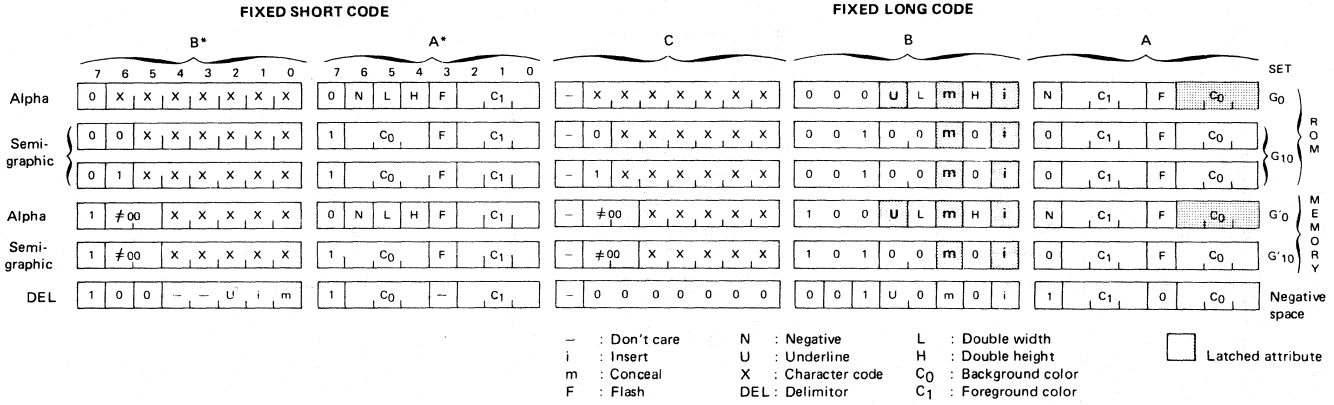


FIGURE 12 – FIXED SHORT CODE TO FIXED LONG CODE TRANSLATION



NOTES

1/ Translation process

The translation process operates through 3 elementary operations :

- Field-to-field : a character code or an attribute value (i.e : C_0, flashing) is directly loaded from short to long code.
- Field-to-constant the decoding of a short code forces the value of the equivalent long code attribute. For example, semigraphic short characters forces normal size (H = 0, L = 0) attributes.
- Latched attributes . at the beginning of each row, these attributes are reset (no underline, not concealed, no insert, black background). Then, they keep their current value until modified by either a field to field or field to constant operation.

2/ EF9340/41 compatibility

It is binary code compatible with few exceptions :

- flashing attribute is negated,
- A7 is negated in delimitors.

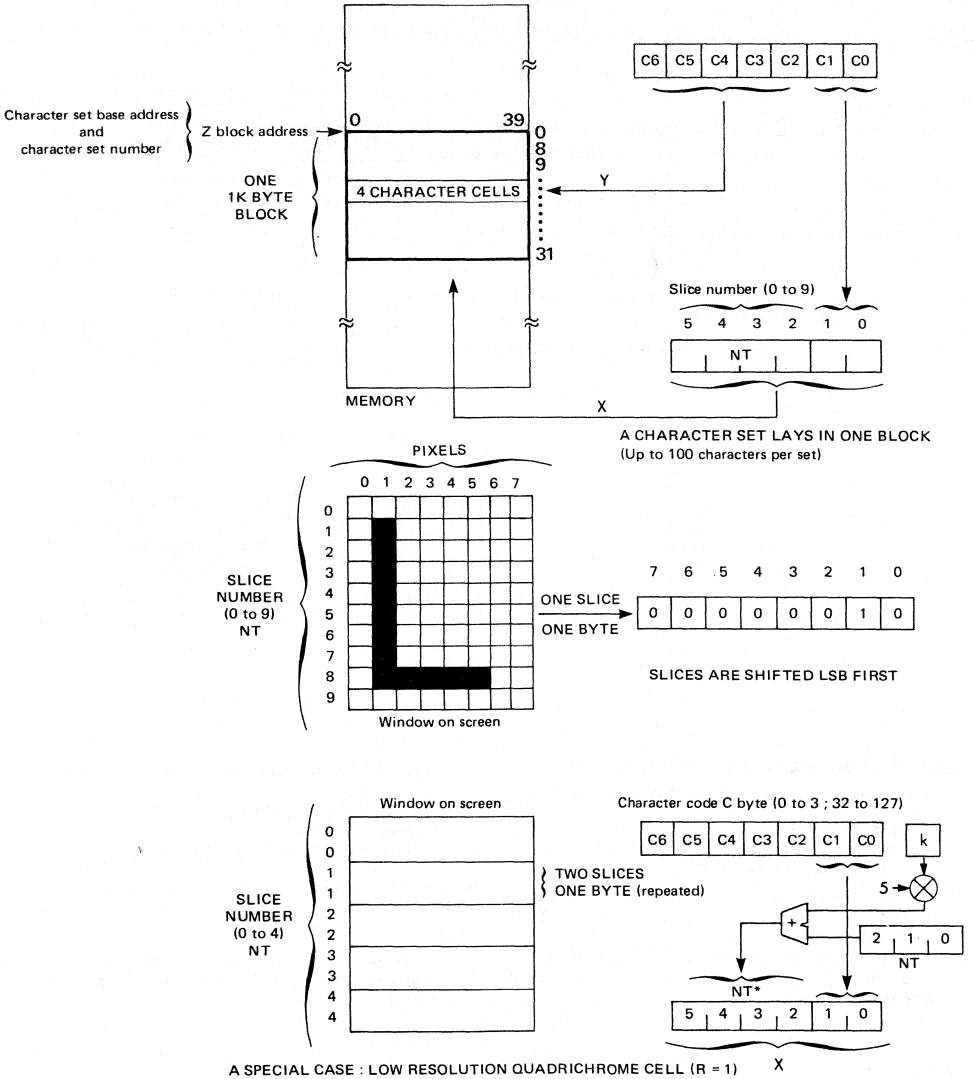
It is also display compatible with 2 exceptions concerning the underlining :

- an alphanumeric belonging to G'_0 may be underlined,
- any alphanumeric following a semigraphic cannot be underlined.

USER DEFINED CHARACTER GENERATOR IN MEMORY : DOR REGISTER

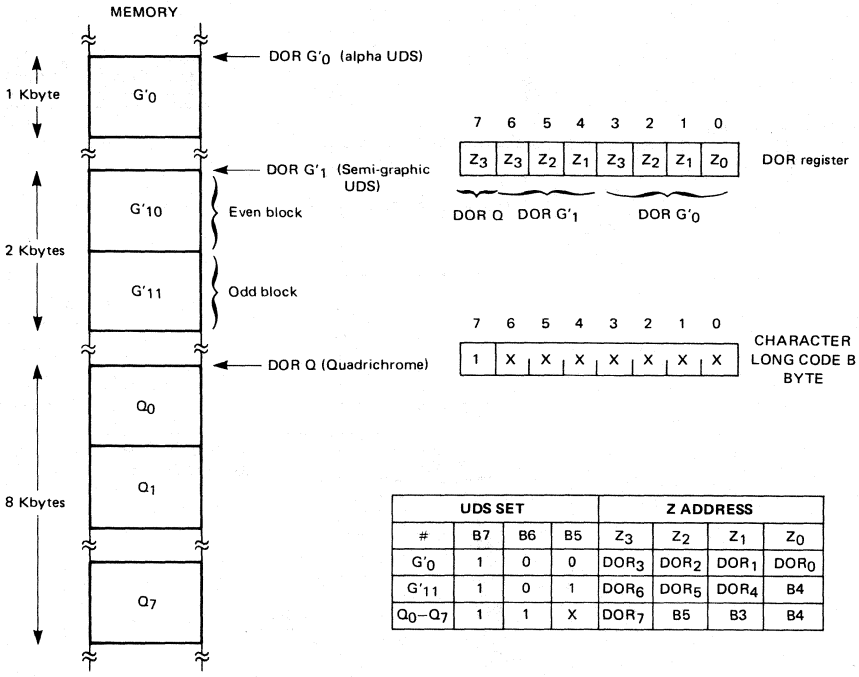
With 40 char./row, the elementary window dimensions on the screen are 10 slices x 8 pixels. Thus, a character cell holds 10 bytes in memory and 4 character cells are packed in one 40-byte buffer (Figure 13). However, 5 bytes of a low resolution quadrichrome cell are enough to fill up the window. In this case, 8 character cells can be packed in one 40-byte buffer.

FIGURE 13 – PACKING UDS CELLS IN MEMORY



The cells of one given character set should be layed in one block.
Up to 100 character cells may be addressed in each set (or 200 for low resolution quadrichrome only). The location in memory, where to fetch the sets in use, are declared by DOR register (Figure 14). For each type of set, it gives the MSB(s) of the Z block address. EF9345 reads the Z LSB(s) in the B byte of the (equivalent) long code. As usual, the character code is read in the C byte. NT is derived from the TV line rank in the row and the double height status.

FIGURE 14 – UDS FETCH TO DISPLAY



UDS SET				Z ADDRESS			
#	B7	B6	B5	Z_3	Z_2	Z_1	Z_0
G'0	1	0	0	DOR_3	DOR_2	DOR_1	DOR_0
G'11	1	0	1	DOR_6	DOR_5	DOR_4	B4
Q_0–Q_7	1	1	X	DOR_7	B5	B3	B4

LOADING USER DEFINED CHARACTER SET

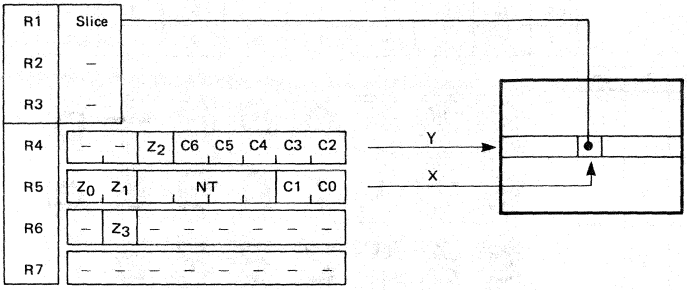
Before loading a character set into RAM, the user must :

- Assign a name to the set :
  - G'0, G'10 or G'11 for bichrome characters.
  - From Q0 to Q7 for quadrichrome characters.
- Assign a character number to each character belonging to this set . character numbers range from 0 to 3 and 32 to 127.
  It is binary coded into 7 bits C(0:6) – C(0:6) will be loaded later on into a C byte character code in order to display the character.
- A pointer to a character slice in memory is then manufactured from :
  - the character number C(0:6)
  - the slice number NT(0:3)
  - the block number assigned to the set Z(0:3).

Figure 15 shows how to proceed with the auxiliary pointer and the OCT command.

Note :
The main pointer may be also used. When sequentially accessing slices of a given character, auto incrementation is helpless.

FIGURE 15 – ACCESSING A CHARACTER SLICE IN MEMORY USING OCT COMMAND WITH AUXILIARY POINTER



ON-CHIP CHARACTER GENERATOR

- G_0 set is common to 40 and 80 char./row modes (Figure 16 and Figure 25).
- G_{10} is the standard mosaïc set for videotex (Figure 17).
- G_{11}, G_{20} and G_{21} cannot be reached from the 16-bit short fixed codes (Figure 18 and Figure 19).

DISPLAYING THE ATTRIBUTES

1. For normal operation, a double height and/or double width character must be repeated in memory in two successive Y and/or X positions. The user may otherwise freely mix any character size.
2. The attributes are logically processed in the following order :
   - Underline or underline cursor : foreground forced on the last slice (NT = 9).
   - Flash : background periodically forced on the whole window (≃ 0.5 Hz). The phase depends on the negative attribute.
   - Conceal : background forced permanently on the whole window. A concealed character neither blinks nor is underlined.
   - Negative : exchange the background and foreground color values when set.
   - Coloring.
   - Complemented cursor mode.
   - Insert : black color forced when required.
3. Basic pixel shift frequency : $f_{CLK} \times 2/3 = 8$ MHz.

FIGURE 16 — G_0 ALPHANUMERIC CHARACTER SET IN 40 CHARACTER/ROW MODE — EF9345

C6	0	0	0	0	1	1	1	1
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

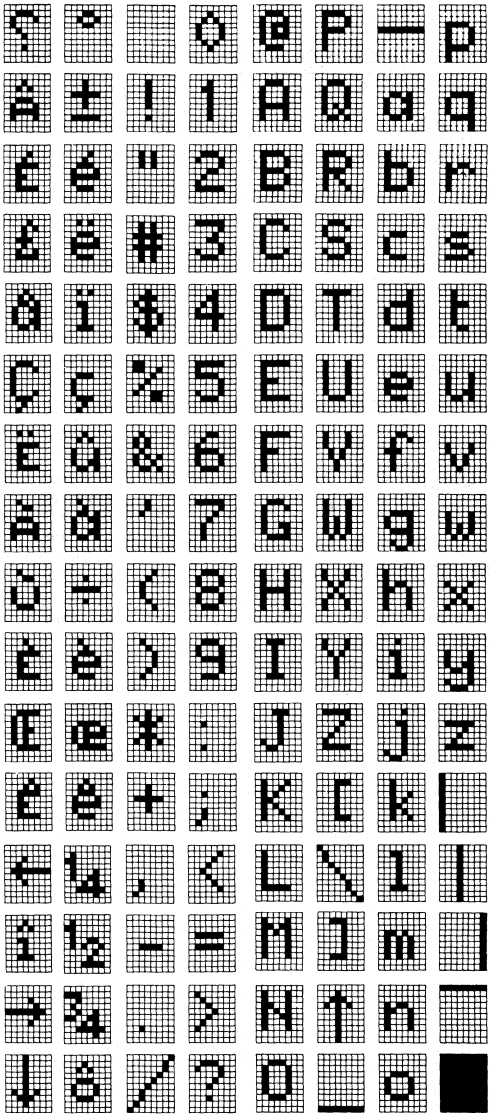


FIGURE 16 bis — G_0 ALPHANUMERIC CHARACTER SET IN 40 CHARACTER/ROW MODE — EF9345 R003

C6	0	0	0	0	1	1	1	1
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

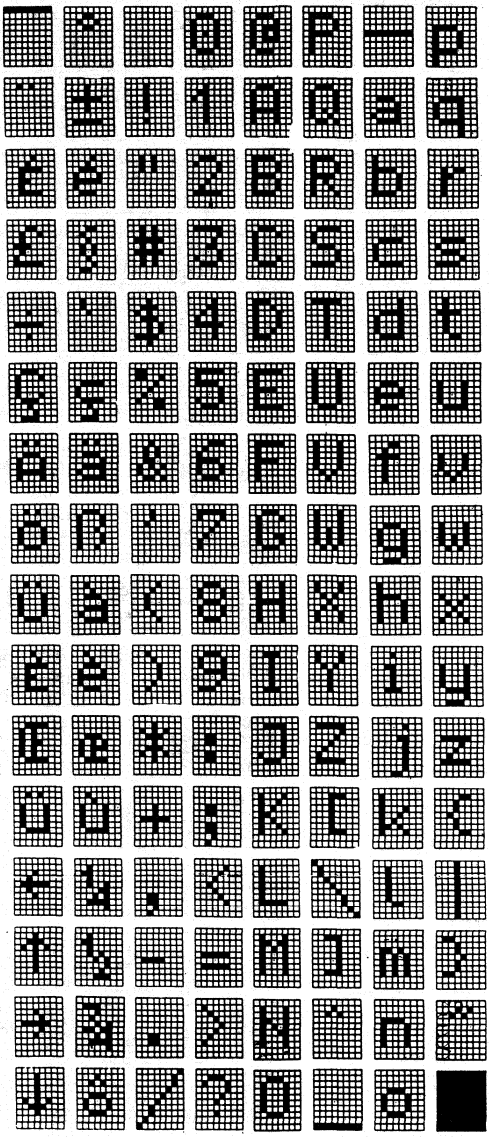


FIGURE 16 ter — G_0 ALPHANUMERIC CHARACTER SET IN 40 CHARACTER/ROW MODE — EF9345 R005

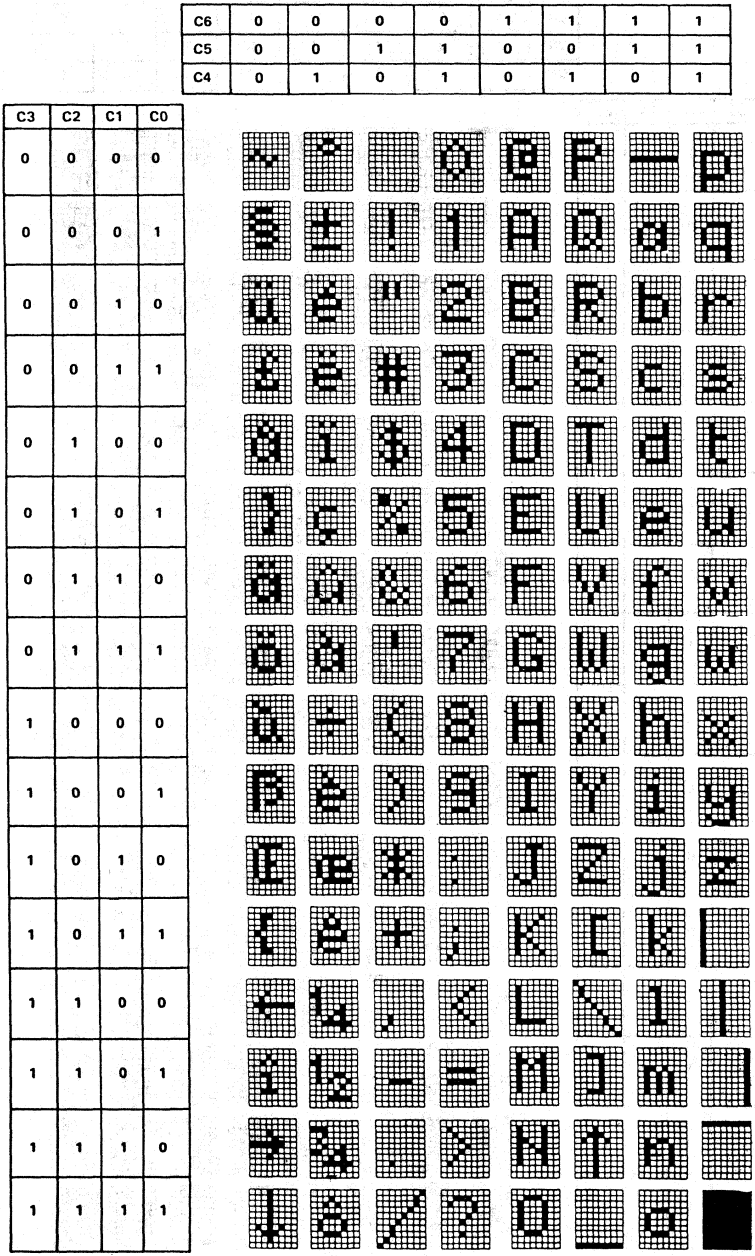


FIGURE 17 – G_{10} SEMIGRAPHIC CHARACTER SET

MOSAIC Semi-graphic SEPARATED Semi-graphic

C6	1	1	1	1	0	0	0	0
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

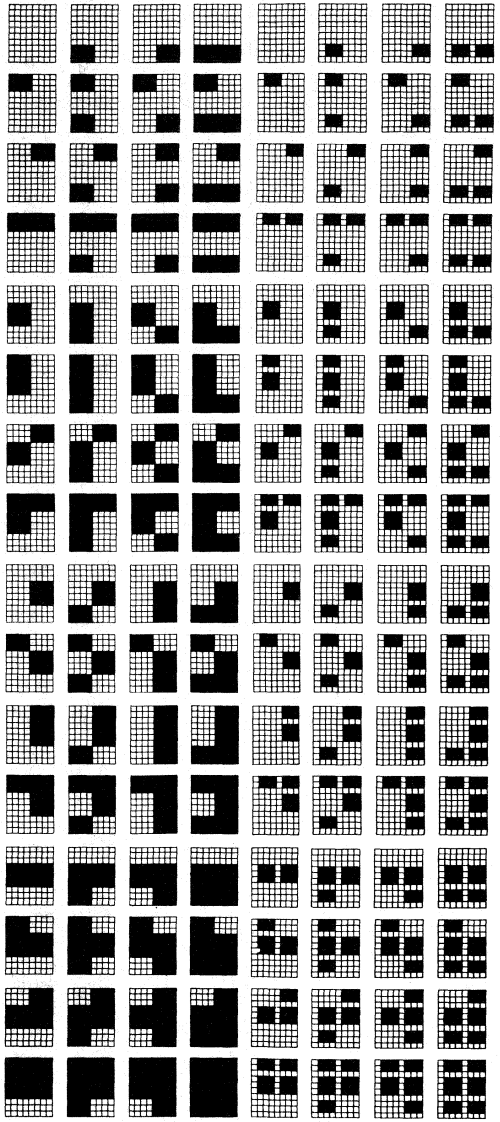
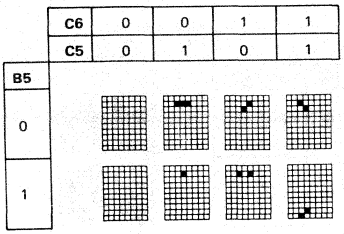


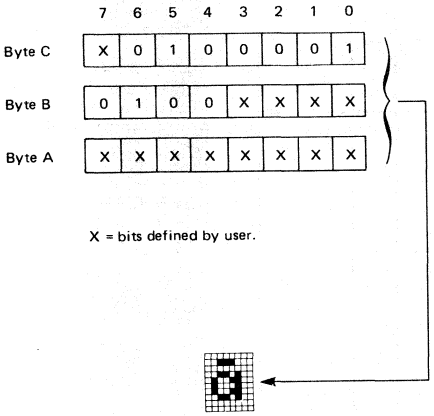
FIGURE 18 – G_{11} STROKE SET

				C5	0	0
				C4	0	1
C3	C2	C1	C0			
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

FIGURE 19 – G_{20} and G_{21} ACCENTUED CHARACTER SETS FOR 9345



Example :



X = bits defined by user.

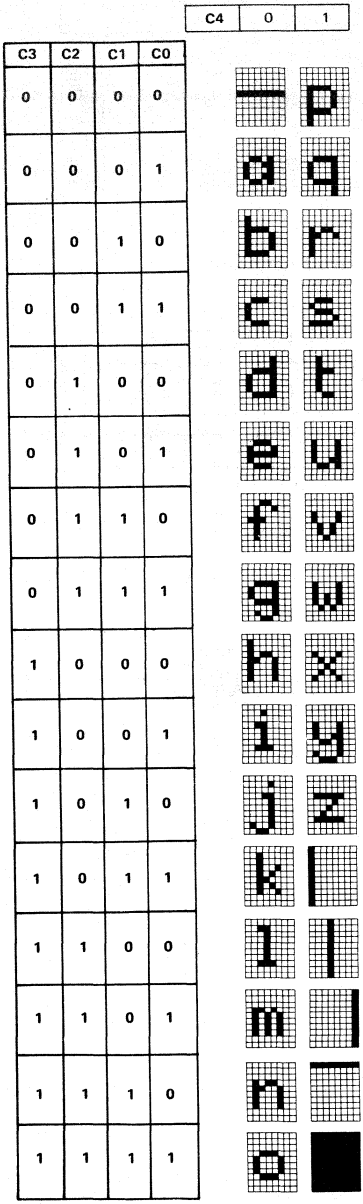
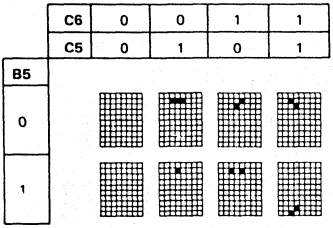


FIGURE 19 bis – G_{20} and G_{21} ACCENTUED CHARACTER SETS FOR 9345 - R003



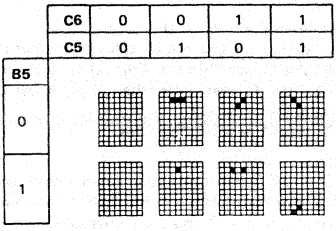
Example :

	7	6	5	4	3	2	1	0
Byte C	X	0	1	0	0	0	0	1
Byte B	0	1	0	0	X	X	X	X
Byte A	X	X	X	X	X	X	X	X

X = bits defined by user.

C3	C2	C1	C0	C4 = 0	C4 = 1
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

FIGURE 19 ter – G_{20} and G_{21} ACCENTUED CHARACTER SETS FOR 9345 - R005



Example :

	7	6	5	4	3	2	1	0
Byte C	X	0	1	0	0	0	0	1
Byte B	0	1	0	0	X	X	X	X
Byte A	X	X	X	X	X	X	X	X

X = bits defined by user.

C3	C2	C1	C0	C4 = 0	C4 = 1
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

80 CHAR/ROW CHARACTER CODES

To display pages in 80 character per row format, one of two character code formats must be selected :

- Long (12 bits) code : 4 parallel attributes and large on-chip 1024 semigraphic character set,
- Short (8 bits) code : no attribute, no semigraphic set.

Both formats address the on-chip G_0 set (128 characters 6 x 10). None allows UDS addressing.

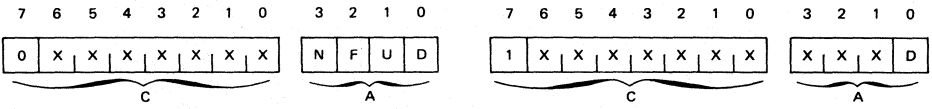
LONG CODES

Each 6 pixels x 10 lines character window on the screen is associated with a 12-bit code in memory, namely a C byte and an attribute nibble A (Figure 10). C7 bit designates the set.

- Alphanumeric set : C7 = 0.
  C(0:6) designates one out of 128 alphanumeric characters in the G_0 on-chip set. This set is common to the 40 char/row format, with the 2 right most columns truncated (see Figure 25).
  A(0:3) gives 4 parallel attributes.
- Mosaïc set : C7 = 1.
  A(1:3) and C(0:6) address a dedicated mosaïc character. Each of these address bits controls the foreground/background status of a 3 pixels x 2 lines sub-window : foreground when the bit is set.

A0 provides a color select attribute.

FIGURE 20 – 80 CHAR/ROW CHARACTER CODE

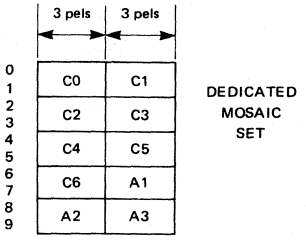


ALPHANUMERIC CHAR CODE

MOSAIC CHAR CODE

N = Negative
F = Flash
U = Underline
D = Color set

128 ALPHANUMERICS
In G_0 set.



SHORT CODES

They are derived from the long code by giving a 0 implicit value to each bit of the A nibble : positive, not underlined, not flashing.

PACKING THE CODES IN MEMORY

Long codes are paired. A pair is packed in a 3-byte word. Therefore, the 80 codes of a row fill a 120-byte row buffer (Figure 21). The left most position on the screen is even. Its corresponding C byte is at the beginning of the first buffer. The next position on the screen is odd. Its corresponding C byte is at the beginning of the second buffer. Both nibbles are packed in the third buffer. With short codes, the same scheme yields 80-byte row buffers.

ACCESS TO THE CODES IN MEMORY

KRL command transfers 12 bits from/to the R1 and R3 registers to/from memory. The read modify write operation, necessary to write the A nibble in memory, is automatically performed provided that the A nibble is repeated in the R3 register (Figure 22). Dedicated auto-incrementation is also performed when required.

KRC command does a similar job for the short codes (Figure 23).

A very simple scheme allows the microprocessor to transcode an horizontal screen location into a pointer (Figure 24). The joint use of this scheme with the dedicated command alleviates all the packing/unpacking troubles.

FIGURE 21 – 80 CHAR/ROW CODE PACKING

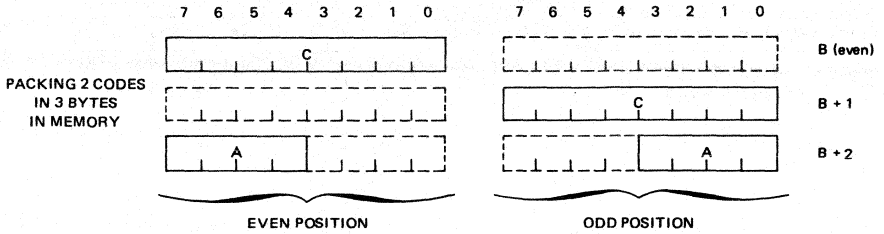


FIGURE 22 – KRL COMMAND : SEQUENTIAL ACCESS TO LONG CODES

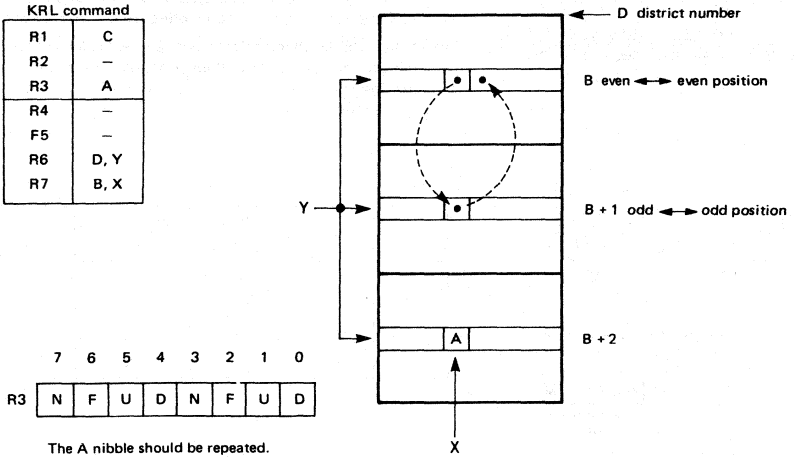


FIGURE 23 – KRC COMMAND SEQUENTIAL ACCESS TO SHORT CODES

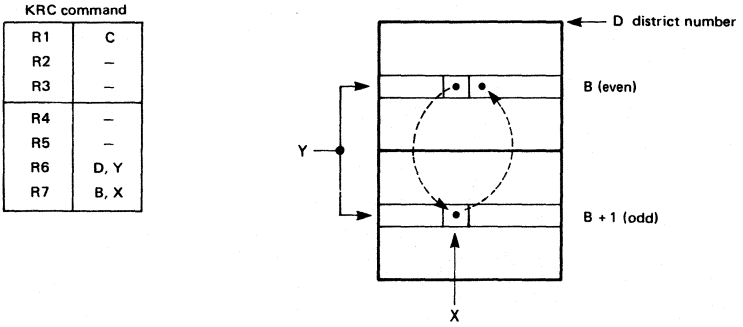
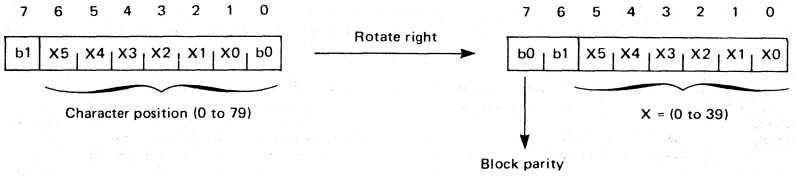


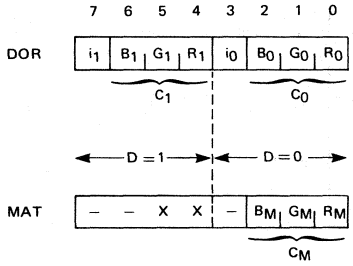
FIGURE 24 – TRANSCODING AN HORIZONTAL SCREEN LOCATION INTO A R7 POINTER



DISPLAYING THE ATTRIBUTES - DOR REGISTER

Short code and mosaïc characters are not flashing, not underlined and "positive".
The attributes are processed in the following order :

- Underline or underlined cursor : foreground is forced on the last slice (NT = 9).
- Flash : background is periodically (0.5 Hz – 50 %) forced on all the window. The phase depends on the negative attribute.
- Color select : a "positive" character is displayed with a background color same as the margin color. The foreground color is selected in DOR register by the D attribute.
- Negative : when the character is negative, background and foreground colors are exchanged. In complemented CURSOR position, these colors are complemented.
- Insert : the D attribute selects one insert value in DOR register. This attribute is then processed up to the current insertion mode (see screen format and attribute insert section).



The pixel shift frequency is f_{CLK} (12 MHz).

D	N	BACKGND COLOR	FOREGND COLOR	i
0	0	C_M	C_0	i0
0	1	C_0	C_M	i0
1	0	C_M	C_1	i1
1	1	C_1	C_M	i1

FIGURE 25 — G_0 ALPHANUMERIC CHARACTER SET IN 80 CHARACTER/ROW MODE — EF9345

C7	0	0	0	0	0	0	0	0
C6	0	0	0	0	1	1	1	1
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

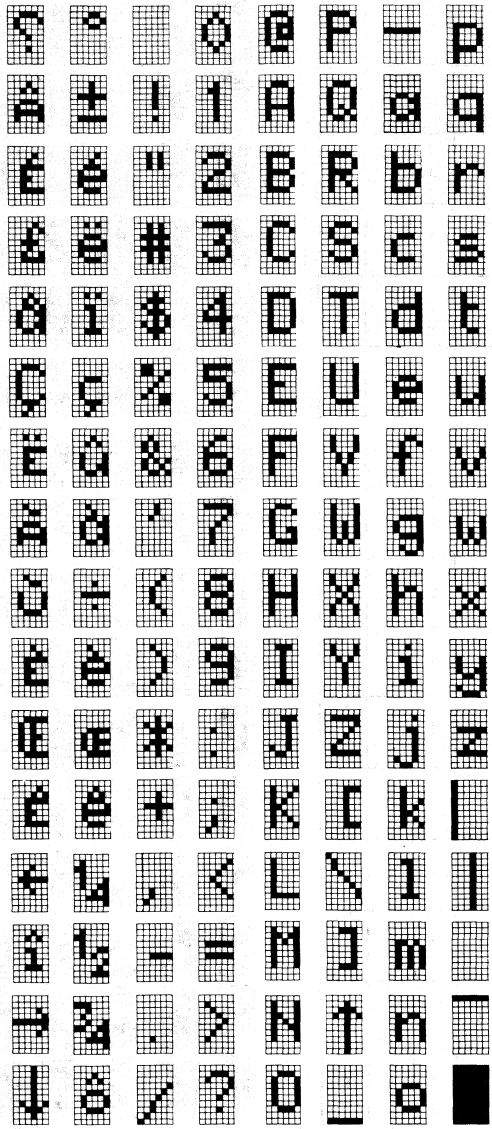


FIGURE 25 bis — G_0 ALPHANUMERIC CHARACTER SET IN 80 CHARACTER/ROW MODE — EF9345 R003

C7	0	0	0	0	0	0	0	0
C6	0	0	0	0	1	1	1	1
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

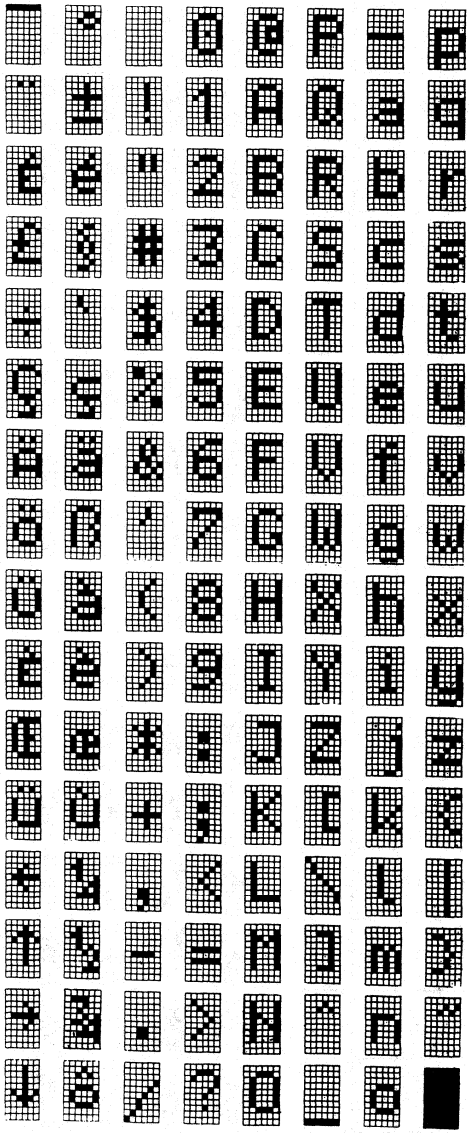
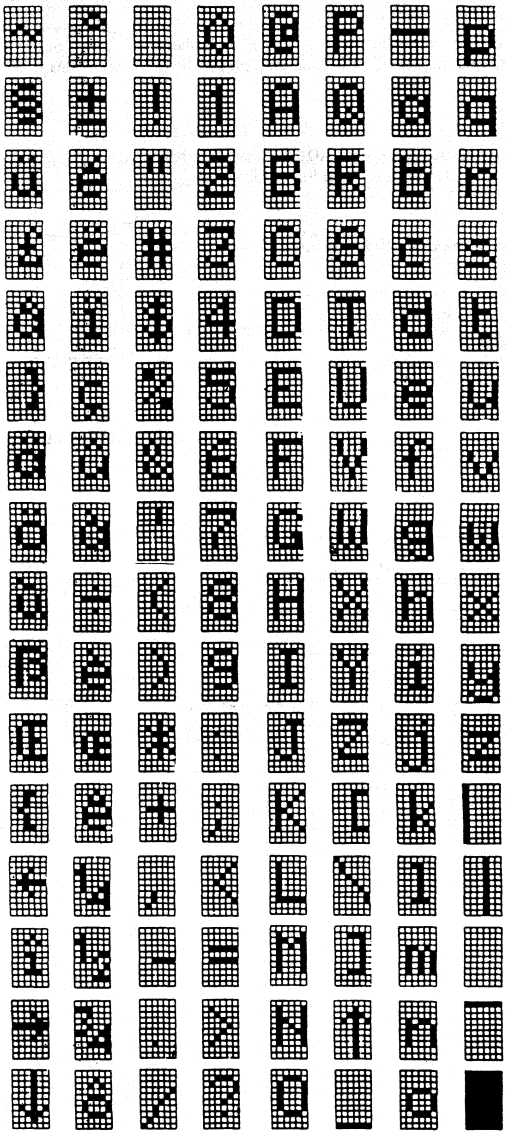


FIGURE 25 ter — G_0 ALPHANUMERIC CHARACTER SET IN 80 CHARACTER/ROW MODE — EF9345 R005

C7	0	0	0	0	0	0	0	0
C6	0	0	0	0	1	1	1	1
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



MICROPROCESSOR ACCESS COMMANDS

A microprocessor bus cycle may transfer one byte from/to the microprocessor to/from a directly addressable register. These registers provide an indirect access :

- to/from 5 on-chip indirect registers : ROR, DOR, MAT, PAT and TGS.
- to/from the private memory.

Due to address/data multiplexing, a bus cycle is a 2 phase process (see Timing diagram 1 or Timing diagram 2).

ADDRESS PHASE

The falling edge of AS latches to AD(0:7) bus state and $\overline{CS}$ signal into the temporary A address register (Figure 26).

- A(0:2) = i
  This register index designates one out of 8 direct access registers R_i.
- A3 = XQR
  This is the execution request bit.
- A(4:7) = ASN
  This is the Auto-Selection Nibble.
- A8 = $\overline{LCS}$
  This is the latched value of $\overline{CS}$ input pin.

EF9345 is selected when the following condition is met : ASN = 2 (Hexa) and $\overline{LCS}$ = 0.

Therefore, EF9345 is mapped in the hexadecimal microprocessor addressing space from XX20 to XX2F, where XX is up to the user. When EF9345 is not selected, its AD bus pins float and no register can be modified.

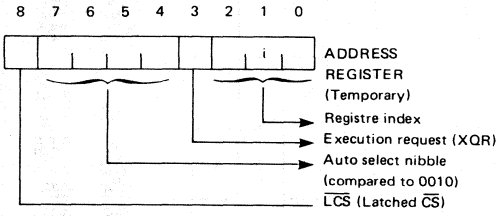
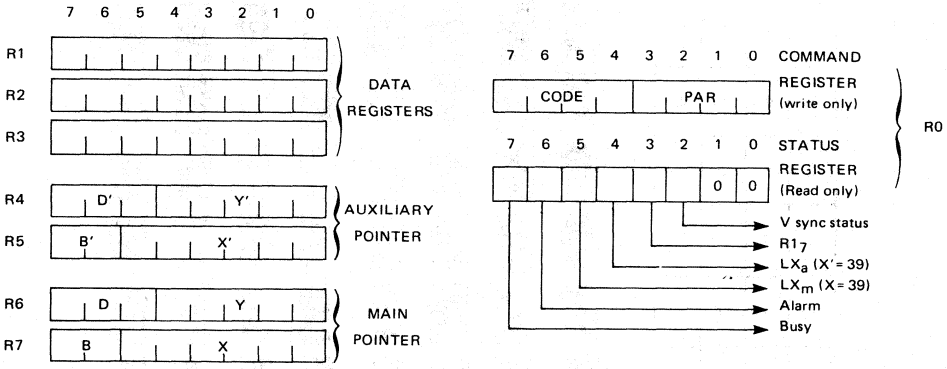


FIGURE 26 – DIRECT ACCESS REGISTERS



DATA PHASE - REGISTERS

When EF9345 is selected and while AS input is low, the R_i register is accessed.
R0 designates a write-only COMMAND register or a read-only STATUS register.
R1 to R7 hold the arguments of a command. They are read/write registers.
R1, R2, R3 are used to transfer the data.
R4, R5 hold the Auxiliary Pointer (AP).
R6, R7 hold the Main Pointer (MP).
(See memory organization ; Pointer section for pointer structure).

COMMAND REGISTER

This register holds a 4-bit command type and 4 bits of orthogonal parameters (see COMMAND TABLE).

Type

There are 4 groups of command :

- The IND command which gives access to on-chip resources,
- The fixed format character code transfer commands,
- The variable character code handling commands,
- The general purpose commands.

Parameters

R/$\overline{W}$:Direction
1 : to DATA registers (R1, R2, R3)
0 : from DATA registers.

r : Internal ressource index (see Figure 27)

I : Auto-incrementation
1 : with post auto-incrementation
0 : without auto-incrementation.

p : Pointer select
1 : auxiliary pointer
0 : main pointer

s, $\overline{s}$: Source, destination select
01 : source : MP ; destination : AP
10 : source : AP ; destination : MP

$\overline{a}$, a : Stop condition
01 : stop at end of buffer
10 : no stop.

STATUS REGISTER

This is a read-only, direct access register.

S7 : BUSY — BUSY is set at the beginning of any command execution. It is reset at completion.

S6 : AI
S5 : LX_m
S4 : LX_a
LX_m or LX_a is set when respectively the main pointer or the auxiliary pointer holds X = 39 before a possible incrementation.
The alarm bit S6 is set when LX_m or LX_a is set and an incrementation is performed after access.

S3 : Gives the MSB value of R_1.

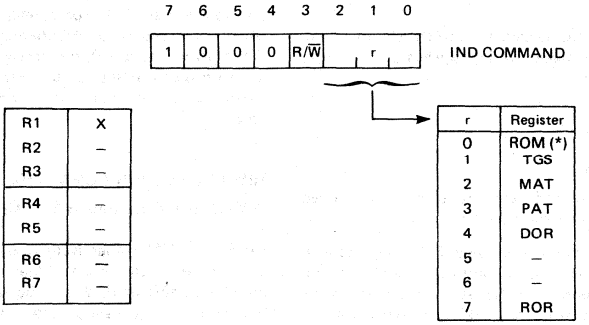
S2 : Gives the vertical synchronization signal state.
This is maskable by the VRM command.

S1 = S0 = 0 Not used.

S3 to S6 are reset at the beginning of any command.

The COMMAND TABLE shows every command able to set, each of these status bits, after completion.

FIGURE 27 – INDIRECT ON-CHIP RESOURCE ACCESS



* Note: A slice in 40C only can be read from the internal character generator. The slice address must be initialized in R6, R7.

NOTES ON COMMAND EXECUTION

1. The execution of any command starts at the trailing edge of DS when (and only when) :
   - EF9345 has been selected,
   - XQR has been set,
   at the previous AS falling edge.

This scheme allows loading a command and its argument in any order. For instance, a command, once loaded, may be re-executed with new or partly new arguments.

2. At power on, the busy state is undeterminated.
   It is recommanded to load first a dummy command with XQR = 1 before any effective command.

3. While Busy is set, the current command is under execution. Register access is then restricted .

   Register access with XQR = 0
   - Read STATUS is effective.
   - Write COMMAND or any other register access are ineffective.

That is to say, the microprocessor reads undetermined values and may not modify a register.

Register access with XQR = 1
- Read STATUS or write COMMAND are effective,
- Access to other registers is ineffective.

However, the previous command is aborted and the new command execution launched (with an initial state undetermined for registers and memory locations handled by the aborted command).

4. Execution suspension

The execution of any command (except VRM, VSM) is suspended during the last and first TV line of an active row. This is because the memory bus cannot be allocated for microprocessor access during this 104 μs period.
This holds too for internal resource access because on-chip data transfer uses internal data memory bus.

IND COMMAND (See figure 27)

This command transfers one byte between R1 and an internal resource. The r parameter designates one on-chip indirect register.

FIXED FORMAT CHARACTER CODE ACCESS : KRF, KRG, KRL KRC

Each of these commands is dedicated to transfer one complete character code between DATA registers and memory. MP is exclusively used.

KRF transfers 24 bits.
KRG transfers 16 bits.
KRL transfers 12 bits.
KRE transfers 8 bits.

Code packing, pointer and data structures are explained in the corresponding character code section.

When auto-incrementation is enabled, MP is automatically updated after access so as to point to the next location. This location corresponds to the next right position on screen. When last position (X = 39) is accessed, LX_m is set. When last position is accessed with auto-incrementation, alarm is also set. MP is then pointing back at the beginning of the row : there is no automatic Y incrementation.

VARIABLE CODE HANDLING COMMANDS : KRV, EXP, CMP, KRE

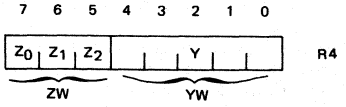
An overview on these commands is given in "handling the variable codes" (40 char./row section).

KRV uses R5 to point the attribute file. LX_a is set when this file is full (the last attribute pair has been accessed).

EXP and CMP use MP and R5 in the same way as KRV. Furthermore, R4 points to a working double buffer. These two commands process a whole row buffer and stop either at the end of the row buffer or when the file overflows. In the last case, the alarm bit is set.

KRE uses MP to point to a buffer and R4 to point to a working double buffer. R5 is unused. In other respects, KRE is identical to KRL.

For these commands, R4(5:7) hold the LSB's block address of the working buffer W.



ZW_3 is given by bit 6 of R6.

GENERAL PURPOSE ACCESS TO A BYTE - OCT

This command uses either MP or AP pointer.
When MP is in use, an overflow yields to a Y incrementation.

MOVE BUFFER COMMANDS : MVB, MVD, MVT

These are memory to memory commands which use R1 as working register.
MVB transfers a byte from source to destination, post-increments the 2 pointers and iterates until the stop condition is met. MVD and MVT are similar but work respectively with 2 byte word and 3 byte word. That is to say, MVB works on buffers, MVD on double buffers and MVT on triple buffers. If the parameter a = 1, the process stops when either source or destination buffer end is reached. If the parameter a = 0, the process never stops until aborted. In this case, main pointer overflow yields to a Y incrementation in MP. So, a whole block or page may be initialized.

MISCELLANEOUS COMMANDS : INY, VRM and VSM

INY command increments Y in MP.

VRM and VSM respectively reset and set a vertical synchronization status mask. When the mask is set, status bit S2 remains at 0. When the mask is reset, status S2 follows the vertical sync. state : it is reset for 2 TV lines per frame and stays at 1 during the remaining period. It becomes readable by the microprocessor from the status register. After power on, the mask state is undetermined.

COMMAND TABLE

TYPE	MEMO	CODE				PARAMETER				STATUS				ARGUMENTS							EXECUTION TIME (1)	
		7	6	5	4	3	2	1	0	AI	LX_m	LX_a	$R1_7$	R1	R2	R3	R4	R5	R6	R7	WRITE	READ
INDIRECT	IND	1	0	0	0	R/$\overline{W}$		r		0	0	0	0	D	–	–	–	–	MP		2	3.5
40 CHARACTERS - 24 BITS	KRF	0	0	0	0	R/$\overline{W}$	0	0	I	X	X	0	0	C	B	A	–	–	MP		4	7.5
40 CHARACTERS - 16 BITS	KRG	0	0	0	0	R/$\overline{W}$	0	1	I	X	X	0	0	A*	B*	W	–	–	MP		5.5	7.5
80 CHARACTERS - 8 BITS	KRC	0	1	0	0	R/$\overline{W}$	0	0	I	X	X	0	0	C	–	–	–	–	MP		9	9.5
80 CHARACTERS - 12 BITS	KRL	0	1	0	1	R/$\overline{W}$	0	0	I	X	X	0	0	C	–	A	–	–	MP		12.5	11.5
40 CHARACTERS VARIABLE	KRV	0	0	1	0	R/$\overline{W}$	0	0	I	X	X	X	X	C	B	A	–	XF	MP		(2) 3 + 3 + j	3.5 + 6 • j
EXPANSION	EXP	0	1	1	0	0	0	0	0	X	0	X	0	C	B	A	PW	XF	MP		(3) < 247	–
COMPRESSION	CMP	0	1	1	1	0	0	0	0	X	0	X	0	C	B	A	PW	XF	MP		(3) < 402	–
EXPANDED CHARACTERS	KRE	0	0	0	1	R/$\overline{W}$	0	0	I	X	X	0	0	C	B	A	PW	–	MP		4	7.5
BYTE	OCT	0	0	1	1	R/$\overline{W}$	p	0	I	X	X	X	0	D	–	–	AP		MP		4	4.5
MOVE BUFFER	MVB	1	1	0	1	s	$\overline{s}$	$\overline{a}$	a	0	0	0	0	W	–	–	AP		MP		(2) 2 + 4.n	–
MOVE DOUBLE BUFFER	MVD	1	1	1	0	s	$\overline{s}$	$\overline{a}$	a	0	0	0	0	W	–	–	AP		MP		(2) 2 + 8.n	–
MOVE TRIPLE BUFFER	MVT	1	1	1	1	s	$\overline{s}$	$\overline{a}$	a	0	0	0	0	W	–	–	AP		MP		(2) 2 + 12.n	–
CLEAR PAGE (4) - 24 BITS	CLF	0	0	0	0	0	1	0	1	X	X	0	0	C	B	A	–	–	MP		< 4700 (1 K code)	–
CLEAR PAGE (4) - 16 BITS	CLG	0	0	0	0	0	1	1	1	X	X	0	0	A*	B*	W	–	–	MP		< 5800 (1 K code)	–
VERTICAL SYNC MASK SET	VSM	1	0	0	1	1	0	0	1	0	0	0	0	–	–	–	–	–	–	–	1	–
VERTICAL SYNC MASK RESET	VRM	1	0	0	1	0	1	0	1	–	–	–	–	–	–	–	–	–	–	–	1	–
INCREMENT Y	INY	1	0	1	1	0	0	0	0	0	0	0	0	–	–	–	–	–	Y	–	2	–
NO OPERATION	NOP	1	0	0	1	0	0	0	1	–	–	–	–	–	–	–	–	–	–	–	1	–

p : Pointer select
1 : auxiliary pointer
0 : main pointer.

s, $\overline{s}$: Source, destination
01 : source = MP ; destination = AP
10 : source = AP ; destination = MP

$\overline{a}$, a : Stop condition
01 : stop at end of buffer
10 : no stop

r : Indirect register number.

– : Not affected
W : Used as working register
PW (ZW, YW) : Working buffer
X : Set or Reset
XF : X File
I : Pointer incrementation
D : Data
MP : Main pointer
AP : Auxiliary pointer.

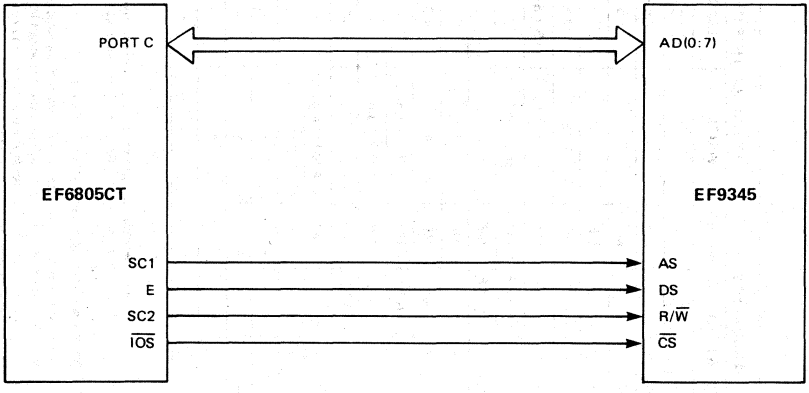
(1) Unit : 12 clock periods ($\simeq 1\ \mu s$) without possible suspension.

(2) n : total number of words $\leqslant 40$; j = 1 for long codes, j = 0 for short codes.

(3) Worst case (20 long codes + 20 short codes).

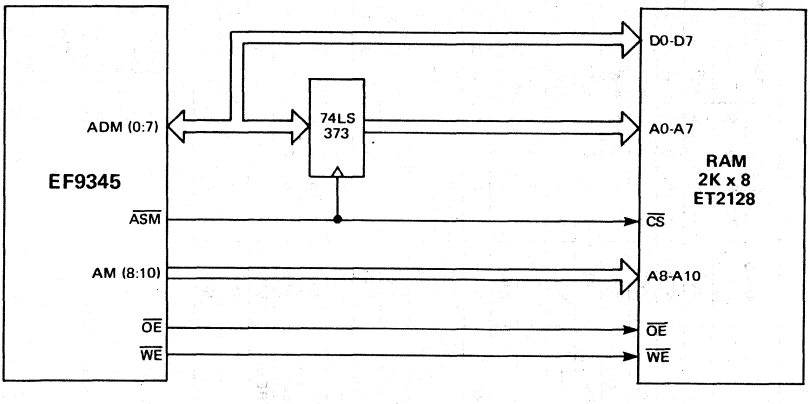
(4) These commands repeat KRF or KRG with Y incrementation when X overflows. When the last position is reached in a row, Y is incremented and the process starts again on the next row. These commands stop only with abort.

INTERFACE WITH EF6805CT



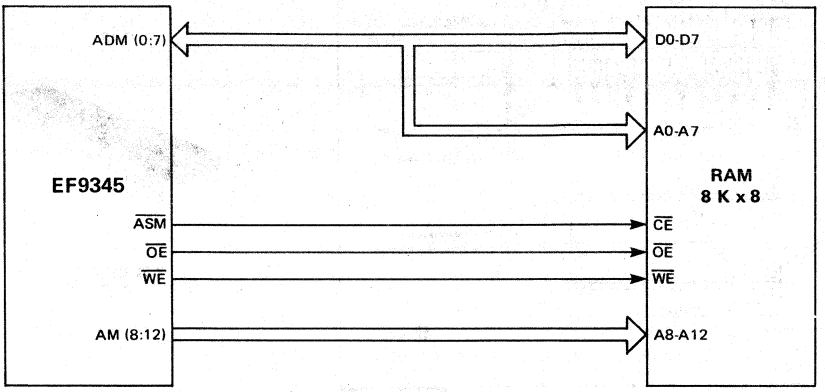
MINIMUM APPLICATION WITH 2K x 8 MEMORY

One page memory terminal in 16-bit fixed format or 24-bit compressed format.



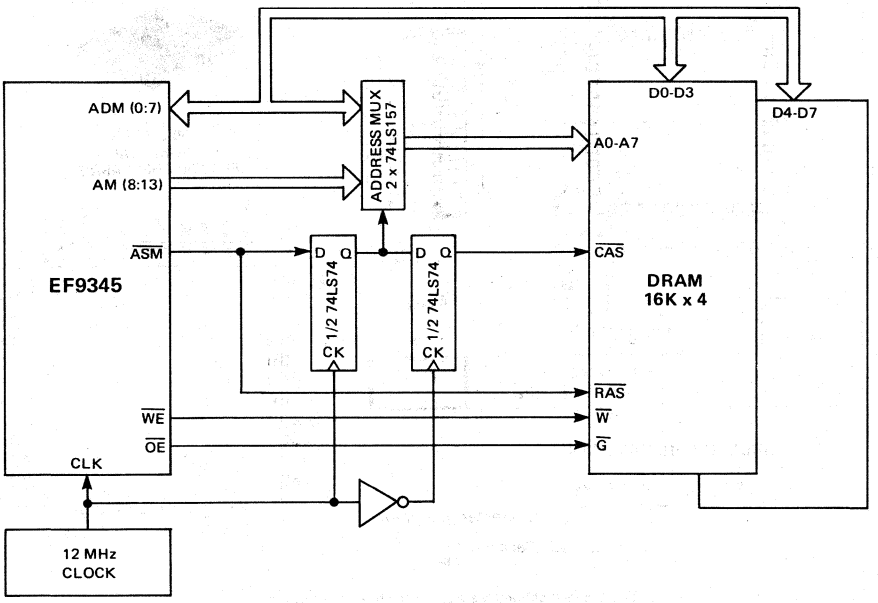
TYPICAL APPLICATION WITH 8K x 8 DYNAMIC OR PSEUDO-STATIC RAM

Multipage terminal with possibility of multiple user definable character sets.

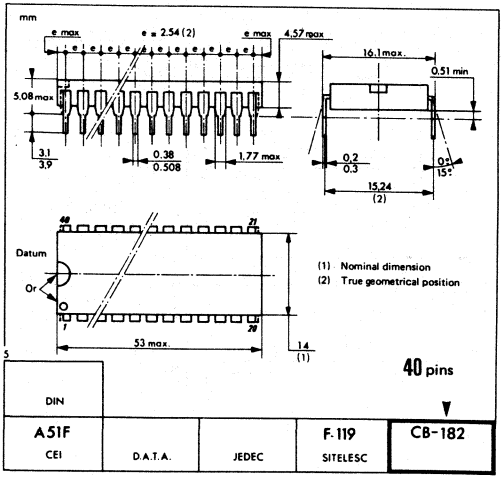


MAXIMUM APPLICATION WITH 16K x 8 MEMORY

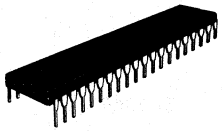
Multipage terminal with user definable character sets and buffer areas.



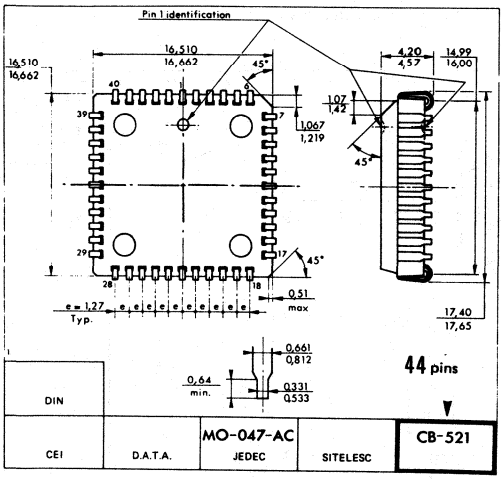
PHYSICAL DIMENSIONS



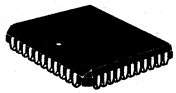
CB-182



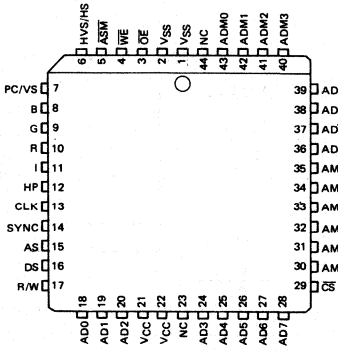
P SUFFIX
PLASTIC PACKAGE



CB-521



FN SUFFIX
SURPICOP
(PLASTIC CHIP-CARRIER)



ORDERING INFORMATION

EF9345 XX RYYY

- RYYY → Character generator
- XX → Package: P, FN

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

THOMSON COMPONENTS MICONDUCTEURS

EF9369

SINGLE CHIP COLOR PALETTE

The EF9369 single chip palette provides a low cost, yet remarkable enhancement for any low to mid-range color graphics application. It allows displaying up to 16 different colors, each of these colors being freely selected out of 4096 preset values. EF9369 contains a 16 register color look-up table, three 4-bit D/A converters and a microprocessor interface for color loading.

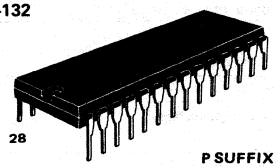
- On chip color look-up table
- 4096 color palette (16 colors selected from 4096)
- On-chip three 4-bit resolution video DACs with γ law correction
- Dot rate up to 30 Megadots per second
- Marking bit for inlay purpose
- Versatile microprocessor interface :
  - directly compatible with address/data multiplexed 8-bit microprocessor bus such as 6801, EF6805CT, 8051...
  - directly compatible with non-multiplexed 8 or 16-bit microprocessor bus (6809, 6502, 68008...).
- Single 5 V supply
- HMOS 2 technology.

HMOS2

SINGLE CHIP COLOR PALETTE

CASES

CB-132

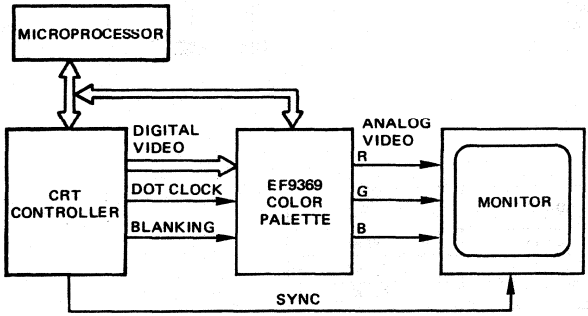


P SUFFIX
PLASTIC PACKAGE

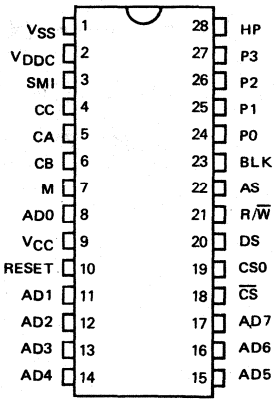
CB-520

FN SUFFIX
PLCC 28

TYPICAL APPLICATION



PIN ASSIGNMENT



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}*	- 0.3 to 7.0	V
Input voltage	V_{in}*	- 0.3 to 7.0	V
Operating temperature range	T_A	0 to 70	°C
Storage temperature range	T_{stg}	- 55 to 150	°C
Max power dissipation	P_{Dm}	0.45	W

*With respect to V_{SS}

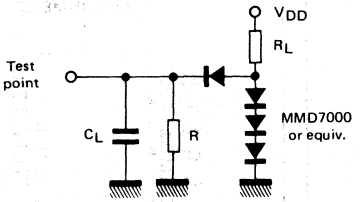
Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

ELECTRICAL OPERATING CHARACTERISTICS

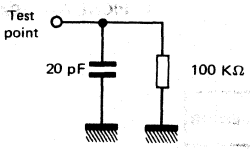
(V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70°C))

Characteristic		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5	5.25	V
Analog supply voltage		V_{DDC}	–	V_{CC}	TBD	V
Analog supply current		I_{DDC}	–	20	–	mA
Input low voltage		V_{IL}	- 0.3	–	0.8	V
Input high voltage	RESET	V_{IH}	3	–	V_{CC}	V
	All other inputs		2	–	V_{CC}	
Input leakage current		I_{in}	–	–	20	µA
Output high voltage (I_{load} = - 500 µA)		V_{OH}	2.4	–	–	V
Output low voltage (I_{load} = 1.6 mA)		V_{OL}	–	–	0.4	V
Power dissipation		P_D	–	250	–	mW
Input capacitance		C_{in}	–	–	15	pF
Three state (off state) input current		I_{TSI}	–	–	10	µA

Test load for digital output



Test load for analog output

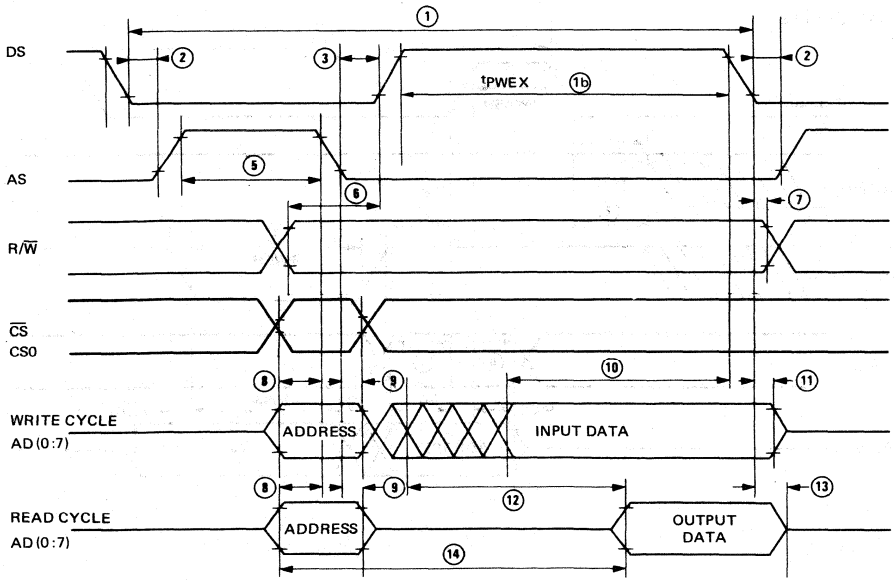


	AD(0:7)	M
C	100 pF	50 pF
R_L	1 KΩ	3.3 KΩ
R	4.7 KΩ	4.7 KΩ

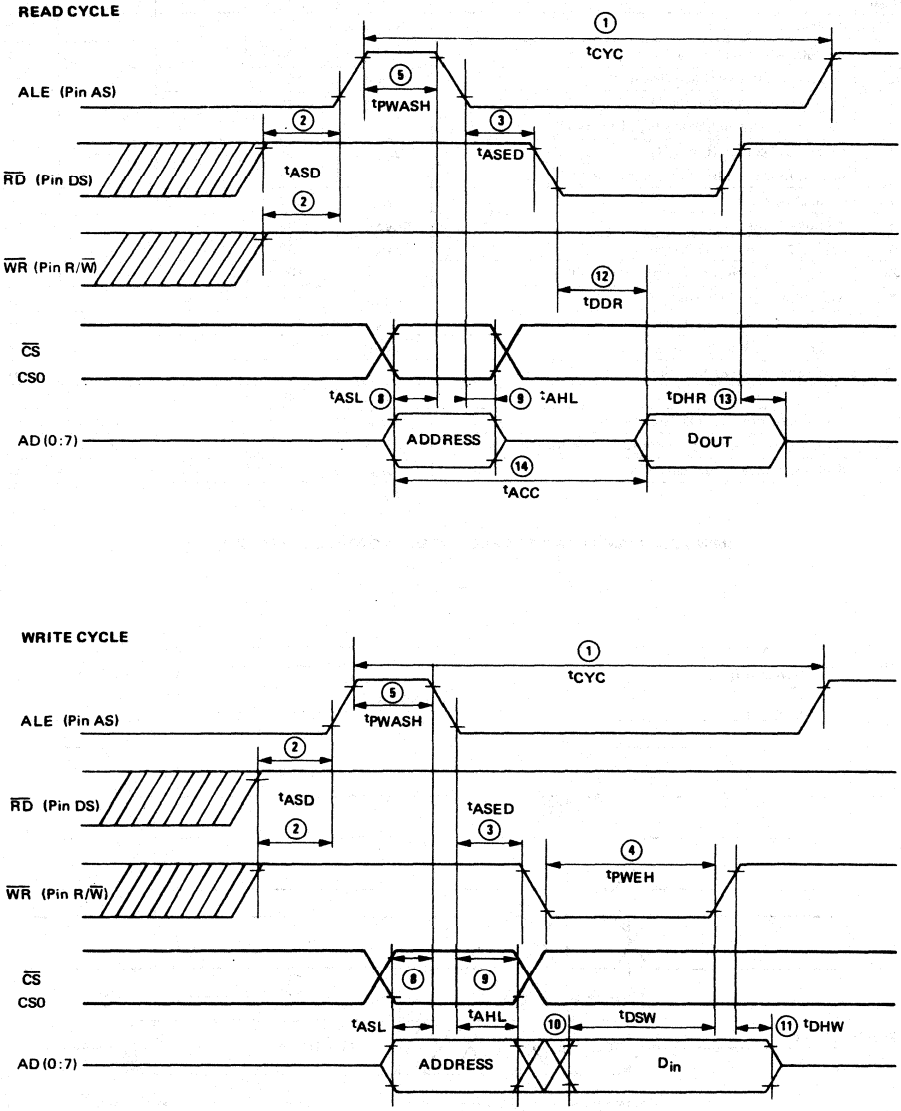
MICROPROCESSOR INTERFACE TIMING AD(0:7), AS, DS, R/$\overline{W}$, $\overline{CS}$, CS0
V_{CC} = 5.0 ± 5 %, T_A = 0° to +70°C, C_L = 100 pF on AD(0:7)
Reference levels : V_{IL} = 0.8 V and V_{IH} = 2 V on all inputs ; V_{OL} = 0.4 V and V_{OH} = 2.4 V on all outputs.

Ident. number	Characteristic	Symbol	Min	Typ	Max	Unit
1	Cycle time	t_{CYC}	400	–	–	ns
1b	DS pulse width high time	t_{PWEX}	200	–	–	ns
1c	DS pulse width low time (Timing 3)	t_{PWEL}	100	–	10000	ns
2	DS low to AS high (timing 1) DS high or R/$\overline{W}$ high to AS high (timing 2)	t_{ASD}	30	–	–	ns
3	AS low to DS high (timing 1) AS low to DS low or R/$\overline{W}$ low (timing 2)	t_{ASED}	30	–	–	ns
4	Write pulse width	t_{PWEH}	200	–	–	ns
5	AS pulse width	t_{PWASH}	100	–	–	ns
6	R/$\overline{W}$ to DS setup time (timing 1)	t_{RWS}	100	–	–	ns
6b	R/$\overline{W}$, AS, $\overline{CS}$, CS0 to DS setup time (timing 3)		100	–	–	
7	R/$\overline{W}$ to DS hold time (timing 1)	t_{RWH}	10	–	–	ns
8	Address and $\overline{CS}$, CS0 setup time	t_{ASL}	20	–	–	ns
9	Address and $\overline{CS}$, CS0 hold time	t_{AHL}	20	–	–	ns
10	Data setup time (write cycle)	t_{DSW}	100	–	–	ns
11	Data hold time (write cycle)	t_{DHW}	10	–	–	ns
12	Data access time from DS (read cycle)	t_{DDR}	–	–	150	ns
13	DS inactive to high impedance state time (read cycle)	t_{DHR}	10	–	80	ns
14	Address to data valid access time	t_{ACC}	–	–	300	ns

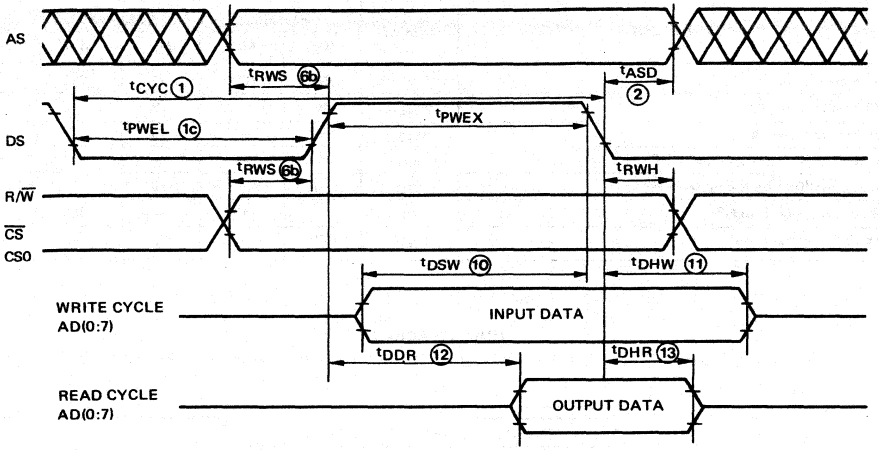
TIMING DIAGRAM 1 – MULTIPLEXED MODE - MOTOROLA TYPE (SMI = V_{SS})



TIMING DIAGRAM 2 – MULTIPLEXED MODE - INTEL TYPE (SMI = V_{SS})



TIMING DIAGRAM 3 – NON-MULTIPLEXED MODE (SMI = V_{CC})

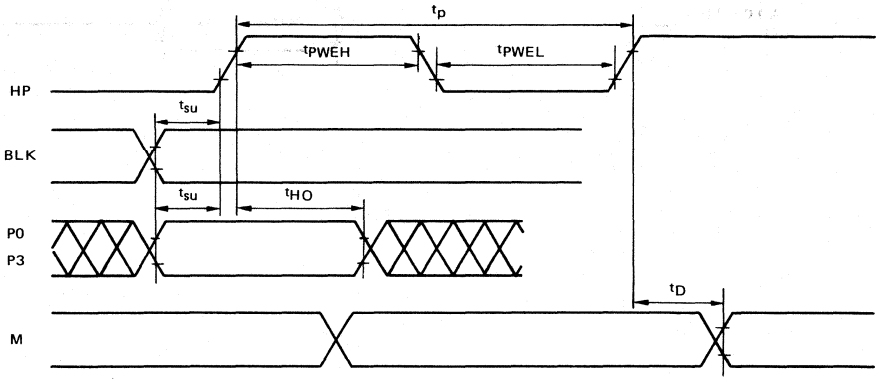


DIGITAL VIDEO SIGNALS - HP, P(0:3), BLK, M, RESET

V_{CC} = 5.0 ± 5 %, T_A = 0°C to + 70°C, C_L = 50 pF on M.
Reference levels : V_{IL} = 0.8 V and V_{IH} = 2 V on all inputs ;
V_{OL} = 0.4 V and V_{OH} = 2.4 V on all outputs.

Characteristic	Symbol	EF9369		EF9369-30		Unit
		Min	Max	Min	Max	
HP clock period	t_P	58	1000	33	1000	ns
HP high pulse width	t_{PWEH}	25	–	13	–	ns
HP low pulse width	t_{PWEL}	25	–	13	–	ns
BLK and P(0:3) set up time to HP	t_{SU}	5	–	5	–	ns
BLK and P(0:3) hold time from HP	t_{HO}	10	–	10	–	ns
M output delay from HP	t_D	–	45	–	30	ns
RESET high pulse width	t_{PWRL}	400	–	400	–	ns

TIMING DIAGRAM 4



ANALOG VIDEO OUTPUTS - CA, CB, CC

V_{DCC} = 5 V, T_A = 0° to+ 70°C, C_L = 20 pF, R_L = 100 kΩ

TABLE 1

Binary input		Analog output (V)		
		Min	Typ	Max
Low level	0000	–	0.8	–
	0001	–	1.18	–
	0010	–	1.28	–
	0011	–	1.36	–
	0100	–	1.42	–
	0101	–	1.47	–
	0110	–	1.52	–
	0111	–	1.56	–
	1000	–	1.60	–
	1001	–	1.63	–
	1010	–	1.66	–
	1011	–	1.69	–
	1100	–	1.72	–
	1101	–	1.75	–
	1110	–	1.78	–
High level	1111	–	1.80	–

Note :
The internal A/D converters deliver on CA, CB and CC outputs 16 levels with γ law correction (γ = 2.8). The typical transfer characteristic is given by :

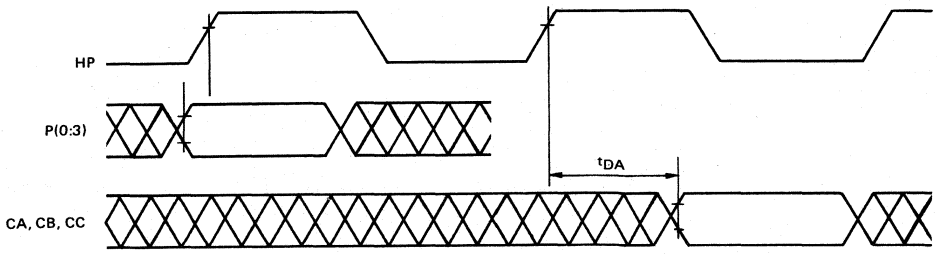
$$V = (\frac{N}{15})^{\frac{1}{2.8}} \cdot \frac{V_{DDC}}{5} + 0.16\, V_{DCC}$$

Where N is the binary input value.

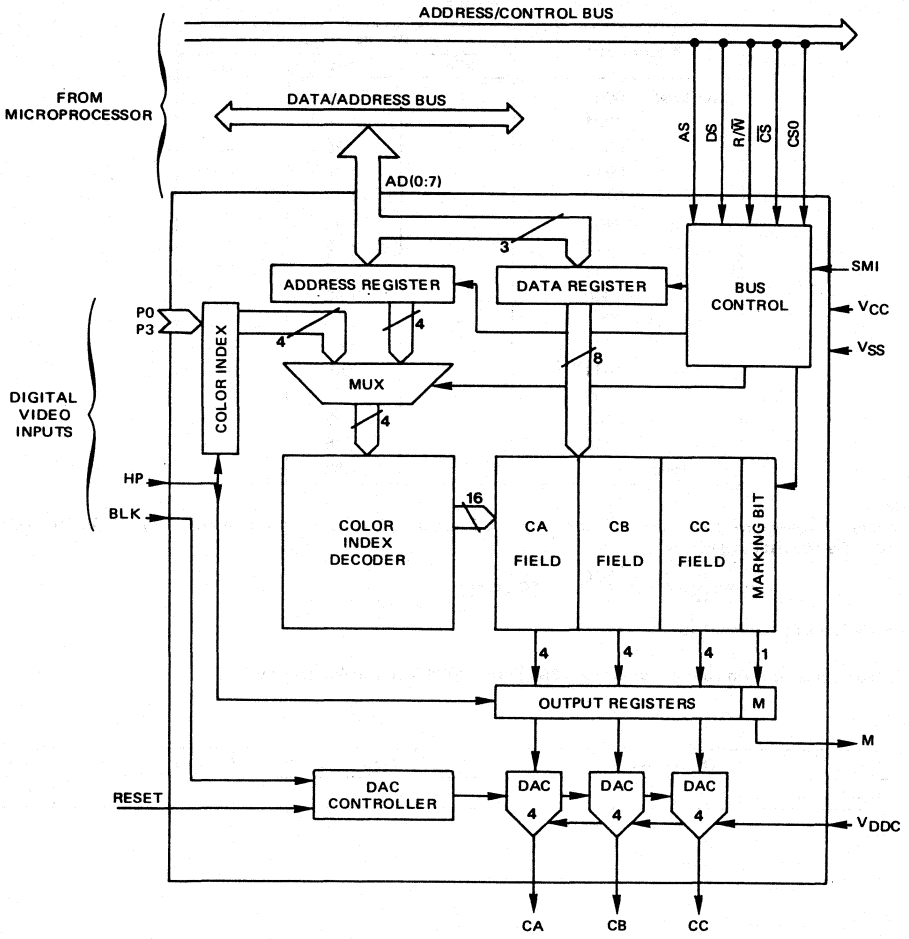
The typical analog video output impedance is 300 Ω for EF9369-30 and 400 Ω for EF9369.

Characteristic	Symbol	Min	Typ	Max	Unit
CA, CB, CC outputs from HP	t_{DA}	–	80	–	ns

TIMING DIAGRAM 5



BLOCK DIAGRAM



PIN DESCRIPTION

MICROPROCESSOR INTERFACE
All the input/output pins are TTL compatible.

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
AD(0:7)	I/O	8-11-14 15 - 17	Multiplexed address/data bus	These 8 bidirectional pins are to be connected to the microprocessor system bus.
SMI	I	3	Interface mode select	When this input is connected to V_{CC}, the EF9369 is in the non multiplexed mode. When this input is connected to V_{SS} (ground), the EF9369 is in a multiplexed mode to provide a direct interface with either Motorola or Intel type microprocessor.
AS	I	22	Address strobe	In non-multiplexed mode, this input selects either the address register (AS = 1) or the data register (AS = 0) to be accessed. In multiplexed mode, the falling edge of this control signal latches the address on the AD(0:7) lines, the state of the Data Strobe (DS) and Chip Select lines ($\overline{CS}$, CS0). When using Intel type microprocessor, this input must be connected to the ALE control line.
DS	I	20	Data strobe	In non-multiplexed mode, this active high control signal enables the AD(0:7) input/output buffers and strobes data to/from the EF9369. This signal is usually derived from the processor E ($\phi 2$) clock. In multiplexed mode, the input is strobed by the falling edge of AS. The strobe value selects either Motorola or Intel type. When using an Intel type microprocessor, DS must be connected to the $\overline{RD}$ control line. With a Motorola type microprocessor, DS must be connected to E($\phi 2$) clock.
R/$\overline{W}$	I	21	Read/Write	This control signal determines whether the EF9369 is read (R/$\overline{W}$ = 1) or written (R/$\overline{W}$ = 0). When using Intel type microprocessor, this input must be connected to the $\overline{WR}$ control line.
$\overline{CS}$ CS0	I	18 19	Chip Select	$\overline{CS}$ must be low and CS0 must be high to select the EF9369. In non-multiplexed mode, the EF9369 remains selected as long as the selection condition is met. In multiplexed mode, the selection condition is latched when AS is low.

VIDEO INTERFACE

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
P(0:3)	I	24 - 27	Pixel inputs	These four TTL compatible inputs are strobed by HP into the color index register to address the color look-up table.
HP	I	28	Dot clock	The rising edge of this input latches the P(0:3) and BLK inputs into the EF9369 and the data out of the color look-up table into the output registers.
M	O	7	Marking	This output is synchronised by HP and delivers the marking bit value from the color look-up table.
CA CB CC	O	5 6 4	Color outputs	These three analog high impedance outputs deliver the color signal levels from the internal D/A converters (DAC). The delay between CA, CB, CC outputs and the latched value P(0:3) is one HP clock period plus t_{DA} (see Timing Diagram 5).
BLK	I	23	Blanking	A high level on this input forces the CA, CB, CC and M outputs to low level.
RESET	I	10	Reset	This active high input forces the CA, CB, CC, outputs to low level until the next microprocessor access to the device.

OTHER PINS

V_{CC}	S	9	Power supply	+ 5 V.
V_{DDC}	S	2	Analog power supply	Power supply for the internal DACs. This input can be connected to V_{CC}.
V_{SS}	S	1	Power supply	Ground.

FUNCTIONAL DESCRIPTION

EF9369 contains a 16 register Color-Look Up Table (CLUT). Each of these 13-bit register holds three 4-bit color fields CA (0:3), CB (0:3) and CC (0:3) and a marking bit M.

These registers can be accessed (read or write) by the microprocessor through the microprocessor interface. These registers are also read by the video process : a 4-bit pixel value and a clock must be provided at pixel rate to the P(0:3) and HP input pins. These signals may be delivered either by 4 video shift registers and the shifting clock of a bit map CRT controller or by an alphanumeric or semigraphic CRT controller. The pixel value, after clock resynchronisation, is used as a color index : it selects one out of the 16 CLUT registers. Each color field of the selected register is converted to an analog signal and delivered to one of the CA, CB or CC output. The marking bit is directly routed to the M output. When the CA, CB and CC outputs are used as RGB analog signals, one color out of 4096 is associated to each pixel value. In short this process freely maps a 16 color index set into a 4096 color set.

MICROPROCESSOR INTERFACE

The 8-bit microprocessor interface gives access (read or write) to the CLUT which is addressed as a 32 byte table. The 13-bit color register # N (N = 0 to 15) is accessed at address 2N and 2N + 1. Even address holds CA (0:3) and CB (0:3), odd address holds CC (0:3) and M (see fig. 1).

EF9369 provides two bus modes through the SMI programming pin :

- Multiplexed mode for address/data multiplexed 8-bit microprocessor bus.
- Non-multiplexed mode for non-multiplexed 8 or 16-bit microprocessor bus.

MULTIPLEXED MODE (SMI connected to V_{SS})

In this mode, EF9369 can be directly connected to popular address/data multiplexed microprocessor, either Motorola type (6801, EF6805CT...) or Intel type (8048, 8051, 8088..). In this last case the EF9369 AS, DS and R/$\overline{W}$ inputs must be connected respectively to the ALE, $\overline{RD}$ and $\overline{WR}$ microprocessor control lines.

FIGURE 1 – CLUT ADDRESSING

Color Look-Up Table (CLUT)								CLUT Byte Address								Register Index
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	#
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	0	0	0	0	0	0
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	0	0	0	0	1	
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	0	0	0	1	0	1
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	0	0	0	1	1	
≈																≈
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	1	1	1	1	0	15
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	1	1	1	1	1	

X = don't care.

In this mode, EF9369 maps into the microprocessor addressing space as 32 CLUT byte address. Random access to one byte takes one cycle : on the falling edge of the AS input, EF9369 latches AD (0:7) into the on-chip address register, the DS and chip select lines into dedicated flip-flops. The strobed value of DS allows recognition of Intel or Motorola type for further processing. (See pin description section and microprocessor timing diagrams for details). When the EF9369 chip select lines enable selection, the addressed byte is accessed during the data phase of the cycle.

NON MULTIPLEXED MODE (SMI connected to V_{CC})

In this mode EF9369 can be directly connected to any 8 or 16-bit, non multiplexed, microprocessor bus (6800, 6809, 6502, 68008...).

This mode provides an indirect, auto-incremented addressing scheme. EF9369 maps into the microprocessor addressing space as 2 byte address only. AS is used to select one out of 2 registers :

- the write only address register (5 bits) addressed when AS = 1.
- the read/write data register (8 bits) addressed when AS = 0.

Random access to a CLUT byte takes two bus cycles :
1/ Load the CLUT address into the address register.
2/ Access (read or write) the value in the data register.

After each access to the data register, the address register is automatically incremented modulo 32. This scheme allows sequential addressing to the CLUT without address reloading, the complete CLUT can so be reloaded in 33 bus cycles.

VIDEO PROCESS

The CRT controller sends to EF9369 a pixel value on pins P (0:3), a pixel rate clock on HP input and a blanking signal on pin BLK. The pixel value is latched into the color index register by the rising edge of HP. The color index register selects one register in the CLUT. The color fields of the selected register are routed to 3 DACs and M is directly routed to the M digital output.

After impedance matching, the CA, CB, and CC outputs can be used to drive a RGB analog color monitor. Alternatively one of these outputs can be used to drive a monochrome monitor thus providing up to 16 gray levels. The marking digital output can be used to drive analog video switches, thus providing video overlay facility on a color per color basis.

The blanking input forces the analog outputs and the M output to low level thus allowing the beam to be switched off during retrace intervals.

NOTES

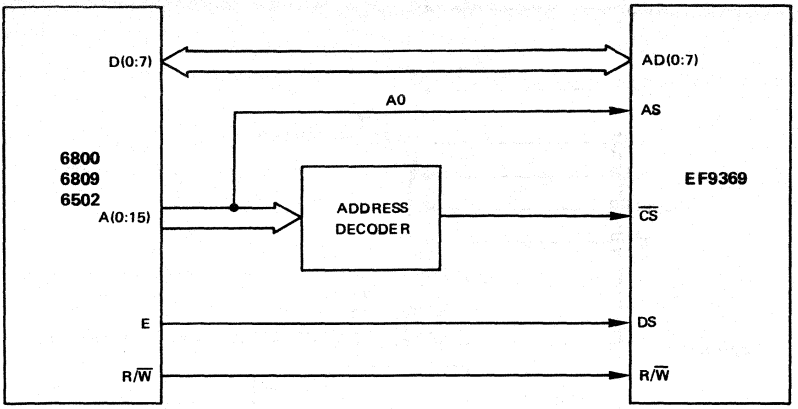
1. Each 4 bit-D/A converter is γ corrected in order to linearize the luminance driven on the screen versus the digital value. The typical digital to voltage conversion law is given table 1. The output voltages are proportionnal to the analog supply voltage V_{DDC}. When required, setting V_{DCC} allows a gain adjustment. But in most applications, V_{DDC} and V_{DD} can be derived from the same supply through independent decoupling.

2. CA, CB and CC are high impedance outputs (500 Ω typical) which require proper adaptation in most applications. THOMSON SEMICONDUCTORS TEA 5114 provides such a 1 V - 75 Ω low cost adaptation. (See fig. 2).

3. As the CLUT is shared between microprocessor access and video access, a low level is forced on the CA, CB, CC and M outputs during any chip select periods. To avoid to spoil the screen with black strokes it is recommended to access the CLUT from the microprocessor only during the retrace periods.

4. RESET - This input forces CA, CB, CC and M outputs to a low level until the next microprocessor access. At power on or at the beginning of a session RESET allows to keep a clean black screen until proper initialization.

INTERFACE WITH 6800/6809 TYPE MICROPROCESSOR



INTERFACE WITH EF6805CT

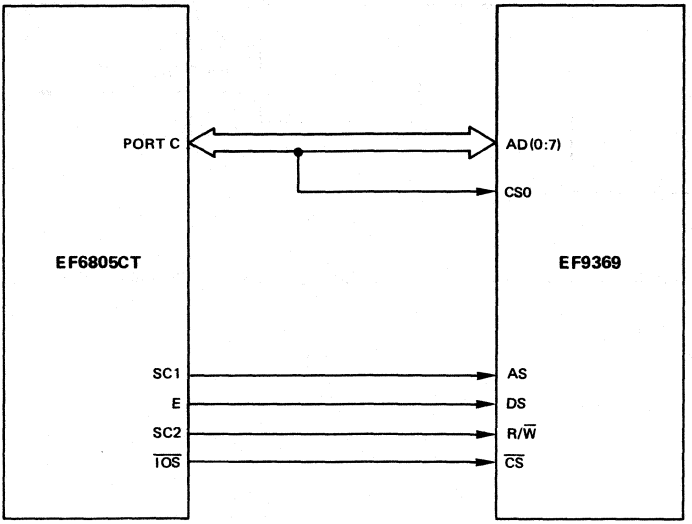
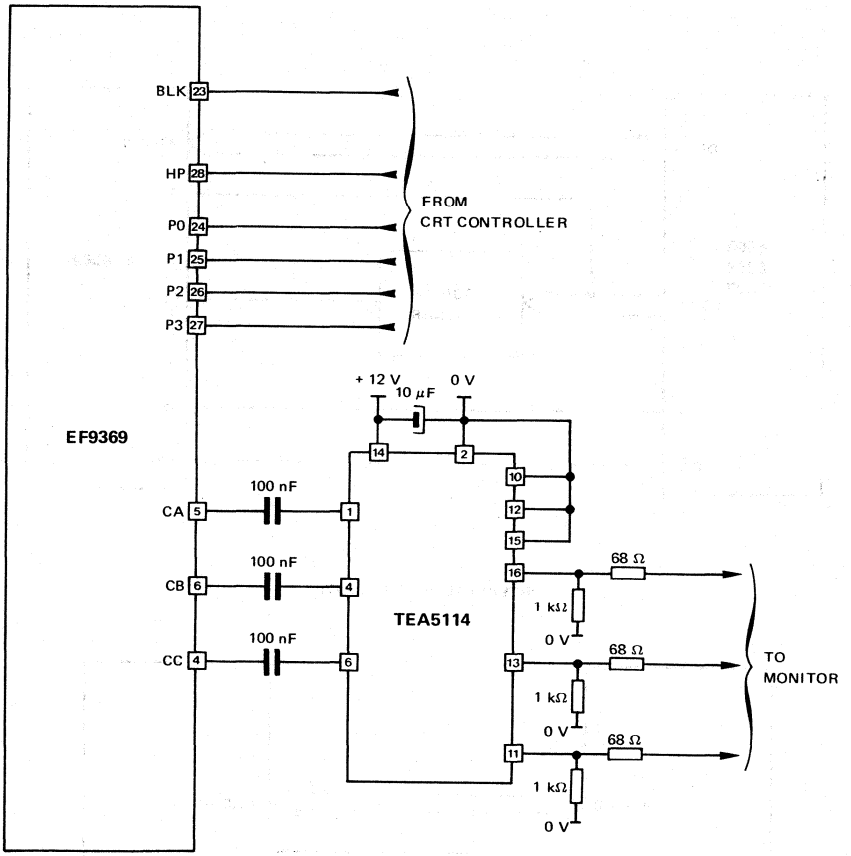


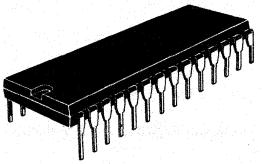
FIGURE 2 – TYPICAL 1 V - 75 Ω VIDEO INTERFACE



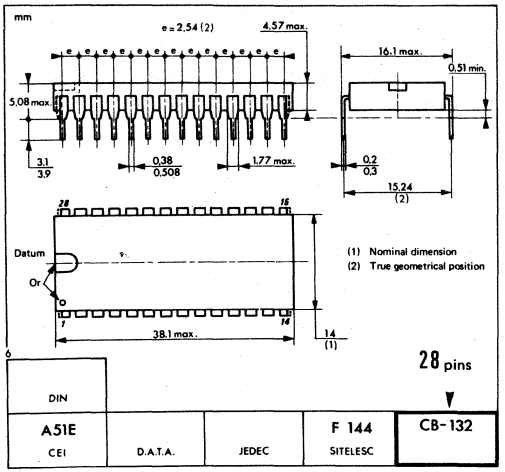
NOTE : Each digital or analog ground must be separately connected to EF9369 pin 1. (See AN-059).

PHYSICAL DIMENSIONS

CB-132

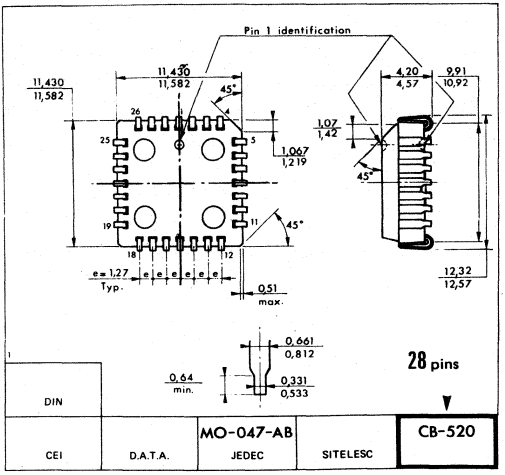


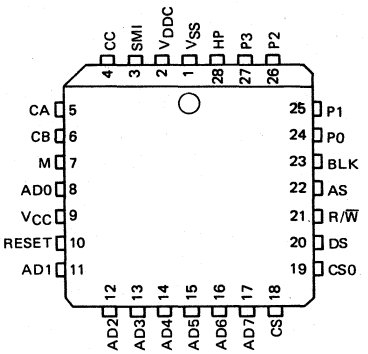
P SUFFIX
PLASTIC PACKAGE



CB-520

FN SUFFIX
PLCC 28





This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

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THOMSON COMPONENTS SEMICONDUCTEURS

TS68494

HMOS2 PALETTE AND SERIAL PORT CONTROLLER

PRODUCT PREVIEW

The TS68494 single chip color palette can be used in any low to mid range color graphics application to provide up to 256 colors freely selected between 4096 values.

Moreover, the TS68494 integrates a serial port controller for dual port video-RAM.

Powerful and cost effective graphics and text application may be achieved with THOMSON-SEMICONDUCTEURS Graphics processor family (TS68483/68493) and TS68494 chip set.

Main features :

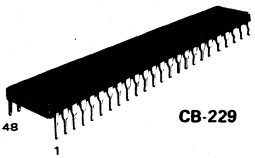
- One chip color look-up table
- 256 colors 8 bits/pixel) between 4096
- Up to 35 Mpixels/sec
- Three on-chip 4-bit video DACs
- RS-343A compatible video outputs
- Serial port controller for dual port video-RAM
- Logical operation between pixel value and programmable masks
- Horizontal zoom and panning capability
- Standard microprocessor interface, TS68000 compatible
- Single 5V supply
- 44 pin PLCC and 48 DIL packages

HMOS2
PALETTE AND SERIAL PORT CONTROLLER

CASES

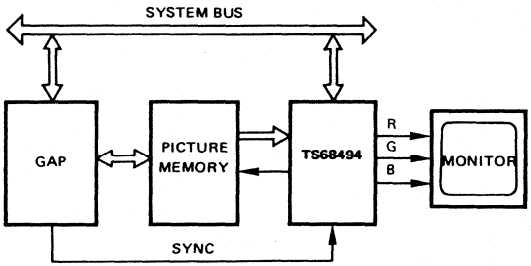
CB-521

PLCC44



PLASTIC PACKAGE

TYPICAL APPLICATION



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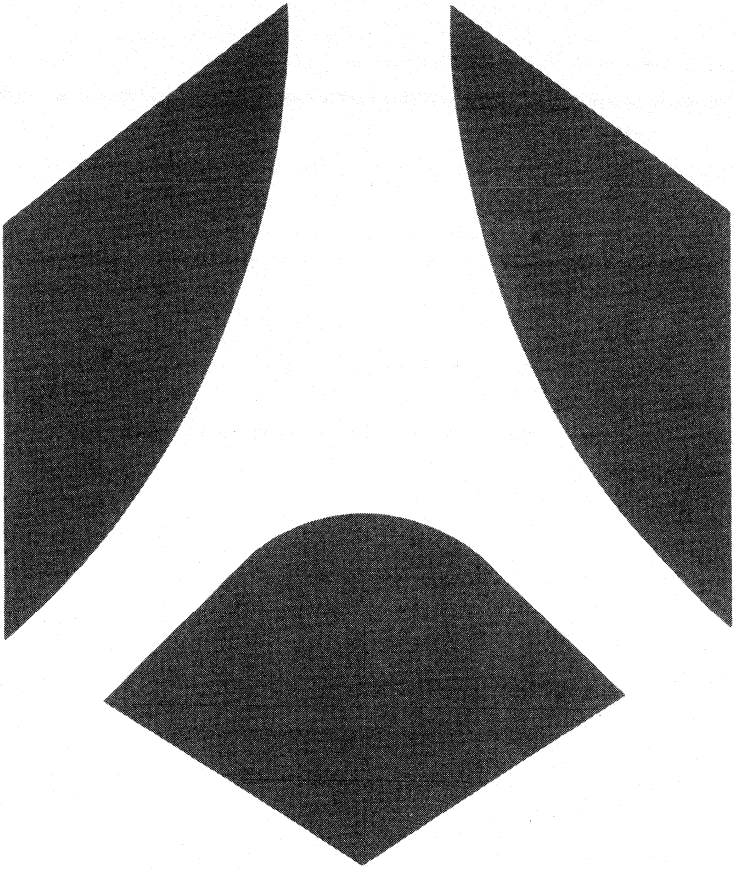
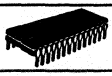


Video converters

VIDEO A/D FLASH CONVERTERS

Part number	Function		Package	Suffix	Page
TS8306	15 MHz - 6 bit Flash A/D converter	DIL16		C, J, P	4-5
TS8307	15 MHz - 7 bit Flash A/D converter	DIL20		C, J, P	4-11
TS8308	Video speed 8 bit Flash A/D converter	DIL24		C, J	4-15
TS8328	Video speed 8 bit Flash A/D converter	DIL28		C, J	4-27

VIDEO D/A CONVERTERS

Part number	Function		Package	Suffix	Page
TS8408	25 MHz 8 bit Voltage output D/A converter	DIL16		C, J	4-33
TS8428	5 MHz - 8 bit Voltage output D/A converter	DIL16		J, P	4-41

THOMSON COMPONENTS SEMICONDUCTEURS

TS8306

15 MHz 6 BIT FLASH A/D CONVERTER

PRODUCT PREVIEW

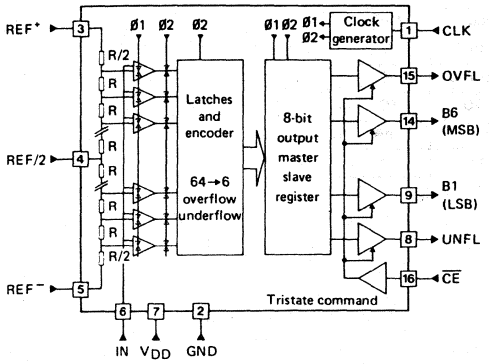
The TS8306 is a monolithic 6-bit HMOS2 parallel (flash) A/D converter designed for video conversion.
Parallel sampling is performed via a resistor ladder and 64 auto-balanced comparators. Conversion is accomplished within one clock pulse.

A very low input capacitance (less than 15 pF) and a low input dynamic range (1 volt possible) allow very easy drive of the TS8306.

- 15 MHz sampling rate.
- 5 MHz input bandwidth without sample and hold.
- Accuracy better than 6 mV (operation at low reference possible).
- Single +5V supply.
- Logic inputs and outputs are TTL and CMOS compatible.
- 6 bit data, underflow and overflow lines are 3-state outputs.
- 16 pin package (chip also available).
- Very low cost device.
- Soon available in SO16 plastic micropackage.

- High speed data acquisition.
- TV video digitizing.
- Radar pulse analysis.
- Medical imaging.
- General purpose hybrid ADC's.
- Optical recognition.
- Fax machine and video printer.
- All high speed A/D conversion applications where low power and low cost are required.

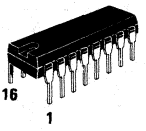
BLOCK DIAGRAM



HMOS2

15 MHz
6-BIT FLASH
A/D CONVERTER

CASE CB-79

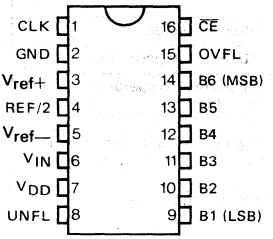


P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

C SUFFIX	J SUFFIX
CERAMIC PACKAGE	CERDIP PACKAGE

PIN ASSIGNMENT



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PIN DESCRIPTION

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
CLK	I	1	Clock input	TTL level accepted
GND	I	2	General ground	Inside, analog and digital ground are separated.
V_{ref+}	I	3	Upper reference	Access to the upper resistance ladder
REF/2	I	4	Middle reference	Access to the middle resistance ladder. The conversion law can be changed by forcing this point by an external voltage source.
V_{ref-}	I	5	Lower reference	Access to the lower resistance ladder.
V_{IN}	I	6	Analog input	
V_{DD}	I	7	Positive supply	Inside, analog and digital supply are separated.
UNFL	O	8	Under flow status line	This line is set to logical "1" when the input signal is lower than the V_{ref^-} voltage. All data (B1 to B6) are reset to logical "0".
B1 (LSB) to B6 (MSB)	O	9 to 14	Output data	
OVFL	O	15	Overflow status line	This line is set to logical "1" when the input signal is higher than the V_{ref^+} voltage ; all data (B1 to B6 are set to logical "1".
$\overline{CE}$	I	16	Tristate enable	$\overline{CE}$ commands the tristate mode for all output buffers (B1 to B6, OVFL and UNFL). When $\overline{CE}$ = "1" : tristate $\overline{CE}$ = "0" : output valid

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage (1)	V_{DD}	- 0.3 to 7	V
Storage temperature	T_{stg}	- 55 to 150	°C
Operating temperature	T_{oper}	0 to 70	°C
Power supply current	I_{GND}, IV_{DD}	150	mA
Digital and analog inputs (1)	V_{in}	- 0.3 to 7	V

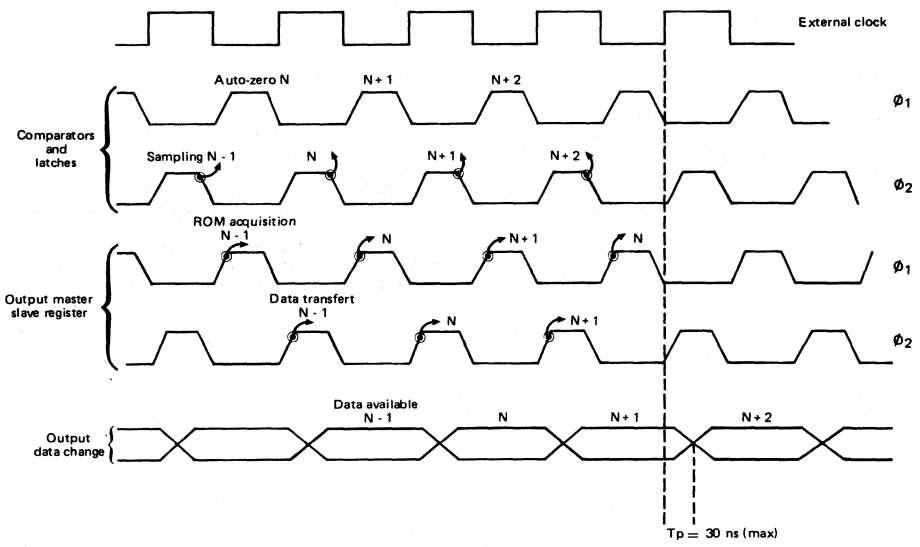
Note: (1) With respect to GND

ELECTRICAL OPERATING CHARACTERISTICS

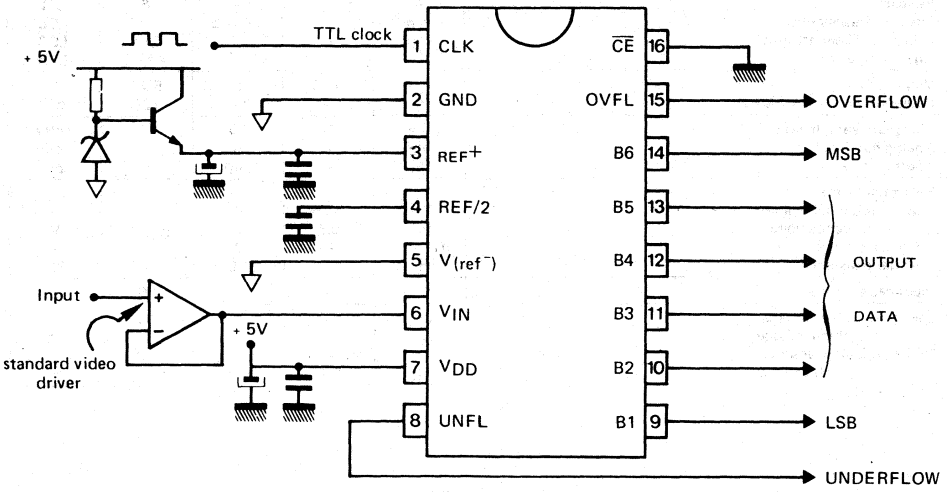
T_{amb} = +25 °C, V_{DD} = + 5 V, V_{REF+} = + 2 V, V_{REF-} = 0V

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	N	–	–	6	BIT
Integral linearity error	I_{LE}	–	± 1/2	–	LSB
Differential linearity error	D_{LE}	–	–	1/4	LSB
Quantizing error	Q_E	– 1/2	–	+ 1/2	LSB
Voltage supply	V_{DD}	4.75	5	5.25	V
Power dissipation (15 MHz)	P_D	–	–	120	mW
Maximum sample rate	F_S	–	15	–	MHz
Analog bandwith	F_C	–	5	–	MHz
Aperture jitter	t_a	–	250	–	pS
Reference ladder:					
lower reference voltage	ref-	– 0.5	0	–	V
upper reference voltage	ref_+	0.8	2	V_{DD} – 1.5	V
full scale range	$ref_+ - ref_-$	–	2	–	–
ladder resistance	R_L	–	1.5	–	kΩ
Input capacitence	C_{in}	–	–	15	pF
Logic output low voltage	V_{OL}	–	–	0.4	V
high voltage	V_{OH}	2.4	–	–	V
Digital input low voltage	V_{IH}	–	–	0.8	V
high voltage	V_{IL}	2.4	–	–	V

TIMING DIAGRAM



TYPICAL CONFIGURATION



Conventions

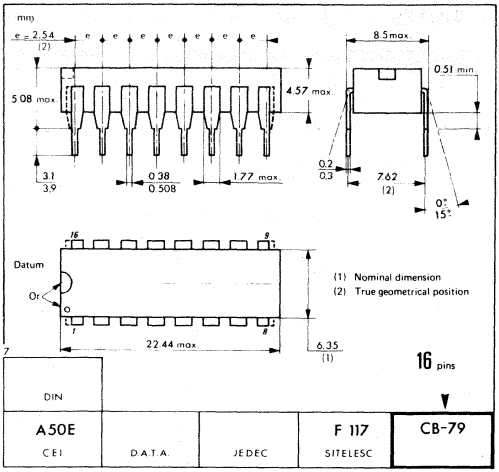
- = Incoming ground pin
- = Ground plane connected to the incoming ground pin

Caution for use

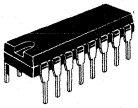
- = 22 µF tantalum capacitors (as near as possible to the incoming ground pin)
- = 100 nF ceramic capacitors (as near as possible to the device pin)

- Avoid DC current flows in the ground plane
- Try to respect star connections for high DC current flows (connection to the incoming pin)

PHYSICAL DIMENSIONS



CB-79

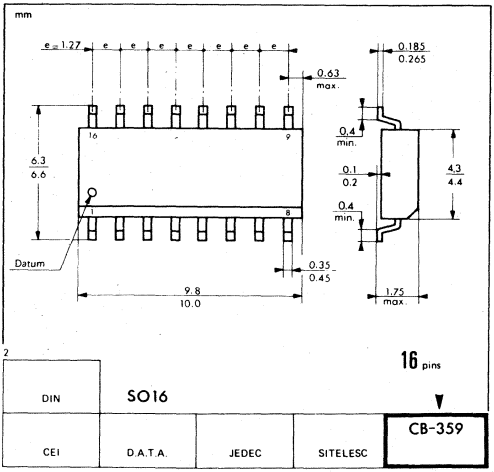


P SUFFIX
PLASTIC PACKAGE

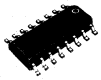
ALSO AVAILABLE

C SUFFIX
CERAMIC PACKAGE

J SUFFIX
CERDIP PACKAGE



CB-359



FP SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

TS8307

15 MHz 7 BIT FLASH A/D CONVERTER

PRODUCT PREVIEW

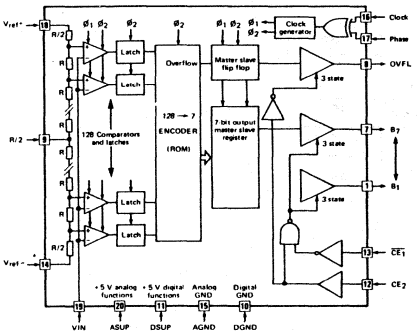
The TS8307 is a monolithic 7-bit HMOS2 parallel (flash) A/D converter designed for video conversion.
Parallel sampling is performed via a resistor ladder and 128 auto-balanced high speed and high accuracy comparators. Conversion is accomplished within one clock pulse.
A very low input capacitance (less than 20 pF) and a low input dynamic range (1 V possible) allow a very easy drive of the TS8307.
Typical characteristics:

- 15 MHz sampling rate.
- 5 MHz input bandwidth without sample and hold.
- Accuracy better than 6 mV.
- Single +5 V supply.
- Logic inputs and outputs are TTL compatible.
- 7-bit data and overflow lines are 3-state outputs.
- Serie operation (2 x 8307) to obtain a 8-bit flash converter (by using overflow and $\overline{CE1}$ and CE2).
- Parallel operation (2 x 8307) to obtain a 30 MHz 7-bit converter (by using Phase and CE2).
- 20-pin slim package.
- Very low cost device.
- ± 1 LSB integral non linearity.
- ± 0.5 LSB differential non linerarity.

Typical applications:

- High speed data acquisition, and instrumentation.
- TV video digitizing.
- Radar pulse analysis.
- Medical and industrial imaging.
- Optical recognition.
- Fax machine and video printer.
- All high speed A/D conversion applications where low power and low cost are required.

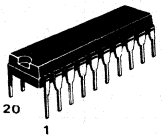
BLOCK DIAGRAM



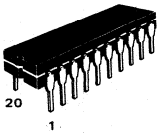
HMOS2

15 MHz 7-bit FLASH A/D CONVERTER

CASE CB-194



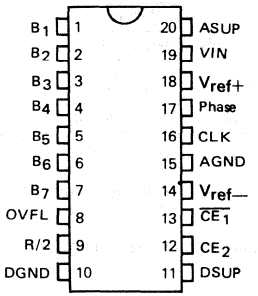
P SUFFIX
PLASTIC PACKAGE



J SUFFIX
CERDIP PACKAGE

Ceramic package (C Suffix) is also available.

PIN ASSIGNMENT



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PIN DESCRIPTION

Name	Pin Type	N°	Function	Description
B_1 (LSB) to B_7 (MSB)	O	1 to 7	Output data	Tristate buffer outputs
OVFL	O	8	Overflow status line	Set to «1» when the input signal is higher than V_{ref+} voltage. All data (B_1 to B_7) are set to «1»
R/2	I	9	Half reference	Access to the half reference voltage. The conversion low can be changed by forcing this point by an external voltage source.
DGND	I	10	Digital ground	
DSUP	I	11	Digital supply	
CE_2	I	12	Tristate command	CE_2 - «0»: tristate for both overflow status and data lines
$\overline{CE_1}$	I	13	Tristane command	CE_2 - «1»: overflow valid but data lines valid only if $\overline{CE_1}$ - «0»
V_{ref-}	I	14	Lower reference	Access to the lower reference voltage. A voltage source must be applied (or ground)
AGND	I	15	Analog ground	
CLK	I	16	Clock input	TTL levels
Phase	I	17	Phase input	When Phase is «0» the input signal is sampled on the falling edge of the input clock. When Phase is «1» the input signal is sampled on the rising edge of the input dock
V_{ref+}	I	18	Upper reference	Access to the upper reference voltage. A voltage source must be applied
VIN	I	19	Analog input	
ASUP	I	20	Analog supply	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltages (1) (1)	DSUP ASUP	- 0.3 to 7 - 0.3 to 7	V
Storage temperature	T_{stg}	- 55 to 150	°C
Operating temperature	T_{oper}	0 to 70	°C
Power supply current	I_{DSUP}, I_{ASUP} I_{DGND}, I_{AGND}	150	mA
Digital and analog inputs (1)	V_{in}	- 0.3 to 7	V

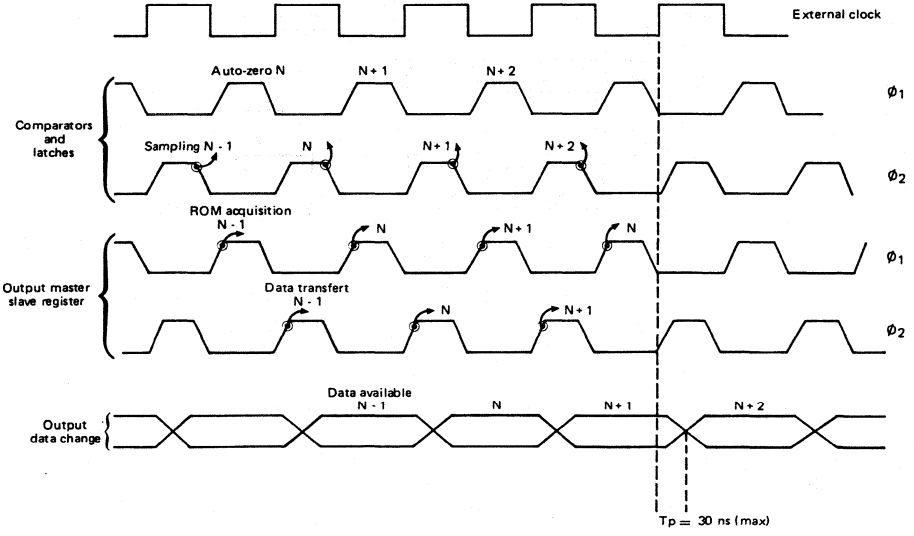
Note: (1) With respect to AGND = DGND

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25°C
ASUP = DSUP = +5 V V_{ref+} = +2 V V_{ref-} = 0 V AGND = DGND = 0 V

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	N	–	–	7	BITS
Linearity error	I_{LE}	–	± 1	–	LSB
Differential linearity error	D_{LE}	–	± 1/2	–	LSB
Quantiting error	Q_E	– 1/2	–	– 1/2	LSB
Voltage supply	ASUP, DSUP	4.75	5	5.25	V
Power dissipation (15 MHz)	P_D	–	–	250	mW
Maximum sample rate	F_S	15	–	20	MSPS
Analog bandwith	F_C	–	5	–	MHz
Aperture jitter	t_a	–	250	–	pS
Preference ladder:					
Lower reference voltage	V_{ref-}	– 0.5	0	–	V
Upper reference voltage	V_{ref+}	1	2	V_{DD} – 1.5	V
Full scale range	$V_{ref+} - V_{ref-}$	1.5	2	V_{DD} – 1.5	V
Ladder resistance	R_{ref}	250	350	450	Ω
Input capacitence	C_{IN}	–	–	20	pF
Logic output low voltage	V_{OL}	–	–	0.4	V
high voltage	V_{OH}	2.4	–	–	V
Digital input low voltage	V_{IH}	–	–	0.8	V
high voltage	V_{IL}	2.4	–	–	V

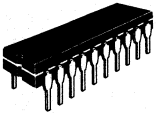
TIMING DIAGRAM (PHASE = «0»)



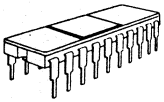
Note: If Phase is set to «1» the external clock is inverted inside the circuit.

PHYSICAL DIMENSIONS

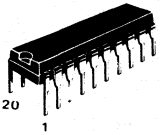
CB-194



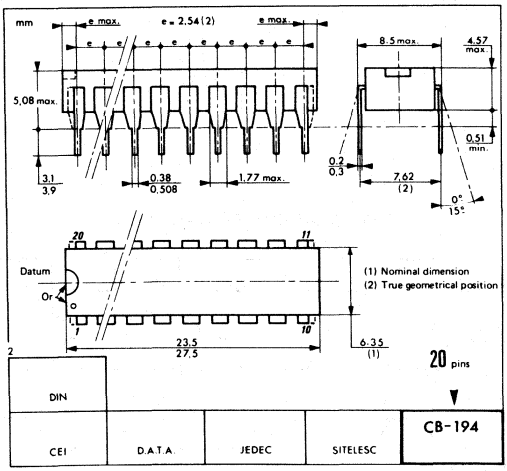
J SUFFIX
CERDIP PACKAGE



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



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THOMSON COMPONENTS SEMICONDUCTEURS

TS8308

VIDEO SPEED 8 BIT FLASH A/D CONVERTER

ADVANCE INFORMATION

The TS8308 is a monolithic 8-bit HMOS2 parallel (flash) A/D converter designed for high speed conversion.
Parallel sampling is performed via resistor ladder and 256 comparators.
Conversion is accomplished within one pulse.
A very low input capacitance (less than 30 pF) and a low input dynamic range (1 V possible) allow a very easy drive of the TS8308.

Typical characteristics:

- Single +5 V supply.
- ±0.5 LSB differential non linearity.
- 15 MHz sampling rate.
- 5 MHz input signal without sample and hold adjunction.
- Very low input capacitance (max. 30 pF).
- All logic inputs and outputs are TTL compatible.
- Data output: 8-bit binary code + overflow.
- Output buffers for 8-bit data and overflow are 3-state type.
- Accuracy better than 6 mV.
- Pin to pin compatible with RCA CA 3308.

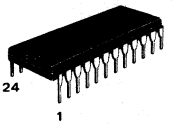
Typical applications:

- TV video digitizing.
- Ultrasound signature analysis.
- Transient signal analysis.
- Radar pulse analysis.
- High energy physics research.
- High speed oscilloscope storage/display.
- General purpose hybrid ADCs.
- Optical character recognition.
- Digital signal processor data acquisition systems.
- Satellite operations.
- Portable video speed products.
- Video printer.
- Fax machine.
- Image processing.
- Medical imaging.
- All high speed A/D conversion applications where low power and low cost are required.

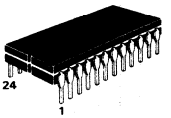
HMOS2

VIDEO SPEED 8-BIT FLASH A/D CONVERTER

CASE CB-68



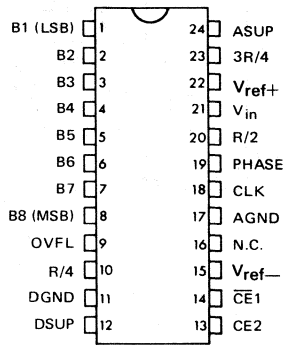
P SUFFIX
PLASTIC PACKAGE



J SUFFIX
CERDIP PACKAGE

Ceramic package (C Suffix) is also available

PIN ASSIGNMENT



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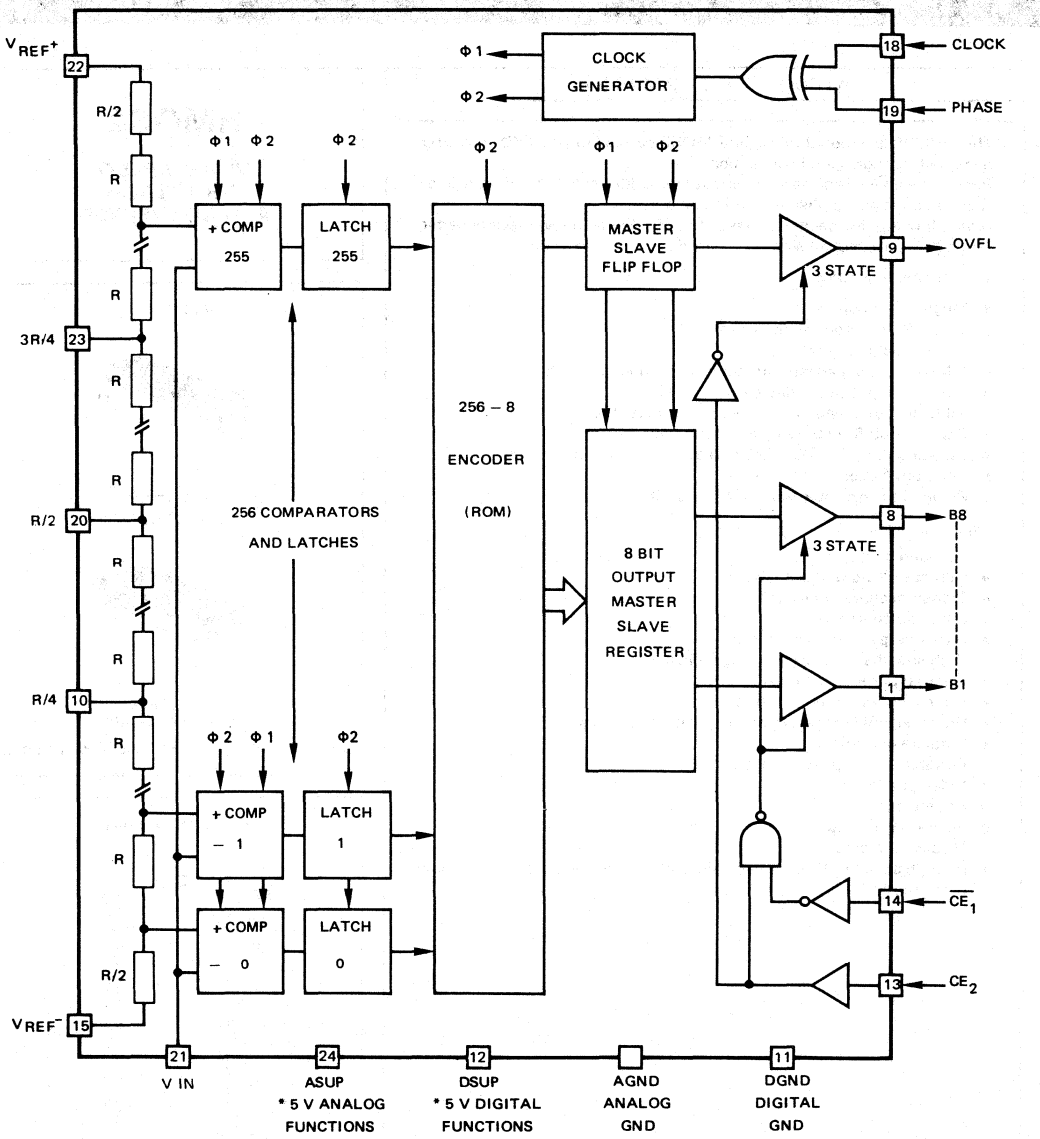
BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Number	Function	Description
B_1 (LSB) to B_8 (MSB)	O	1 to 8	Output data	Tristate buffer outputs
OVFL	O	9	Overflow status line	This line is set to logical "1" when the input signal is higher than the $V_{REF}+$ voltage. All data (B_1 to B_8) are set to logical "1".
R/4	I	10	First quarter reference	Access to the first quarter reference voltage
DGND	I	11	Digital ground	
DSUP	I	12	Digital supply	
CE2	I	13	Tristate command	CE2 = "0" : tristate for both overflow status and data lines
$\overline{CE1}$	I	14	Tristate command	CE2 = "1": overflow valid out data lines valid only if $\overline{CE1}$ = "0".
$V_{REF}-$	I	15	Lower reference	Access to the lower reference voltage. A voltage source must be applied (or ground)
NC		16	Non connected	
AGND	I	17	Analog ground	
CLK	I	18	Clock input	TTL levels
PHASE	I	19	Phase input	When phase is "0" the input signal is sampled on the falling edge of the input clock. When phase is "1" the input signal is sampled on the rising edge of the input clock
R/2	I	20	Half reference	Access to the half reference voltage
V_{IN}	I	21	Analog input	
$V_{REF}+$	I	22	Upper reference	Access to the upper reference voltage. A voltage source must be applied
3 R/4	I	23	Third quarter reference	Access to the third quarter reference voltage
ASUP	I	24	Analog supply	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage (1) (1)	DSUP ASUP	- 0.3 to + 7 - 0.3 to + 7	V V
Storage temperature	T_{stg}	- 55 to 150	°C
Operating temperature	T_{oper}	0 to 70	°C
Power supply current	IDSUP IASUP IDGND IAGND	150	mA
Digital and analog inputs (1)	V_{in}	- 0.3 to + 7	V

Nota: (1) With respect to AGND = DGND

ELECTRICAL OPERATING CHARACTERISTICS

ASUP = DSUP = 5 V, AGND = DGND = 0 V, V_{ref-} = 0 V, V_{ref+} = 3 V, Phase = 1, F_S = 14.8 MHz, F_C = 4 MHz

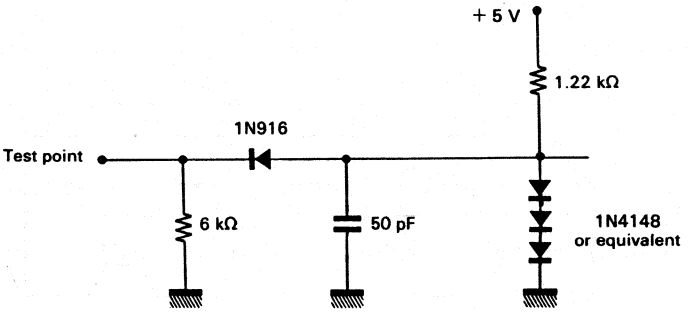
Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	N			8	
Linearity error (Peak to Peak)*	ILE			4	LSB
Differential linearity error	DLE		1/2	0.7	LSB
Quantizing error	QE	— 1/2		+ 1/2	LSB
Aperture time	t_{AP}		250		ps
Voltage supply	ASUP, DSUP	4.75	5	5.25	V
Power dissipation (4 MHz):					
Analog supply	PDA		350	450	mW
Digital supply	PDD		90	150	mW
Maximum sample rate	F_S	15		20	MHz
Analog bandwidth	F_C	3.5	5		MHz
Reference ladder:					
Lower reference voltage	V_{ref-}	0	0		V
Upper reference voltage	V_{ref+}	1	2	ASUP- 1.5	V
Full scale range		1	2	ASUP- 1.5	V
Ladder resistance	V_{ref}	400	550	900	ohm
Input capitance	C_{IN}			30	pF
Logic output low voltage	V_{OL}			0.4	V
high voltage	V_{OH}	2.4			V
Digital input low voltage	V_{IL}			0.8	V
high voltage	V_{IH}	2.4			V
Total harmonic distorsion	HD		— 37	— 34	dB
HF gain	GHF			0.4	dB

* See integral non linearity template

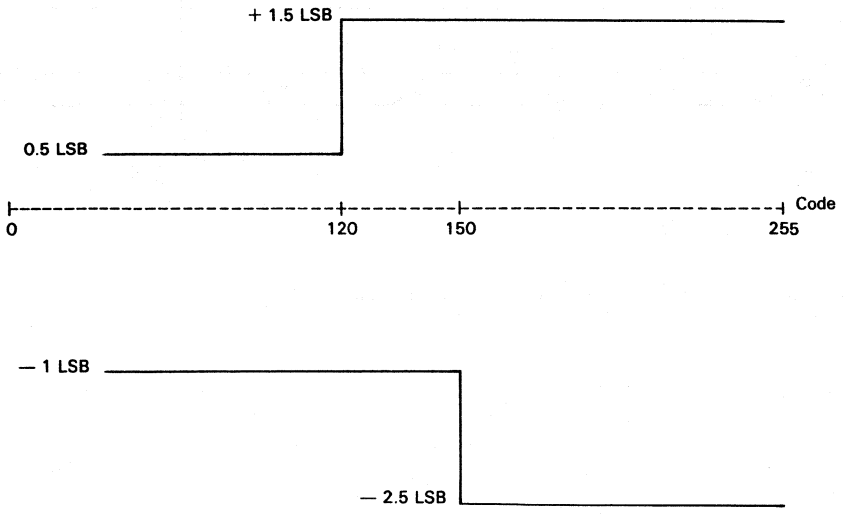
DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Clock pulse width	t_{cl}	25			ns
	t_{ch}	25			ns
Clock rise time	t_{cr}		5		ns
Clock fall time	t_{cf}		5		ns
Outputs progag. (1)	t_P		25	40	ns
Outputs transient (1)	t_{THL}			25	ns
	t_{TLH}			25	ns

(1) Note:



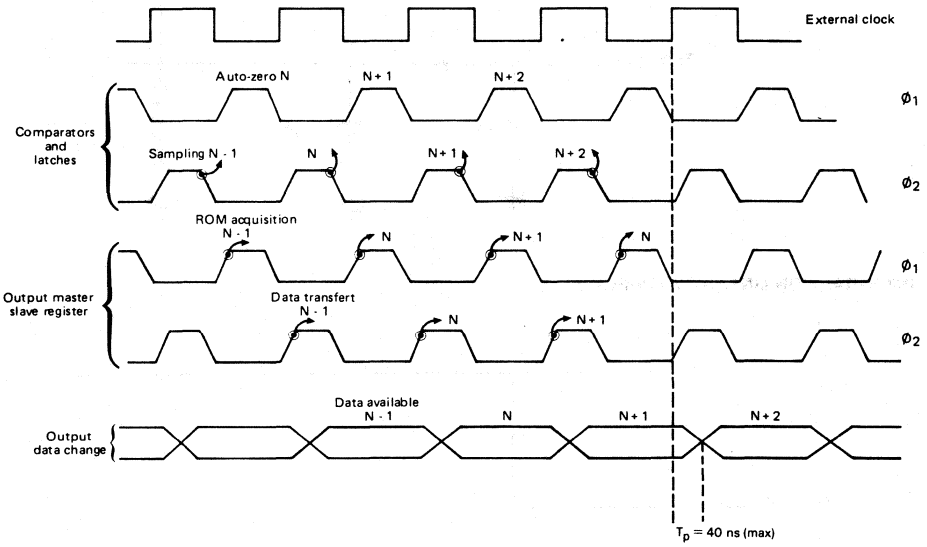
INTEGRAL NON LINEARITY TEMPLATE:



Conditions: 1/4, 1/2 and 3/4 pins free, $F_S = 12.5$ MHz, $F = 3.125$ kHz (slope).

Note: Applying a low impedance DC voltage ($V_{ref+}/2$) on pin R/2 allows to obtain an integral non linearity better than ± 1 LSB from code 0 to 255.

TIMING DIAGRAM (PHASE = " O ")



NB : If phase is set to "1", the external clock is inverted inside the circuit

FUNCTIONAL DESCRIPTION

Circuit TS8308 includes:

- a sequencer generating internal clock,
- a core ensuring conversion,
- an output circuit delivering digital data,
- the sequencer generates 6 internal clocks from pins CLK and PHASE:

Internal phases	Circuits concerned	Function	Value (PHASE = 0)
Φ 1	Comparators	Autozero	$\overline{CLK}$
Φ 2	Comparators	Sampling and comparison	CLK
Φ 3	Latches	Storage	Φ 2 + D
Φ 4	Encoder	Transmission	Φ2 + D
Φ 5	Output master/slave flip - flop	Sampling	Φ 1 + D
Φ 6	Output master/slave flip - flop	Storage	Φ 2 + D

N.B.: D is a time-delay introduced to compensate the signal propagation.

- the core includes:
  - — A resistor linear network delivering 256 reference voltages distributed linearly between external reference voltages V_{ref+} and V_{ref-}. Access to quarter (R/4), half (R/2) and three quarter (3R/4) bridges enable the following:
    - either improve linearity by externally forcing reference voltages,
    - filter disturbances going through the bridge by means of external capacitors,
    - or delinearize the bridge by means of external resistors (law of linear compression by blocks).
  - — A set of 256 voltage comparators parallel connected across the 256 taps of the reference bridge and the input analog signal which defines the 256 (2^8) quantification levels.
    In first phase Φ1, these comparators store their flip-flop threshold then, in phase Φ2 they compare the thresholds with the input signal.
    The comparators with an input signal voltage lower than the reference voltage present a given state at the output, the others present the complementary state.
    The 256 comparators output is stored in 256 latches at the end of phase Φ3 = Φ2.
  - — A 256 to 8 decoder detecting the transition between the comparators in a given state and the ones in the complementary state.
    The line enabled corresponds to the last comparator which has tripped, i.e. the comparator with the reference voltage nearest by default to the input signal.
  - — A ROM following the decoder and coding over 8 bits the detected comparison chain in binary.
    If the input signal is lower than the lowest reference voltage (1st comparator), code 0 is written at the output.
    If the input signal is higher than the upper most reference voltage (256th comparator), code 255 is written at the output and overflow bit is set to 1.
- The output stage consists of 9 identical parts (8 bits and overflow) each formed of a flip-flop D connected to the ROM output with an output buffer. This buffer is enabled on phase Φ6 = Φ2 and includes a selective high impedance command.
  Inputs $\overline{CE1}$ and CE2 switch the output bits to this 3rd state (with overflow bit if required) in order to facilitate the following*:
  - — parallel connection of the 2 converters thus providing a double sampling frequency while maintaining an 8 bit resolution,
  - — series connection of the 2 converters providing a 9 bit resolution while maintaining a 20 MHz sampling frequency.

$\overline{CE1}$	CE2	B1,...B8 in 3rd state	B9 (OVFL) in 3rd state
0	0	Yes	Yes
0	1	No	No
1	0	Yes	Yes
1	1	Yes	No

* See application information.

TYPICAL EVALUATION CIRCUIT *

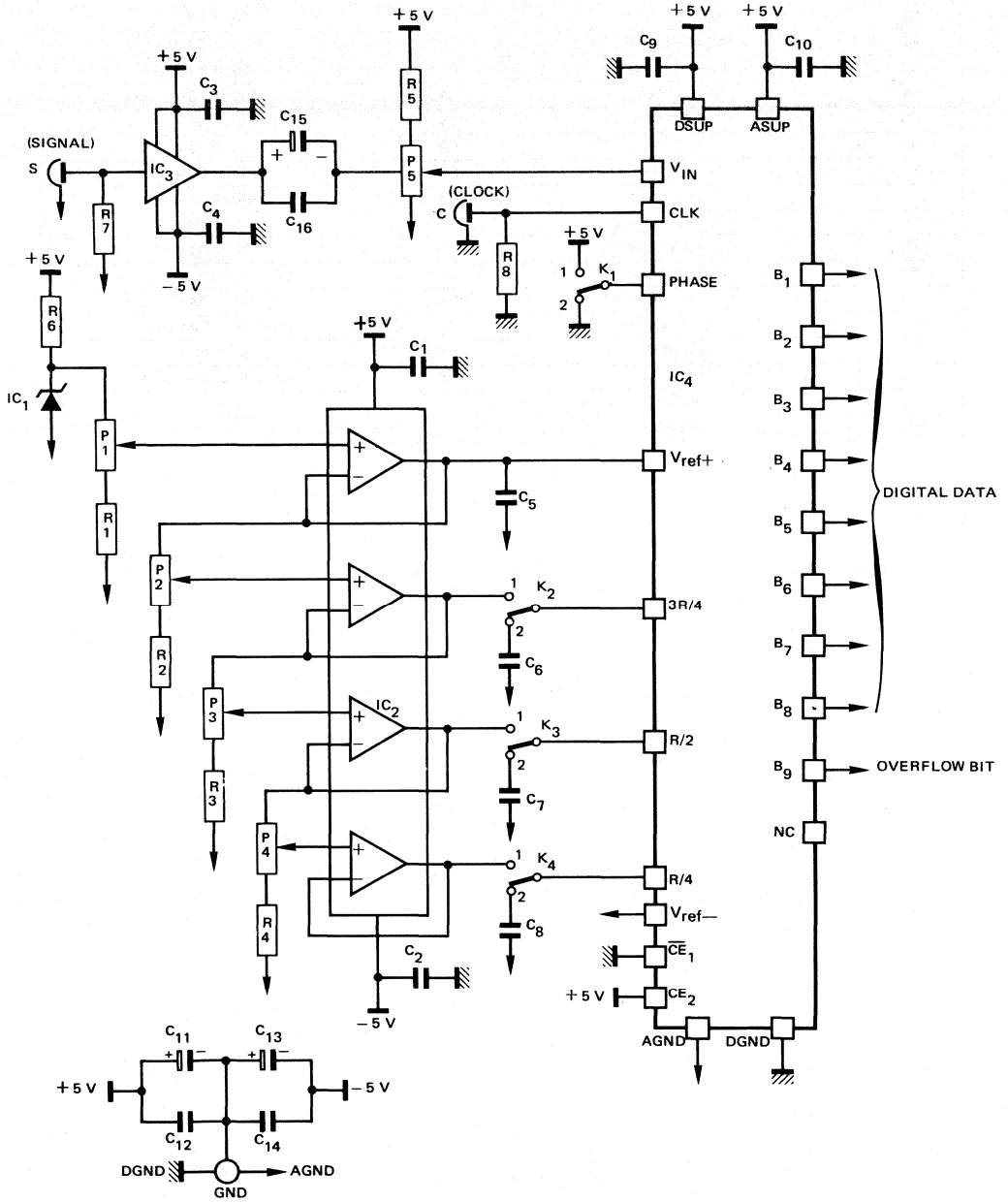
The general circuit used for the flash converter in typical conditions (8 bits, 20 MHz) is represented on figure 1.

- Voltage reference.
  Flash converter requiring a positive reference voltage (V_{ref+}) ranging from 1.5 V to 3 V (typ: 2 V), the circuit generates a reference voltage of 2.5 V from the power supply voltage (+5 V) and a precision regulation diode (IC_1).
- Resistor bridge reference voltages.
  The circuit allows to access some particular points on the resistor bridge. These points correspond to 3/4, 1/2 and 1/4 of the bridge total resistance. This feature enables use of the flash convertor in two ways:
  - — in linear operation with these 3 points grounded by uncoupling capacitors in order to filter disturbances along the bridge (K2, K3 and K4 in position 2),
  - — in non-linear operation with the following 2 functions:
    - improvement in flash converter integral linearity by forcing the 3 points to their corresponding voltages (K2, K3 and K4 on poisition 1),
    - implementation of a non-linear conversion law (compression law for instance) in order to better observe the results of the conversion on one part only of the transfer characteristic (K2, K3, K4 on position 1).
- Analog signal.
  The input analog signal must be driven by a wide band buffer amplifier (IC_3) with a very low output impedance.

  In order to eliminate the almost uncontrollable offsets introduced by the source generator or buffer amplifier proper, two capacitors parallel mounted (C_{15} and C_{16}) are added in series after the amplifier.
  For low frequencies (< 1MHz) tantalum capacitor (C_{15}) is used as a short-circuit; for higher frequencies (> 1 MHz) the ceramic capacitor (C_{16}) is used as a short-circuit.
  After these capacitors, a potentiometer (P5) with the middle point connected to the flash converter input adds a DC component to the input signal. The signal thus obtained has an overage value different from zero, lying between V_{ref-} and V_{ref+} and which can be converted by the flash converter.
- Clock signal.
  Clock signals are TTL or CMOS signals. The PHASE command is used to invert (K_1 on position 1) or not (K_1 on position 2) the external signal.
- Considerations on electrical layout.
  A certain number of elementary precautions should be taken in the electrical layout when using high frequencies.
  The main ones are as follows:
  - — a ground plane for the components,
  - — the ground tracks corresponding to the various signals (clock, input signal, references) are separated and connected together to a single point,
  - — a star distributed power supplies (idem for ground) to avoid any possible loop,
  - — a maximum capacitive uncoupling as close as possible to each circuit.

* For typical application circuit, the same surroundings can be used.

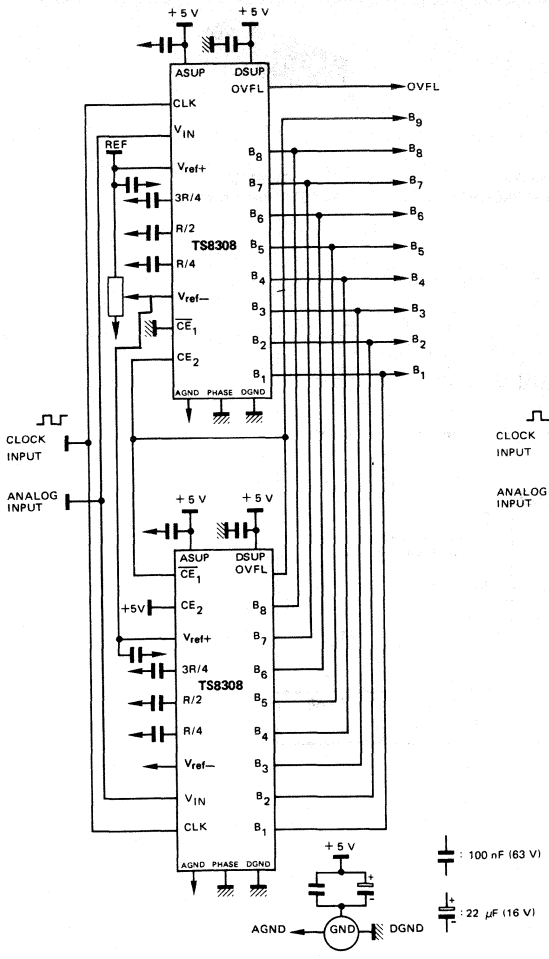
TYPICAL EVALUATION CIRCUIT
(continued)



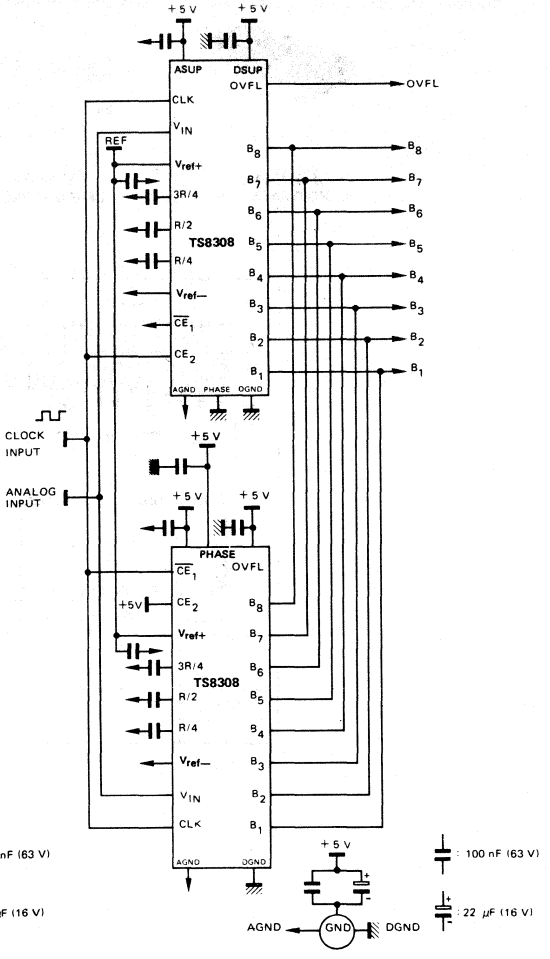
8 BIT RESOLUTION CONFIGURATION 20 MHZ SAMPLING RATE

Component	Value	Component	Value
R1	5.6 KΩ (1/4 W)	C1	100 nF 63 V
R2	3.3 KΩ (1/4 W)	C2	100 nF 63 V
R3	1.2 KΩ (1/4 W)	C3	100 nF 63 V
R4	560 Ω (1/4 W)	C4	100 nF 63 V
R5	10 KΩ (1/4 W)	C5	100 nF 63 V
R6	2 KΩ (1/4 W)	C6	100 nF 63 V
R7	47Ω (1/4 W)	C7	100 nF 63 V
R8	47 Ω (1/4 W)	C8	100 nF 63 V
P1	10 KΩ (multiturns)	C9	100 nF 63 V
P2	10 KΩ (multiturns)	C10	100 nF 63 V
P3	10 KΩ (multiturns)	C11	22 µF 16 V (Tantalum)
P4	10 KΩ (multiturns)	C12	100 nF 63 V
P5	10 KΩ (multiturns)	C13	22 µF 16 V (Tantalum)
IC1	TDB 0136	C14	100 nF 63 V
IC2	TDB 0084	C15	68 µF 16 V (Tantalum)
IC3	LH 0002	C16	100 nF 63 V
IC4	TS 8308		

TYPICAL APPLICATION



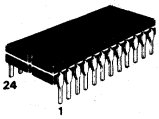
TYPICAL TS8308 9 BIT RESOLUTION CONFIGURATION
20 MHz SAMPLING RATE



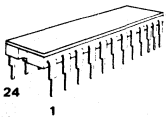
TYPICAL TS8308 8 BIT RESOLUTION CONFIGURATION
40 MHz SAMPLING RATE

PHYSICAL DIMENSIONS

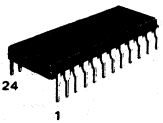
CB-68



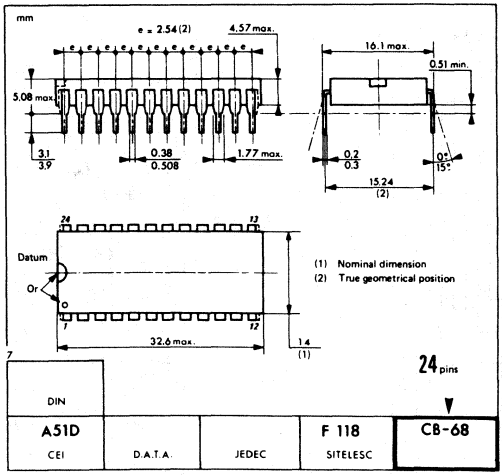
J SUFFIX
CERDIP PACKAGE



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



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THOMSON COMPONENTS SEMICONDUCTEURS

TS8328

VIDEO SPEED 8 BIT FLASH A/D CONVERTER

ADVANCE INFORMATION

The TS8328 is the minimal configuration (20 pins) of the TS8308 (24 pins) full flash ADC.
This monolithic parallel A/D converter is designed for high speed conversion. Sampling is performed via a resistor ladder and 256 autobalanced high speed and high accuracy comparators. Conversion is accomplished within one clock pulse.
A very low input capacitance (less than 25 pF) and a low input dynamic range (1 V possible) allow a very easy drive of the TS8328.

Typical characteristics:

- Single +5 V supply.
- ±0.5 LSB differential non linearity.
- 15 MHz sampling rate.
- 5 MHz input signal without sample and hold adjunction.
- Very low input capacitance (max 25 pF).
- All logic inputs and outputs are TTL compatible.
- Data output: 8-bit binary code.
- Output buffers for 8-bit data are 3-state type.
- Accuracy better than 6 mV.
- 20 pins slim line package (0.3 inch).

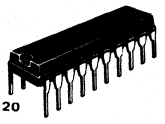
Typical applications:

- Pulse coding for high energy physics experiments.
- High speed data acquisition and instrumentation.
- TV and video digitizing.
- Radar pulse coding.
- Medical and industrial imaging.
- Optical recognition.
- All high speed A/D conversion applications where low power and low cost are required.

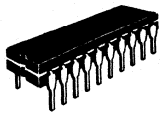
HMOS2

VIDEO SPEED 8 BIT FLASH ADC

CASE CB-194



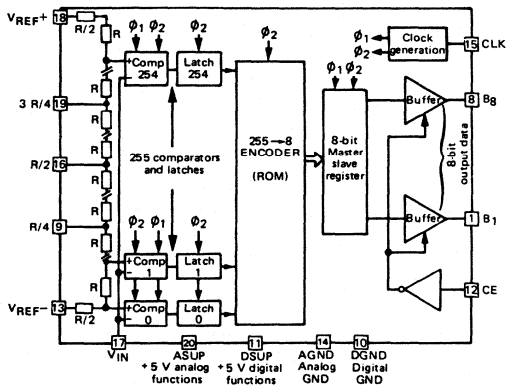
P SUFFIX
PLASTIC PACKAGE



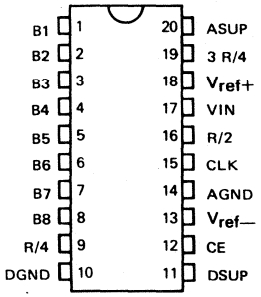
J SUFFIX
CERDIP PACKAGE

* Ceramic package (C Suffix) is also available.

BLOCK DIAGRAM



PIN ASSIGNMENT



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PIN DESCRIPTION

Name	Type	N°	Function	Description
B_1 (LSB) to B_8 (MSB)	O (MSB)	1 to 8	Output data	Tristate buffer outputs
R/4	I	9	First quarter reference	Access to the first quarter reference voltage
DGND	I	10	Digital ground	
DSUP	I	11	Digital supply	
CE	I	12	Tristate command	Commands the 3 state mode for data lines CE = "0" : 3 state CE = "1" : data valid
V_{ref-}	I	13	Lower reference	Access to the lower reference voltage. A voltage source must be applied (or ground).
AGND	I	14	Analog ground	
CLK	I	15	Clock input	The input signal is sampled on the falling edge of the clock. Output data are changing on the next rising edge.
R/2	I	16	Half reference	Access to the half reference voltage.
VIN	I	17	Signal input	
V_{ref+}	I	18	Upper reference	Access to the upper reference voltage. A voltage source must be applied.
3 R/4	I	19	Third quarter reference	Access to the third quarter reference voltage.
ASUP	I	20	Analog supply	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage (1) (1)	DSUP ASUP	- 0.3 to + 7 - 0.3 to + 7	V V
Storage temperature	T_{stg}	- 55 to + 150	°C
Operating temperature	T_{oper}	0 to + 70	°C
Power supply current	IDSUP IASUP IDGND IAGND	150	mA
Digital and analog inputs (1)	V_{in}	- 0.3 to + 7	V

Note: (1) With respect to AGND = DGND

ELECTRICAL OPERATING CHARACTERISTICS

ASUP = DSUP = 5 V, AGND = DGND = 0 V, V_{ref-} = 0 V, V_{ref+} = 3 V, Phase = 1, F_S = 14,8 MHz, F_C = 4 MHz

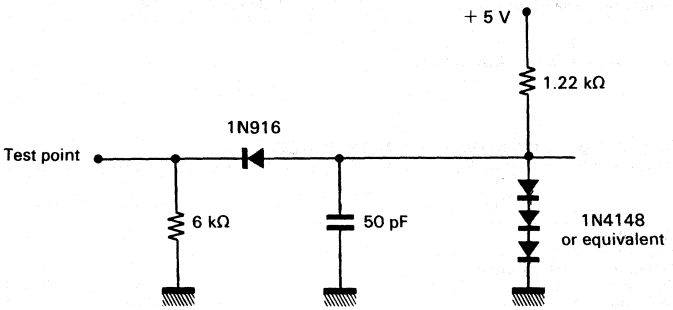
Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	N	–	–	8	
Linearity error (Peak to Peak)*	ILE	–	–	4	LSB
Differential linearity error	DLE	–	1/2	0.7	LSB
Quantizing error	QE	— 1/2	–	+ 1/2	LSB
Apperture time	t_{AP}	–	250	–	ps
Voltage supply	ASUP, DSUP	4.75	5	5.25	V
Power dissipation (4 MHz):					
Analog supply	PDA	–	350	450	mW
Digital supply	PDD	–	90	150	mW
Maximum sample rate	F_S	15	–	20	MHz
Analog bandwidth	F_C	3.5	5	–	MHz
Reference ladder:					
Lower reference voltage	V_{ref-}	0	0	–	V
Upper reference voltage	V_{ref+}	1	2	ASUP-1.5	V
Full scale range		1	2	ASUP-1.5	V
Ladder resistance	R_{ref}	400	550	900	ohm
Input capitance	C_{IN}	–	–	30	pF
Logic output low voltage	V_{OL}	–	–	0.4	V
high voltage	V_{OH}	2.4	–	–	V
Digital input low voltage	V_{IL}	–	–	0.8	V
high voltage	V_{IH}	2.4	–	–	V
Total harmonic distorsion	HD	–	— 37	— 34	dB
HF gain	GHF	–	–	0.4	dB

* See integral non linearity template

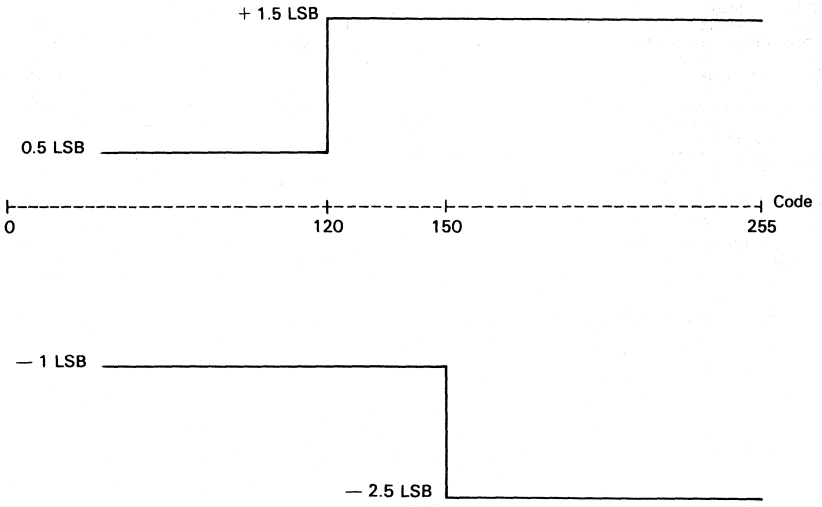
DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Clock pulse width	t_{cl}	25	–	–	ns
	t_{ch}	25	–	–	ns
Clock rise time	t_{cr}	–	5	–	ns
Clock fall time	t_{cf}	–	5	–	ns
Outputs progag. (1)	t_P	–	25	40	ns
Outputs transient (1)	t_{THL}	–	–	25	ns
	t_{TLH}	–	–	25	ns

(1) Note:



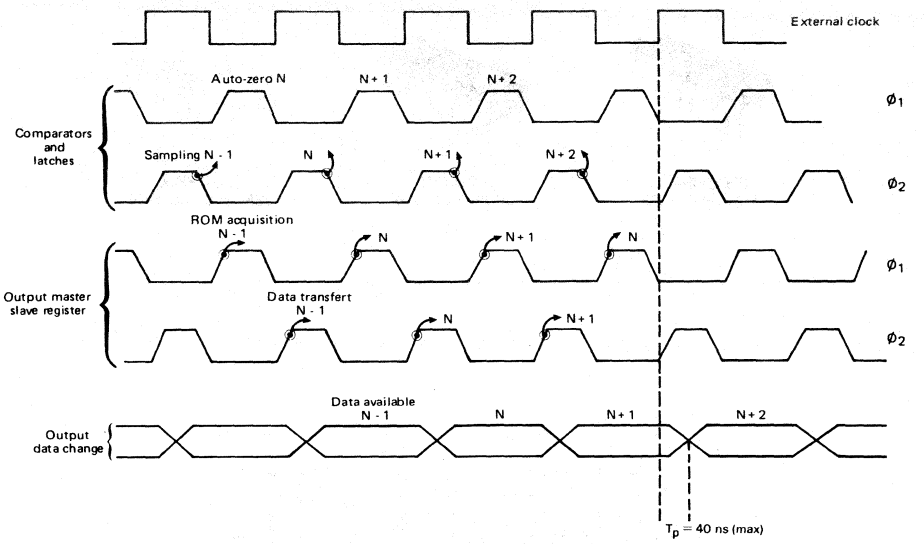
INTEGRAL NON LINEARITY TEMPLATE:



Conditions: 1/4, 1/2 and 3/4 pins free, F_S = 12,5 MHz, F = 3,125 kHz (slope).

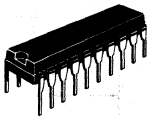
Note: Applying a low impedance DC voltage (V_{ref+}/ 2) on pin R/2 allows to obtain an integral non linearity better than ± 1 LSB from code 0 to 255.

TIMING DIAGRAM

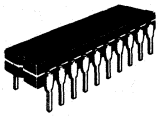


PHYSICAL DIMENSIONS

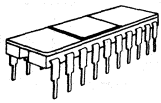
CB-194



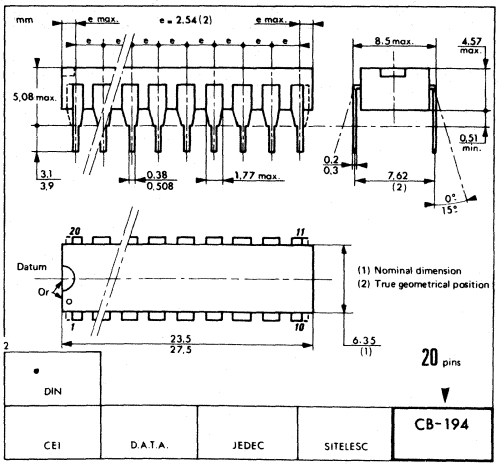
P SUFFIX
PLASTIC PACKAGE



J SUFFIX
CERDIP PACKAGE



C SUFFIX
CERAMIC PACKAGE



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Printed in France

TS8408

25 MHz 8 BIT VOLTAGE OUTPUT D/A CONVERTER

ADVANCE INFORMATION

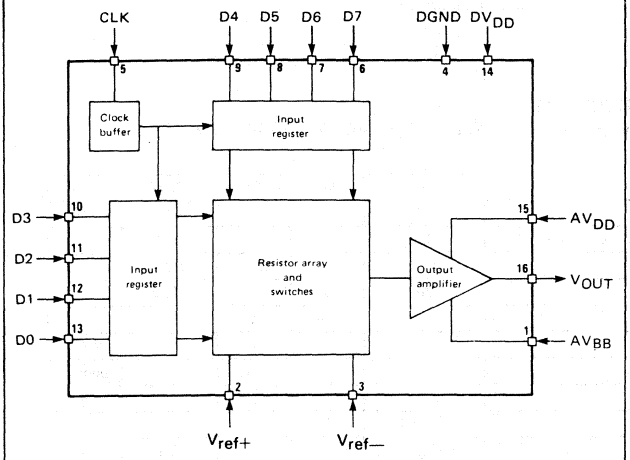
The TS8408 circuit is an 8-bit monolithic digital to analog converter incorporating latches for the logic inputs, designed for 25 MHz conversion rate.
Implemented in HMOS2 technology the circuit contains an on-chip output amplifier, allowing loads as low as 75 Ω, while the full scale setting time within 1/2 LSB is only 35 ns. The circuit is supplied between +5 V and —3 V. This converter offers an inherent monotonicity due to the structure and an integral linearity of 0.6 LSB.

- Differential linearity: ±1/4 LSB error maximum.
- Integral linearity error: 0.6 LSB typ.
- Fast settling time: 35 ns typ.
- Digital inputs are TTL and CMOS compatible.
- No external output amplifier required.
- Loads: 75 Ω min. 25 pF max.
- 16-pin DIL package.

Typical applications:

- TV video digitizing.
- Analog function generator.
  All high speed D/A conversion applications where low power and low cost are required.

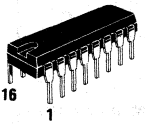
BLOCK DIAGRAM



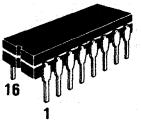
HMOS2

25 MHz
8-BIT VOLTAGE OUTPUT
D/A CONVERTER

CASE CB-79



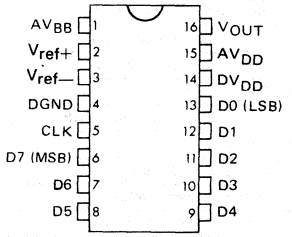
P SUFFIX
PLASTIC PACKAGE



J SUFFIX
CERDIP PACKAGE

Ceramic package (C Suffix) is also available.

PIN ASSIGNMENT



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PIN DESCRIPTION

Name	Type	Number	Function	Description
AV_{BB}	I	1	Negative analog supply	Supply for output video amplifier only
V_{ref+}	I	2	Upper reference	Access to the upper reference voltage. A voltage source must be applied
V_{ref-}	I	3	Lower reference	Access to the lower reference voltage. A voltage source must be applied (or ground)
DGND	I	4	Digital ground	
CLK	I	5	Clock input	TTL levels
D0 (LSB) to D7 (MSB)	I	6 to 13	Digital input	
DV_{DD}	I	14	Digital supply	
AV_{DD}	I	15	Positive analog supply	Supply for output video amplifier only
V_{out}	O	16	Analog output	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltages (1) (1) (1)	DV_{DD} AV_{DD} AV_{BB}	- 0.3 to 6 - 0.3 to 6 - 0.4 to + 0.3	V V V
Storage temperature	T_{stg}	- 55 to 150	°C
Operating temperature	T_{oper}	0 to 70	°C
Power supply current	IDV_{DD} ID_{GND} IAV_{DD} IAV_{BB}	150	mA
Digital and analog inputs (1)	V_{in}	- 0.3 to 6	V

Note: (1) With respect to DGND

ELECTRICAL OPERATING CHARACTERISTICS

$DV_{DD} = AV_{DD} = +5$ V $AV_{BB} = -3$ V $V_{ref+} = +2$ V $V_{ref-} = 0$ V AGND = DGND = 0 V
$T_{amb} = +25$ °C

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	N	—	—	8	Bit
Integral linearity error. (Given values according to the "best line")	I.L.E.	—	± 0.6	± 1	L.S.B.
Differential linearity error	D.L.E.	—	± 0.1	± 0.25	L.S.B.
Zero code output voltage	V_{IO}	80	150	200	mV
Gain	—	—	0.9	—	—
Zero code output voltage drift	—	—	0.3	—	mV/°C
Gain drift	—	—	100	—	ppm/°C
Differential gain error	—	—	2	—	%
Lower reference voltage	V_{ref-}	0	0	—	V
Upper reference voltage	V_{ref+}	—	2	2.2	V
Full scale range	$V_{ref+} - V_{ref-}$	1	2	2.2	V
Ladder resistance	R_{ref}	1.5	2	2.7	KΩ

ELECTRICAL OPERATING CHARACTERISTICS (CONTINUED)
$DV_{DD} = AV_{DD} = +5\,V$ $AV_{BB} = -3\,V$ $V_{ref+} = +2\,V$ $V_{ref-} = 0\,V$ $AGND = DGND = 0\,V$
$T_{amb} = +25\,°C$

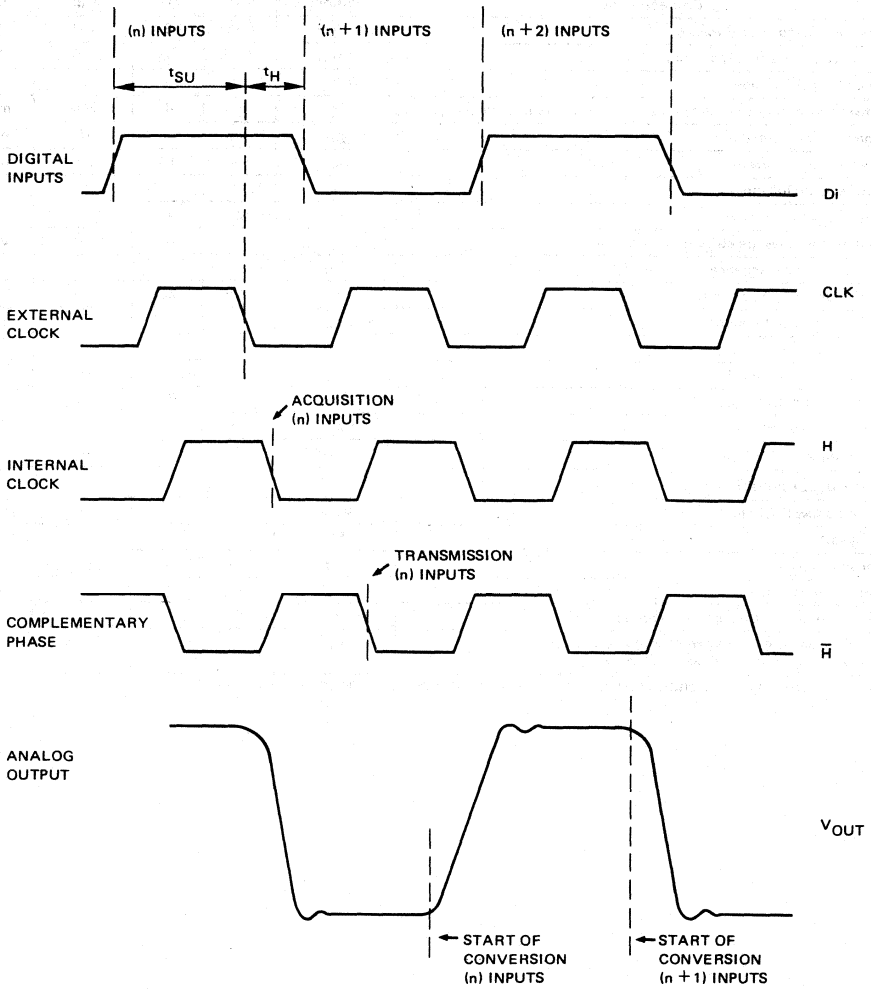
Characteristic	Symbol	Min	Typ	Max	Unit
Positive anolog supply voltage	AV_{DD}	4.75	5	5.25	V
Negative analog supply voltage	AV_{BB}	- 3.15	- 3	- 2.85	V
Digital supply voltage	DV_{DD}	4.75	5	5.25	V
Power dissipation. (Without load and at maximum clock frequency)	P_D	—	140	200	mW
Analog supply current	I_{DA}	—	9	15	mA
Digital supply current	I_{DD}	—	13	25	mA
Low level digital input	V_{IL}	—	—	0.8	V
High level digital input	V_{IH}	2	—	—	V
Digital input leakage current	I_L	—	—	10	μA
Digital input capacitance	C_{IN}	—	—	10	pF
Maximum conversion rate	F_S	20	25	—	MHz
Minimum clock frequency	$F_{C\,min}$	—	1	10	kHz
Set up time.(See timing)	t_{SU}	0	—	—	ns
Hold time.(See timing)	t_H	15	—	—	ns
Settling time (to ± 1/2 L.S.B.)	t_S	—	35	45	ns
Clock pulse width low	t_{PWL}	15	—	—	ns
Clock pulse width high	t_{PWH}	15	—	—	ns

Video output amplifier :

Gain bandwith product	$A_V.BP$	—	80	—	MHz
Slew rate	SR	—	100	—	$V/\mu S$
Closed loop gain	A_V	—	0.9	—	—
Output impedance	R_{OUT}	—	1	3	Ω
Load resistance.(Connected to ground)	R_L	75	—	—	Ω
Load capacitance (If a higher capacitor is applied, overshoot oscillations must be filtered)	C_L	—	—	25	pF

N.B: To improve dynamic characteristics, no current limitation is provided in this device.

TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

- Circuit TS8408 includes the following:
  - a network of identical series resistors and related acces switches,
  - a clock circuit,
  - a logic part to store and decode digital inputs,
  - an output video amplifier.
  - The resistor network is built around a matrix with 16 rows and 16 columns. This network includes 256 taps and delivers 256 voltage references distributed linearly between V_{ref-} and V_{ref+}.
    256 switches controlled in groups of 16 permit selection of the voltages corresponding to one column.
    16 switches each connected to 16 column selection switches are used for selecting one of the 16 voltages selected previously, the voltage which corresponds to the input digital combination.
    Two row and column decoders control these switches.
  - The clock circuit reshapes the external clock to provide 2 non overlapping internal clock phases.
  - Data are stored by means of 8 dynamic registers. Data are acquired on the falling edge of the external clock and output from the registers on the following rising edge.
  - The output video amplifier impedance stage mounted performs impedance matching between the resistor network and the output circuit.

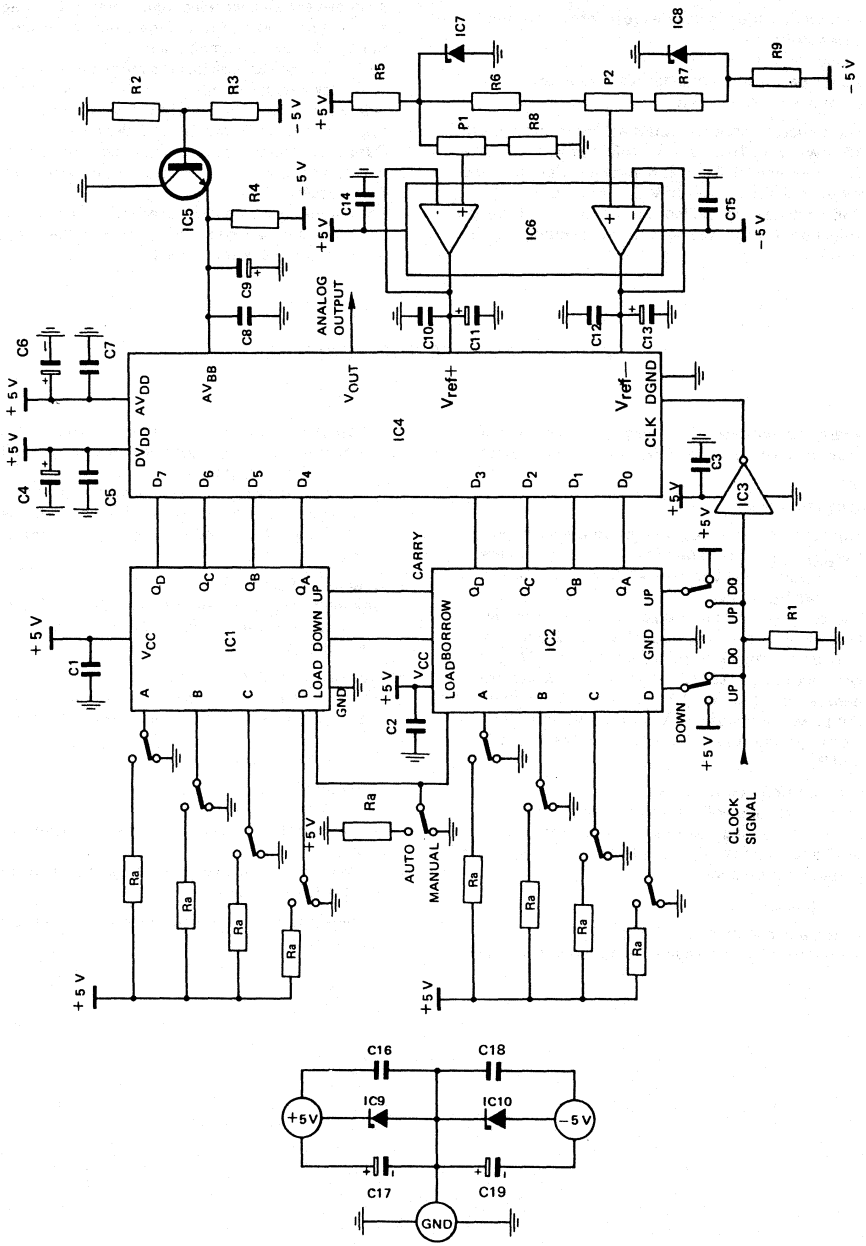
TYPICAL EVALUATION* CIRCUIT

The general circuit used to evaluate the converter in typical conditions (8 bits - 25 MHz) is shown on the next page.

- Voltage references:
  - The converter requires a negative power supply (AV_{BB}) of —3 V generated by the circuit from the power supply voltage (—5 V), transistor IC_5 and resistors R_2, R_3, R_4.
  - The converter requires a positive reference voltage (V_{ref+}) lying between 1 V and 2.5 V (typ: 2 V) and a negative reference voltage (V_{ref-}) lying between —0.5 V and 1 V (typ: 0 V) which are generated by the circuit (+2.5 V and —2.5 V) from the power supplies (+5 V and —5 V), the precision regulation diodes IC_7 and IC_8 and resistors R_5 and R_9.
- Converter reference voltages
  From the previous voltage references (+2.5 V and —2.5 V) the circuit generates the converter positive (V_{ref+}) and negative (V_{ref-}) referencre voltages as indicated on the diagram.
- Up/Down count:
  - Automatic operation (dynamic):
    The circuit allows the converter to convert voltage ramps with positif (up count) or negative (down count) slopes up to frequencies exceeding 25 MHz.
  - Manual operation (static):
    The circuit is used to check converter static operation by sending to its digital inputs the 256 possible binary combinations (from 0 to 255) with 8 bits.
- Overvoltage protection.
  Unidirectional protection transits (IC_9 and IC_{10}) protect the converter from possible power supply overvoltages.
- Electrical considerations.
  A number of elementary precautions should be taken in the component layout when using high frequencies.
  These are the following:
  - ground plane for the components,
  - single ground reference point,
  - star-distributed power supplies to prevent looping,
  - maximum capacitive uncoupling as close as possible to the circuits.

* For typical application circuit, the same surroundings can be used.

TYPICAL EVALUATION CIRCUIT
(continued)

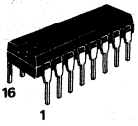


TYPICAL EVALUATION CIRCUIT (CONTINUED)

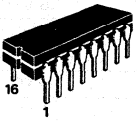
Component	Value	Component	Value
R1	47Ω (1/4 w)	C10	100nf (50 v)
R2	18 KΩ (1/4 w)	C11	1 μ f (25 v) tantalum
R3	22 KΩ (1/4 w)	C12	100 nf (50 v)
R4	220Ω (1/4 w)	C13	1 μ f (25 v) tantalum
R5	2 KΩ (1/4 w)	C14	100 nf (50 v)
R6	8.2 KΩ (1/4 w)	C15	100 nf (50 v)
R7	12 KΩ (1/4 w)	C16	100 nf (50 v)
R8	5.6 KΩ (1/4 w)	C17	1 μ f (25 v) tantalum
R9	2 KΩ (1/4 w)	C18	100 nf (50 v)
Ra	4.7 KΩ (resistor array)	C19	1 μ f (25 v) tantalum
P1	10 KΩ (multiturn)	IC1	74 F 193
P2	10 KΩ (multiturn)	IC2	74 F 193
C1	100 nf (50 v)	IC3	74 LS 04
C2	100 nf (50 v)	IC4	T S 8408
C3	100 nf (50 v)	IC5	2N 2369
C4	1 μf (25 v) tantalum	IC6	TDB 0084
C5	100 nf (50 v)	IC7	TDB 0136
C6	1 μf (25 v) tantalum	IC8	TBD 0136
C7	100 nf (50 v)	IC9	TG MP5
C8	100 nf (50 v)	IC10	TG MP5
C9	1 μ (25 v) tantalum		

PHYSICAL DIMENSIONS

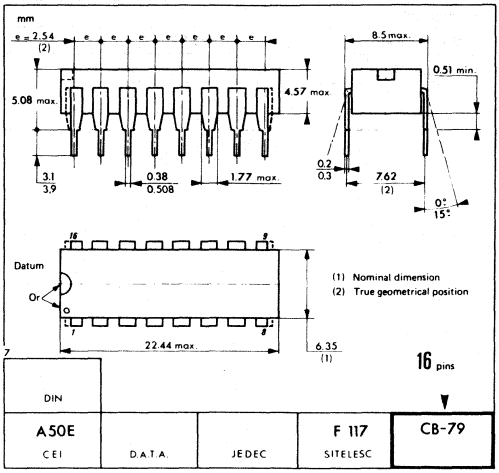
CB-79



P SUFFIX
PLASTIC PACKAGE



J SUFFIX
CERDIP PACKAGE



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THOMSON COMPONENTS SEMICONDUCTEURS

TS8428

5 MHz 8 BIT VOLTAGE OUTPUT D/A CONVERTER

ADVANCE INFORMATION

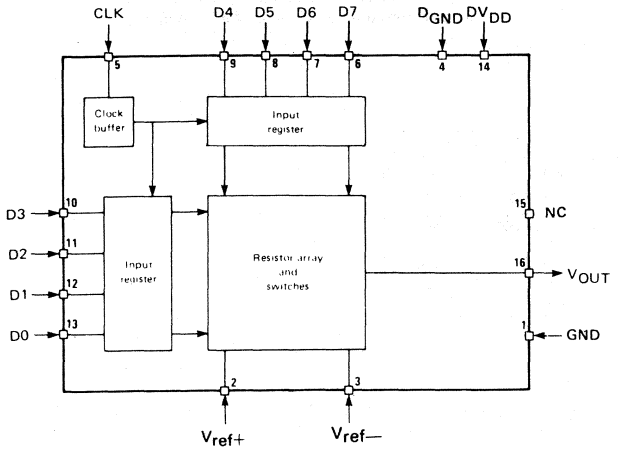
The TS8428 circuit is an 8-bit monolithic digital to analog converter incorporating latches for the logic inputs, designed for 5 MHz conversion rate and implemented in HMOS2 technology. The TS8428 can be compared to a digital potentiometer with an output resistance R_{out} = 3kΩ. The circuit is supplied between +5 V and GND. This converter offers an inherent monotonicity due to the structure and an integral linearity better than ± 1/2 LSB.

- Differential linearity: ±1/4 LSB error maximum.
- Integral linearity error: ±1/2 LSB typ.
- Single power supply: +5 V.
- Digital inputs are TTL and CMOS compatible.
- 16 pins DIL package.

Typical applications:

- Digitally controlled potentiometer.
- Analog function generator.
- All high speed 8-bit DAC where very low power and low cost are required

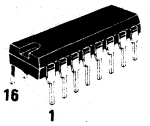
BLOCK DIAGRAM



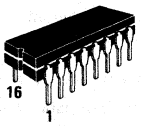
HMOS2

5 MHz
8-BIT VOLTAGE OUTPUT
D/A CONVERTER

CASE CB-79



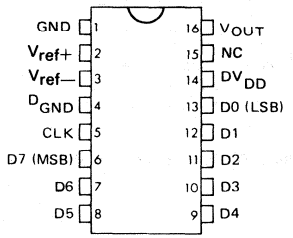
P SUFFIX
PLASTIC PACKAGE



J SUFFIX
CERDIP PACKAGE

Ceramic package (C suffix) is also available

PIN ASSIGNMENT



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PIN DESCRIPTION

Name	Type	Number	Function	Description
GND	I	1	Ground	
V_{ref+}	I	2	Upper reference	Access to the upper reference voltage. A voltage source must be applied
V_{ref-}	I	3	Lower reference	Access to the lower reference voltage. A voltage source must be applied (or ground)
DGND	I	4	Digital ground	
CLK	I	5	Clock input	TTL levels
D_0 (LSB) to D_7 (MSB)	I	6 to 13	Digital input	
DV_{DD}	I	14	Digital supply	
NC		15	Non connected	
V_{out}	O	16	Analog output	

FUNCTIONAL DESCRIPTION

- Circuit TS8428 includes the following:
  - — a network of identical series resistors and related access switches,
  - — a clock circuit,
  - — a logic part to store and decode digital inputs.

The resistor network is built around a matrix with 16 rows and 16 columns. This network includes 256 taps and delivers 256 voltage references distributed linearly between V_{ref-} and V_{ref+}. 256 switches controlled in groups of 16 permit selection of the voltages corresponding to one column.

16 switches each connected to 16 column selection switches are used for selecting out of the 16 voltages selected previously, the voltage which corresponds to the input digital combination.
Two row and column decoders control these switches.

The clock circuit reshapes the external clock to provide 2 non overlapping internal clock phases.

Data are stored by means of 8 dynamic registers. Data are acquired on the falling edge of the external clock and output from the registers on the following rising edge.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage (1)	DV_{DD}	- 0.3 to + 7	V
Operating temperature	T_{oper}	0 to 70	°C
Storage temperature	T_{stg}	- 55 to 150	°C
Power supply current	IDV_{DD} ID_{GND}	150	mA
Digital and analog inputs (1)	V_{in}	- 0.3 to + 7	V

Note: (1) With respect to DGND = GND

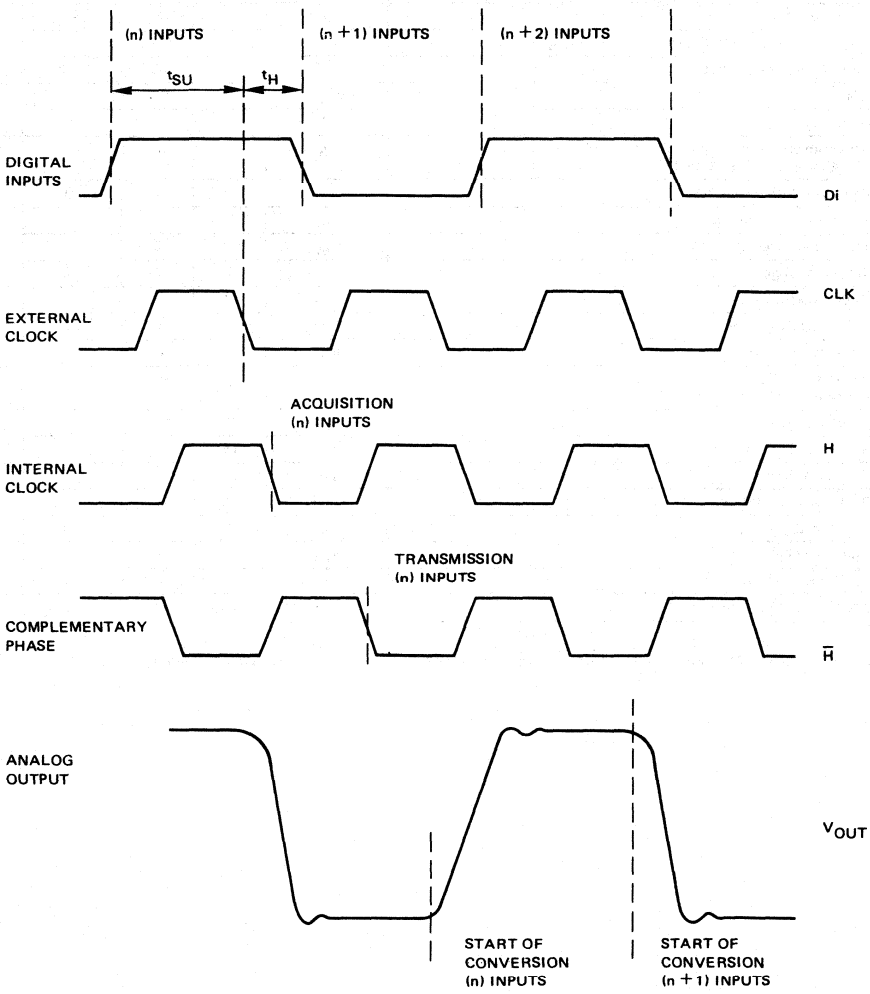
ELECTRICAL OPERATING CHARACTERISTICS

$DV_{DD} = +5$ V $V_{ref+} = +2$ V $V_{ref-} = 0$ V GND = 0 V
$T_{amb} = +25$ °C

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	N	—	8	—	Bit
Integral linearity error. (Given values according to the "best line")	ILE	—	± 0.5	± 1	LSB
Differential linearity error	DLE	—	± 0.1	± 0.25	LSB
Offset	V_{OFF}	—	0.5	—	LSB
Gain	G	—	1	—	
Maximum conversion rate. (With an external output video amplifier, 5 pF load)	F_S	—	5*	—	MHz
Minimum clock frequency	F_{CL}	—	1	10	kHz
Lower reference voltage	V_{ref-}	0	0	—	V
Upper reference voltage	V_{ref+}		2	3.5	V
Full-scale range	$V_{ref+} - V_{ref-}$	1	2	3.5	V
Ladder resistance	R_{ref}	1.5	2	2.7	KΩ
Digital supply voltage	DV_{DD}	4.75	5	5.25	V
Digital supply current	I_{DD}	—	13	25	mA
Power dissipation. (Without load and at maximum clock frequency)	P_D	—	65	125	mW
Setup time. (See timing)	t_{SU}	0	—	—	ns
Hold time. (See timing)	t_H	15			ns
Clock pulse width low	t_{PWL}	60	—	—	ns
Clock pulse width high	t_{PWH}	60			ns
Low level digital input	V_{IL}	—	—	0.8	V
High level digital input	V_{IH}	2	—	—	V
Digital input leakage current	I_L	—	—	10	μA
Digital input capacitance	C_{IN}	—	—	10	pF

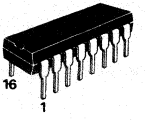
*Maximum conversion rate is only limited by the output resistor (3 KΩ typ.) and capacitive load

TIMING DIAGRAM

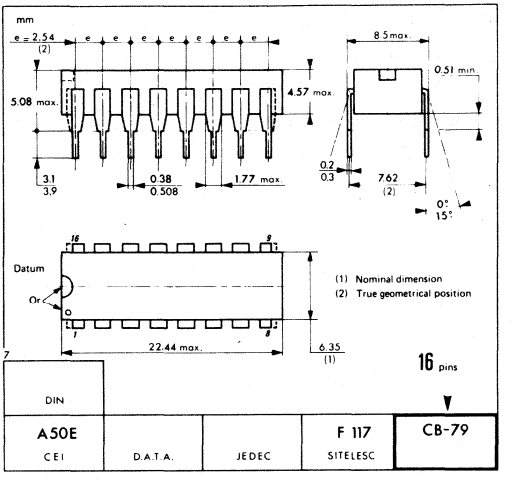


PHYSICAL DIMENSIONS

CB-79



P SUFFIX
PLASTIC PACKAGE
J SUFFIX
CERDIP PACKAGE



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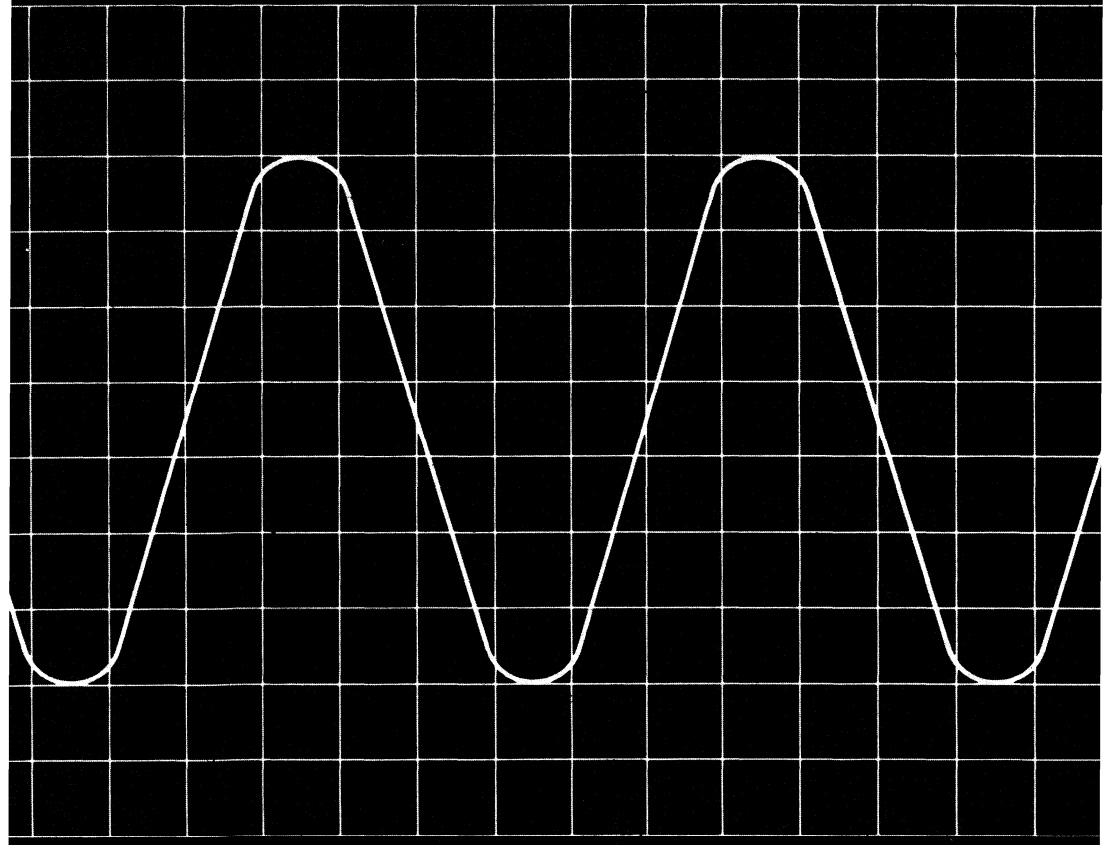
NOTES

Printed in France

IMPLEMENTATION AROUND TS8308 AND TS8408 VIDEO CONVERTER

APPLICATION NOTES — AN-062



THOMSON
COMPONENTS
SEMICONDUCTEURS

O. LEENHARDT: Applications laboratory

INTRODUCTION

Apart from its numerous advantages, digital data processing has made considerable progress over the last few years, firstly with signals occupying a limited frequency spectrum, then with signals covering a wider frequency spectrum and finally today with signals covering a very large frequency band (several MHz) such as video and radar.

For the handling of such signals (6-9 bits, 5-30 MHz) there exists at present a certain number of bipolar or hybrid converters but which for many applications are both costly and complex. Also, their power consumption (greater than 1 Watt) is generally high and their implementation is not always as simple as one would desire.

The goal of this application note is to show the minimum surroundings required around the two THOMSON SEMICONDUCTEURS 8-bit video converters (TS 8308 (A.D.C.) and TS 8408 (D.A.C)), then to infer their very high implementation facilities.

EXAMPLE OF AN EVALUATION CIRCUIT FOR TS 8308 IN TYPICAL CONDITIONS

INTRODUCTION

A general purpose evaluation circuit used for the Flash converter in typical conditions is represented figure 1. This circuit allows the following possibilities:

- Resolution: 8 bit (with overflow bit).
- Conversion rate: 15 MHz (typ), 20 MHz (max).
- Analog bandwith: 3.5 MHz (typ), 5 MHz (max).
- Self-contained and adjustable positive voltage references.
- Input DC level adjustable from 0 to 2.5 V.
- Access to three taps of the resistor ladder (R/4, R/2 and 3R/4).
- Choice of clock polarity.
- Power supply voltages: ± 5 V.

CIRCUIT ELECTRICAL DESCRIPTION

Voltage references

As the Flash converter requires a positive reference voltage ($VREF^+$) ranging from 1 V to 3 V (typ: 2 V), the circuit generates a voltage reference of 2.5 V from the power supply voltage (+ 5 V) and a precision regulation diode (IC 1).

Resistor ladder reference voltages

The circuit can be used to access some particular points of the resistor ladder. These points correspond to 3/4, 1/2 and 1/4 of the ladder totale resistance. This feature enables the use of the Flash converter in two ways:

- in a linear operation with these three points grounded by uncoupling capacitors in order to filter disturbances along the ladder (K2, K3 and K4 on position 2),
- in a non-linear operation with the following two functions:
  - — improvement in Flash converter integral linearity by forcing these three points to their corresponding voltages (K2, K3 and K4 on position 1),
  - — implementation of a non-linear conversion law (compression law for example) in order to better observe the results of the conversion on a specific part only of the transfer characteristic (K2, K3 and K4 on position 1).

Analog signal

The input analog signal must be driven by a wideband buffer amplifier (IC3) with a very low output impedance (< 50 Ohm).

In order to eliminate the almost uncontrollable offsets introduced by the source generator or the buffer amplifier proper, two capacitors parallel mounted (C15 and C16) are added in series after the amplifier.

For low frequencies (< 1 MHz), tantalum capacitor (C15) is used as a short-circuit; for higher frequencies (> 1 MHz), ceramic capacitor (C16) is used as a short-circuit.

After these capacitors, a potentiometer (P5) with the middle point connected to the Flash converter input adds a DC component to the input signal.

The signal thus obtained has a DC value different from zero, lying between $VREF^+$ and $VREF^-$, and which can be converted by the Flash converter.

Clock signal

Clock signal is a TTL or a CMOS signal. The "PHASE" command can be used to invert (K1 on position 1) or not (K1 on position 2) the external clock.

Considerations on electrical layout

A certain number of elementary precautions must be taken on the electrical layout when using high frequencies. The main ones are as follows:

- a ground plane for the component side,
- ground tracks corresponding to the various signals (clock, input signal, references) separated and connected together only to a single point,
- power supplies and grounds star-distributed in order to avoid any possible loop,
- maximum capacitive uncoupling as close as possible to each circuit.

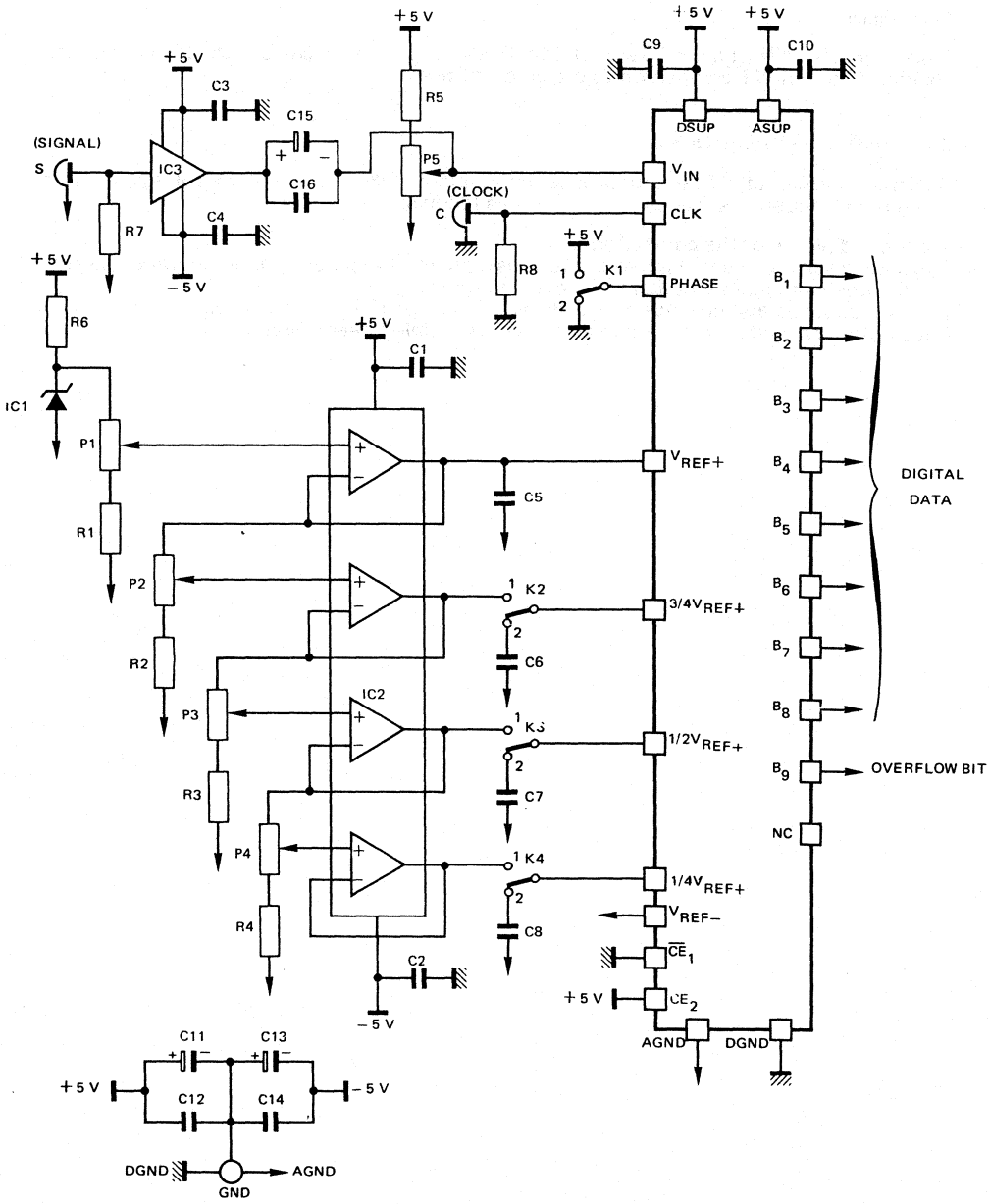

+5 V
C3
C15
R5
C9
C10
DSUP
ASUP
(SIGNAL)
S
IC3
C16
P5
V_{IN}
(CLOCK)
C
CLK
C4
R7
R8
K1
PHASE
-5 V
R6
C1
IC1
P1
V_{REF+}
B_1
B_2
B_3
B_4
B_5
B_6
B_7
B_8
B_9
DIGITAL DATA
OVERFLOW BIT
NC
C5
R1
P2
K2
$3/4V_{REF+}$
C6
R2
IC2
P3
K3
$1/2V_{REF+}$
C7
R3
P4
K4
$1/4V_{REF+}$
V_{REF-}
R4
C8
$\overline{CE}_1$
CE_2
C2
AGND
DGND
C11
C13
C12
C14
GND

FIGURE 1

COMPONENT VALUES

R1 = 5.6 kΩ (1/4 W)
R2 = 3.3 kΩ (1/4 W)
R3 = 1.2 kΩ (1/4 W)
R4 = 560 Ω (1/4 W)
R5 = 10 kΩ (1/4 W)
R6 = 2 kΩ (1/4 W)
R7 = 47 Ω (1/4 W)
R8 = 47 Ω (1/4 W)

P1 = 10 kΩ (multiturn)
P2 = 10 kΩ (multiturn)
P3 = 10 kΩ (multiturn)
P4 = 10 kΩ (multiturn)
P5 = 10 kΩ (multiturn)

C1 = 100 nF 63 V
C2 = 100 nF 63 V
C3 = 100 nF 63 V
C4 = 100 nF 63 V
C5 = 100 nF 63 V
C6 = 100 nF 63 V
C7 = 100 nF 63 V
C8 = 100 nF 63 V
C9 = 100 nF 63 V
C10 = 100 nF 63 V
C11 = 68 µF 16 V (Tantalum)
C12 = 100 nF 63 V
C13 = 68 µF 16 V (Tantalum)
C14 = 100 nF 63 V
C15 = 68 µF 16 V (Tantalum)
C16 = 100 nF 63 V

IC1 = TDB 0136
IC2 = TDB 0084
IC3 = LH 0002
IC4 = TS 8308

EXAMPLE OF AN EVALUATION CIRCUIT FOR TS 8408 IN TYPICAL CONDITIONS

INTRODUCTION

A general purpose evaluation circuit used for the DAC in typical conditions is represented figure 2. This circuit allows the following possibilities:

- Resolution: 8 bit.
- Conversion rate: 20 MHz (typ), 25 MHz (max).
- Self-contained and adjustable voltage references.
- Self-contained TS 8408 transient overvoltage protection.
- Digital input choice:
  - — Count up and count down with synchronous clock counters.
  - — Dedicated inputs according to specified application.
  - — Static inputs.
- Clock choice:
  - — Internal (with quartz oscillator).
  - — External.
- Power supply voltages: ± 5 V.

CIRCUIT ELECTRICAL DESCRIPTION

Voltage references

- The DAC requires a negative power supply (AVBB) of — 3 V which is generated by the circuit from the power supply voltage (— 5 V), the transistor IC5 and the resistors R2, R3 and R4.
- As the DAC requires a positive voltage reference ($VREF^+$) lying between 1 V and 3 V (typ: 2 V) and a negative voltage reference ($VREF^-$) lying between — 0.5 V and 1 V (typ: 0 V), the circuit generates two voltage references (+ 2.5 V and — 2.5 V) from the power supplies (+ 5 V and — 5 V), the precision regulation diodes IC7 and IC8, and the resistors R5 and R9.

DAC reference voltages

From the previous voltage references (+ 2.5 V and — 2.5 V), the circuit generates the DAC positive ($VREF^+$) and negative ($VREF^-$) reference voltages as indicated on the figure 2.

Count up/down

- Automatic operation (dynamic) (K9 on position 2):
  The circuit allows the DAC to convert voltage ramps with positive (Count up: K11 on position 1, K12 on position 2) or negative (Count down: K11 on position 2, K12 on position 1) slopes up to frequency exceeding 25 MHz.
- Manual operation (static) (K9 on position 1):
  The circuit can be used to check DAC static operation by sending to its digital inputs the 256 possible binary combinations (from 0 to 255) with 8 bits (K1, K2, K3, K4, K5, K6, K7 and K8).

Clock signal

The clock signal is a TTL or a CMOS signal. It can be an internal (K10 on position 2) or an external (K10 on position 1) signal.

Transient overvoltage protection

Unidirectional protection transils (IC9 and IC10) are used to protect the DAC from possible transient power supply overvoltages.

Electrical considerations

A certain number of elementary precautions must be taken in the electrical layout when using high frequencies. The main ones are as follows:

- a ground plane for the component side,
- a single ground reference point,
- star-distributed power supplies,
- maximum capacitive uncoupling as close as possible to each circuit.

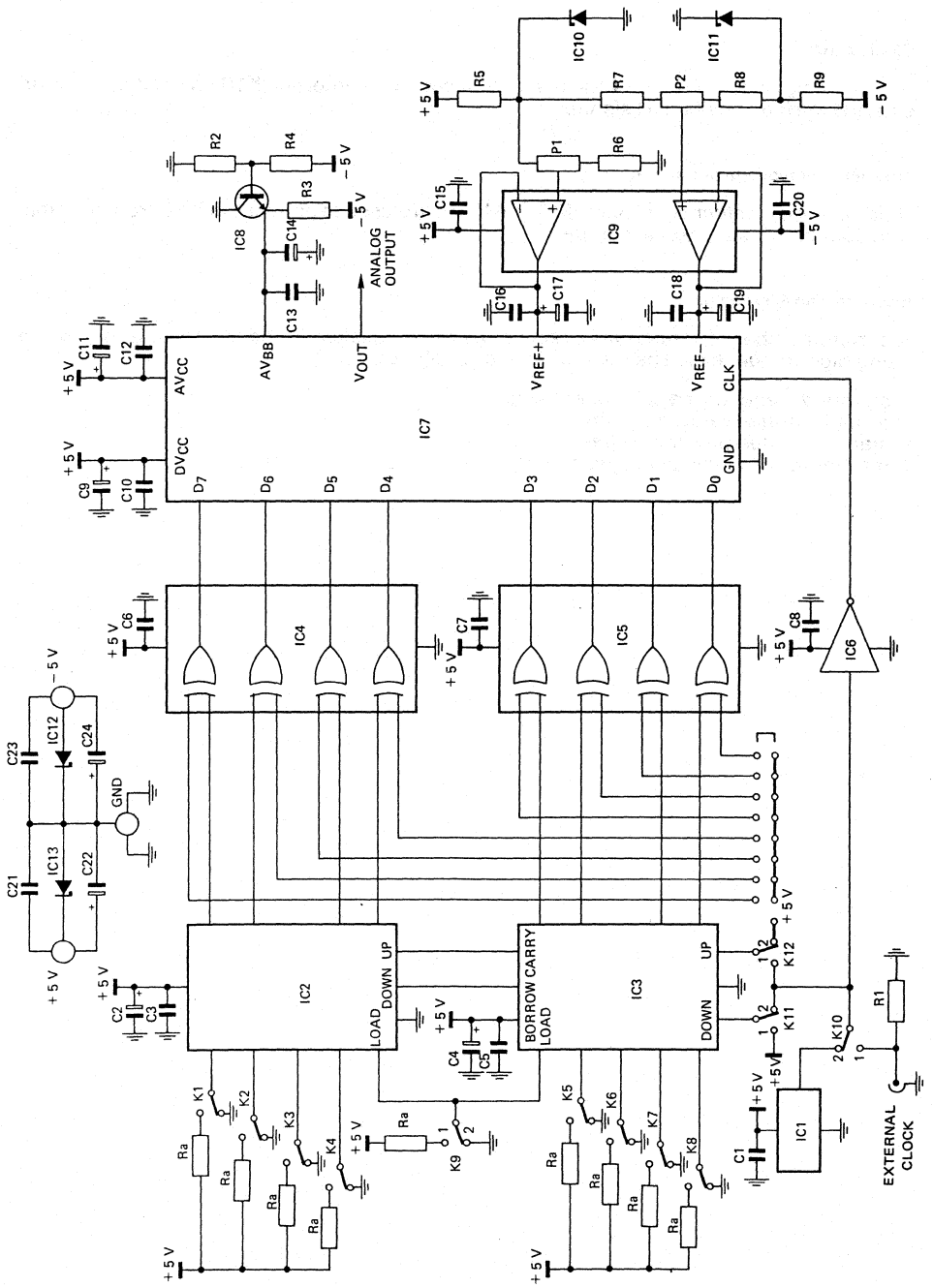

IC10
IC11
+5 V
R5
R7
P2
R8
R9
−5 V
R2
R4
P1
R6
R3
IC8
C14
C13
ANALOG OUTPUT
C15
C20
IC9
C16
C17
C18
C19
C11
C12
AVCC
AVBB
VOUT
VREF+
VREF−
CLK
IC7
DVCC
C9
C10
D7
D6
D5
D4
D3
D2
D1
D0
GND
C6
IC4
C7
IC5
C8
IC6
IC12
C23
C24
GND
IC13
C21
C22
IC2
DOWN UP
LOAD
BORROW CARRY
LOAD
IC3
UP
DOWN
C2
C3
C4
C5
K12
K11
K10
R1
EXTERNAL CLOCK
IC1
C1
K1
K2
K3
K4
K5
K6
K7
K8
K9
Ra

FIGURE 2

COMPONENT VALUES

R1 = 47 Ω (1/4 W)
R2 = 18 kΩ (1/4 W)
R3 = 220 Ω (1/4 W)
R4 = 22 kΩ (1/4 W)
R5 = 2 kΩ (1/4 W)
R6 = 5.6 kΩ (1/4 W)
R7 = 8.2 kΩ (1/4 W)
R8 = 12 kΩ (1/4 W)
R9 = 2 kΩ (1/4 W)
Ra = 4.7 kΩ (Resistor array)

P1 = 10 kΩ (multiturn)
P2 = 10 kΩ (multiturn)

C1 = 100 nF 50 V
C2 = 1 µF 25 V (Tantalum)
C3 = 100 nF 50 V
C4 = 1 µF 25 V (Tantalum)
C5 = 100 nF 50 V
C6 = 100 nF 50 V
C7 = 100 nF 50 V
C8 = 100 nF 50 V
C9 = 1 µF 25 V (Tantalum)
C10 = 100 nF 50 V
C11 = 1 µF 25 V (Tantalum)
C12 = 100 nF 50 V
C13 = 100 nF 50 V
C14 = 1 µF 25 V (Tantalum)
C15 = 100 nF 50 V
C16 = 100 nF 50 V
C17 = 1 µF 25 V (Tantalum)
C18 = 100 nF 50 V
C19 = 1 µF 25 V (Tantalum)
C20 = 100 nF 50 V
C21 = 100 nF 50 V
C22 = 22 µF 35 V (Tantalum)
C23 = 100 nF 50 V
C24 = 22 µF 35 V (Tantalum)

IC1 = K 1114 A (20 MHz)
IC2 = 74 ALS 193
IC3 = 74 ALS 193
IC4 = 74 S 86
IC5 = 74 S 86
IC6 = 74 LS 04
IC7 = TS 8408
IC8 = 2N 2369
IC9 = TDB 0084
IC10 = TDB 0136
IC11 = TDB 0136
IC12 = 1N 5908
IC13 = 1N 5908

EXAMPLE OF INTERFACING THE TS 8308 AND THE TS 8408

INTRODUCTION

A general purpose interfacing circuit used for TS 8308 and TS 8408 is represented figure 3. This circuit allows the A/D and the D/A conversions of an analog signal with the following possibilities:

- Analog bandwidth: 3.5 MHz (typ), 5 MHz (max).
- Conversion rate: 15 MHz (typ), 20 MHz (max).
- Self-contained and adjustable positive voltage reference for each converter.
- Self-contained transient overvoltage protection.
- Input DC level adjustable from 0 to 2.5 V.
- Clock choice:

  — Internal (with quartz oscillator).
  — External.

- Choice of clock polarity (for TS 8308).
- Implementation of "PERITELEVISION" plug for the TV signal conversion (TV application).
- Power supply voltages:

  — ± 5 V (for ADC and DAC).
  — +12 V (for TV application).

CIRCUIT ELECTRICAL DESCRIPTION

Voltage references

- The circuit generates the negative supply voltage (— 3 V) required by the DAC from the transistor IC9 and the resistors R10, R11 and R12.
- The circuit generates also two positive voltage references of 2.5 V from the positive supply voltage (+ 5 V) and a precision regulation diode (IC11 and IC12).

ADC and DAC reference voltages

- From the previous voltage reference (2.5 V), the circuit generates ADC and DAC positive reference voltages ($VREF^+$) as indicated on figure 3.
- The TS 8308 resistor ladder is used in a linear operation (R/4, R/2 and 3R/4 grounded by uncoupling capacitors).

Analog signal

The input analog signal is driven as previously explained (2).

Clock signal

The clock signal can be an internal (K3 on position 2) or an external (K3 on position 1) signal. The "PHASE" command can be used to invert (K4 on position 1) or not (K4 on position 2) the TS 8308 clock signal.

Transient overvoltage protection

The transient overvoltage protection is implemented on the circuit as previously explained (1).

TV application

The circuit allows to use the "PERITELEVISION" plug for TV signal conversion. For this application, it is required to switch the pin 8 of this plug to + 12 V. Thus, it is possible to access on the circuit (pin 19 of the plug) to the TV signal coming from the antenna.

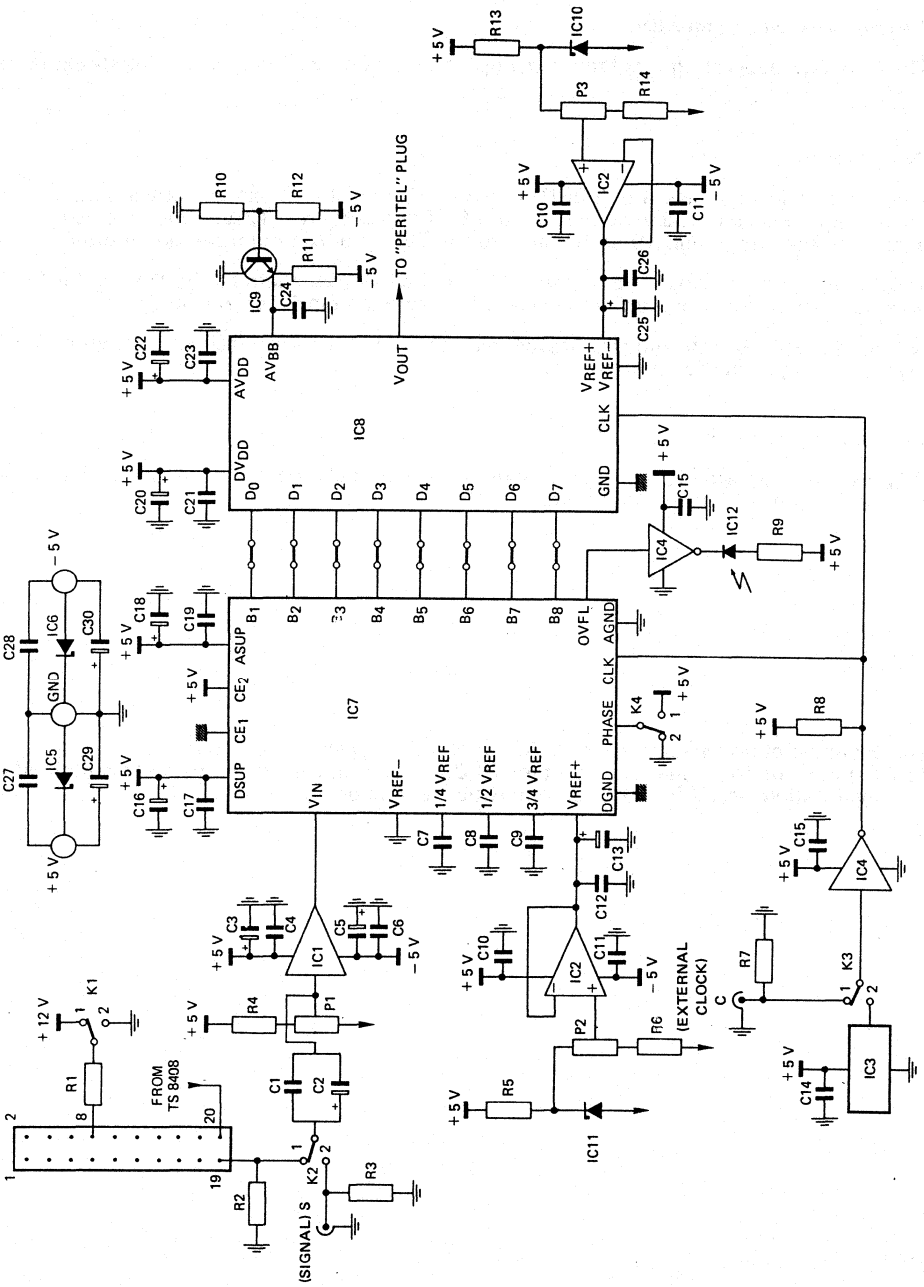
The TV signal is so converted by the ADC, then converted again by the DAC to be finally applied to the video input of the television set (from the pin 20 of the plug).

NOTE: If the pin 8 of the plug is not switched to + 12 V, it is not possible to access to the TV signal coming from the antenna.

Electrical considerations

As previously explained (2) the same layout and electrical precautions must be taken when interfacing the two video converters.

(1) Example of an evaluation circuit for TS 8408 in typical conditions.
(2) Example of an evaluation circuit for TS 8308 and typical conditions and example of an evalutation circuit for TS 8408 and typical conditions.



TO "PERITEL" PLUG
IC8
IC7
IC1
IC2
IC3
IC4
IC5
IC6
IC9
IC10
IC11
IC12
AVDD
AVBB
VOUT
VREF+
VREF−
CLK
GND
DVDD
D0
D1
D2
D3
D4
D5
D6
D7
B1
B2
B3
B4
B5
B6
B7
B8
ASUP
CE2
CE1
DSUP
VIN
VREF−
1/4 VREF
1/2 VREF
3/4 VREF
VREF+
DGND
OVFL
AGND
PHASE
CLK
GND
+5 V
−5 V
+12 V
FROM TS 8408
(SIGNAL) S
(EXTERNAL CLOCK)
K1
K2
K3
K4
P1
P2
P3
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30

FIGURE 3

COMPONENT VALUES

R1 = 4.7 kΩ (1/4 W)
R2 = 68 Ω (1/4 W)
R3 = 47 Ω (1/4 W)
R4 = 10 kΩ (1/4 W)
R5 = 2 kΩ (1/4 W)
R6 = 5.6 kΩ (1/4 W)
R7 = 47 Ω (1/4 W)
R8 = 1 kΩ (1/4 W)
R9 = 180 Ω (1/4 W)
R10 = 18 kΩ (1/4 W)
R11 = 220 Ω (1/4 W)
R12 = 22 kΩ (1/4 W)
R13 = 2 kΩ (1/4 W)
R14 = 5.6 kΩ (1/4 W)

P1 = 10 kΩ (multiturn)
P2 = 20 kΩ (multiturn)
P3 = 20 kΩ (multiturn)

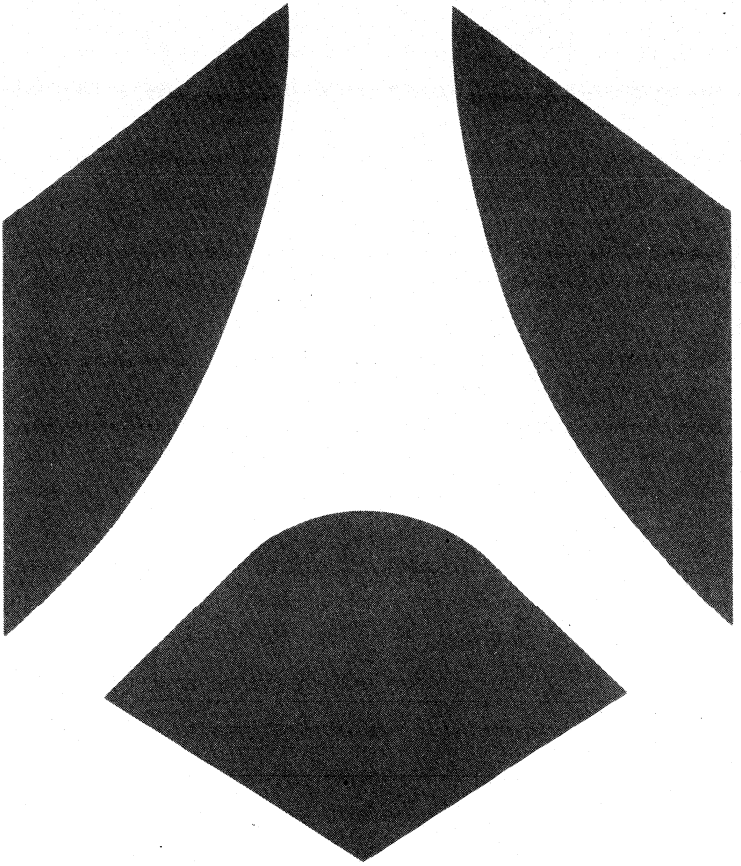
C1 = 100 nF 50 V
C2 = 68 µF 16 V (Tantalum)
C3 = 1 µF 35 V (Tantalum)
C4 = 100 nF 50 V
C5 = 1 µF 35 V (Tantalum)
C6 = 100 nF 50 V
C7 = 100 nF 50 V
C8 = 100 nF 50 V
C9 = 100 nF 50 V
C10 = 100 nF 50 V
C11 = 100 nF 50 V
C12 = 100 nF 50 V
C13 = 1 µF 35 V (Tantalum)
C14 = 100 nF 50 V
C15 = 100 nF 50 V
C16 = 1 µF 35 V (Tantalum)
C17 = 100 nF 50 V
C18 = 1 µF 35 V (Tantalum)
C19 = 100 nF 50 V
C20 = 1 µF 35 V (Tantalum)
C21 = 100 nF 50 V
C22 = 1 µF 35 V (Tantalum)
C23 = 100 nF 50 V
C24 = 100 nF 50 V
C25 = 1 µF 35 V (Tantalum)
C26 = 100 nF 50 V
C27 = 100 nF 50 V
C28 = 100 nF 50 V
C29 = 22 µF 16 V (Tantalum)
C30 = 22 µF 16 V (Tantalum)

IC1 = LH 0002
IC2 = TDB 0084
IC3 = K 11488 (16 MHz)
IC4 = SN 7406
IC5 = 1N 5908
IC6 = 1N 5908
IC7 = TS 8308
IC8 = TS 8408
IC9 = 2N 2222
IC10 = LM 336
IC11 = LM 336
IC12 = LED

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France



Mask programmable filters

MASK - PROGRAMMABLE SWITCHED CAPACITOR FILTERS

Part number	Function	Type	Order	Clock to cut-off freq. ratio	Package	Suffix	Page
TSG85XX	—	—	—	—	—		5.9
TSG8510	Low pass	Cauer	5	75.3			5.29
TSG8511	Low pass	Cauer	7	75.3			5.35
TSG8512	Low pass	Cauer	7	100	DIL8		5.41
TSG8513	Low pass	Chebychev	8	60			5.47
TSG8514	Low pass	Butterworth	8	80		P	5.53
TSG8530	High pass	Cauer	3	320			5.59
TSG8531	High pass	Cauer	6	400	DIL16		5.65
TSG8532	High pass	Chebychev	6	500			5.71
TSG8550	Band pass	Cauer Q = 7	6	48			5.77
TSG8551	Band pass	Chebychev Q = 35	8	187.2			5.83
TSG8670	Low pass	Cauer	4	85.36	DIL18		5.89
TSGF08 CUSTOM	Low pass High pass Band pass Notch Group delay Equalizers	Butterworth Legendre Chebychev Bessel Cauer	4 to 8	20 to 400	DIL8 DIL16		5.93

A MASK PROGRAMMABLE FILTERS (M.P.F) FAMILY AND ITS "FILCAD" SOFTWARE PACKAGE

A CMOS M.P.F CHIP FAMILY WITH A "CAD PACKAGE" CAPABLE OF TRANSFORM ANY FILTER SPECIFICATION INTO INTEGRATED CIRCUIT ON A SHORT LEAD TIME (4 or 8 weeks depending on filter specifications).

Three M.P.F bases and a complete software package adapted to Switched Capacitor Filter (S.C.F) designs have been developed by THOMSON SEMICONDUCTEURS to solve your filtering problems:

TSG8704 base:

- S.C.F order between 2 and 4.
- 1 optional internal clock oscillator.
- Optional external driving of output sample and hold.
- 1 uncommitted operational amplifier.
- 2 package versions:
  - 8 pins: filter only.
  - 14 pins: filter + 1 op. amp. + oscillator.

TSG8508 base:

- S.C.F order between 4 and 8.
- 2 uncommitted operational amplifiers.
- 2 package versions:
  - 8 pins: filter only.
  - 16 pins: filter + 2 op. amplifiers.

TSG8612 base:

- S.C.F order between 8 and 12.
- 2 filters possibilities on the same chip (Σ order $\leqslant$ 12).
- 2 clock inputs.
- Optional external driving of output sample and hold.
- 2 uncommitted operational amplifiers.
- 5 package versions:
  - 16 pins: 1 filter.
  - 16 pins: 1 filter + driving of output S/H.
  - 18 pins: 2 filters.
  - 20 pins: 2 filters + 2 clock inputs.
  - 20 pins: 2 filters + 2 clock inputs + driving of output S/H.

These three bases are available both for standard and semi custom products.
Customers have the possibility of design themselves their M.P.F thanks to the FILCAD software package and proper training from THOMSON SEMICONDUCTEURS.

FILCAD:

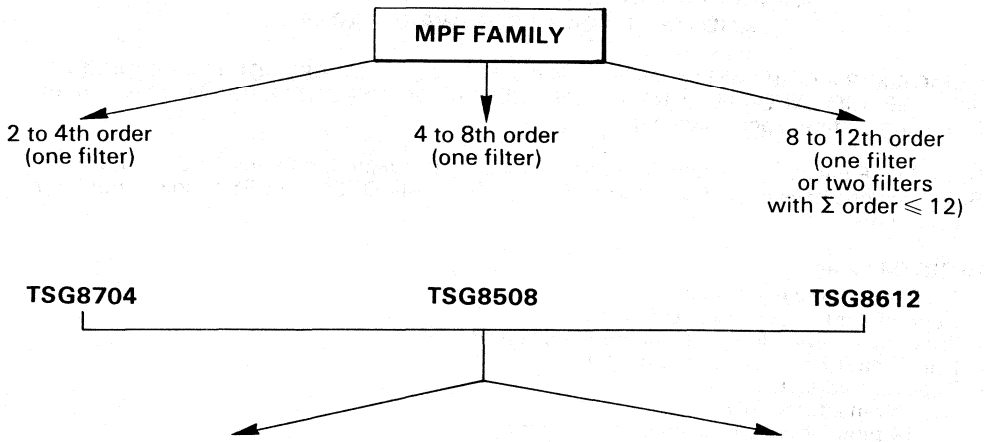
A software package developed by THOMSON SEMICONDUCTEURS for the Mask Programmable Switched Capacitor Filter family:

TSG8704 - TSG8508 - TSG8612

FILCAD input is the filter template. Then, synthesis, simulations and routing programs are linked in order to finally generate the GDS2 layout file for realization of the personalization mask.

FILCAD is available in THOMSON SEMICONDUCTEURS Design Centers and some of its Associated Design Centers.

By using the three M.P.F bases and CAD tools, THOMSON SEMICONDUCTEURS is proposing a complete filter family which includes standard filters and semi custom filters.



Low-pass:

TSG8510: 5th order CAUER (PCM)
TSG8511: 7th order CAUER (50 dB)
TSG8512: 7th order CAUER (75 dB)
TSG8513: 8th order CHEBYCHEV
TSG8514: 8th order BUTTERWORTH

TSGF04 / Customer identification

TSGF08 / Customer identification

TSGF12 / Customer identification

High-pass:

TSG8530: 3rd order CAUER
TSG8531: 6th order CAUER
TSG8532: 6th order CHEBYCHEV

Notch:

TSG8540: 6th order (Q = 7)

Band-pass:

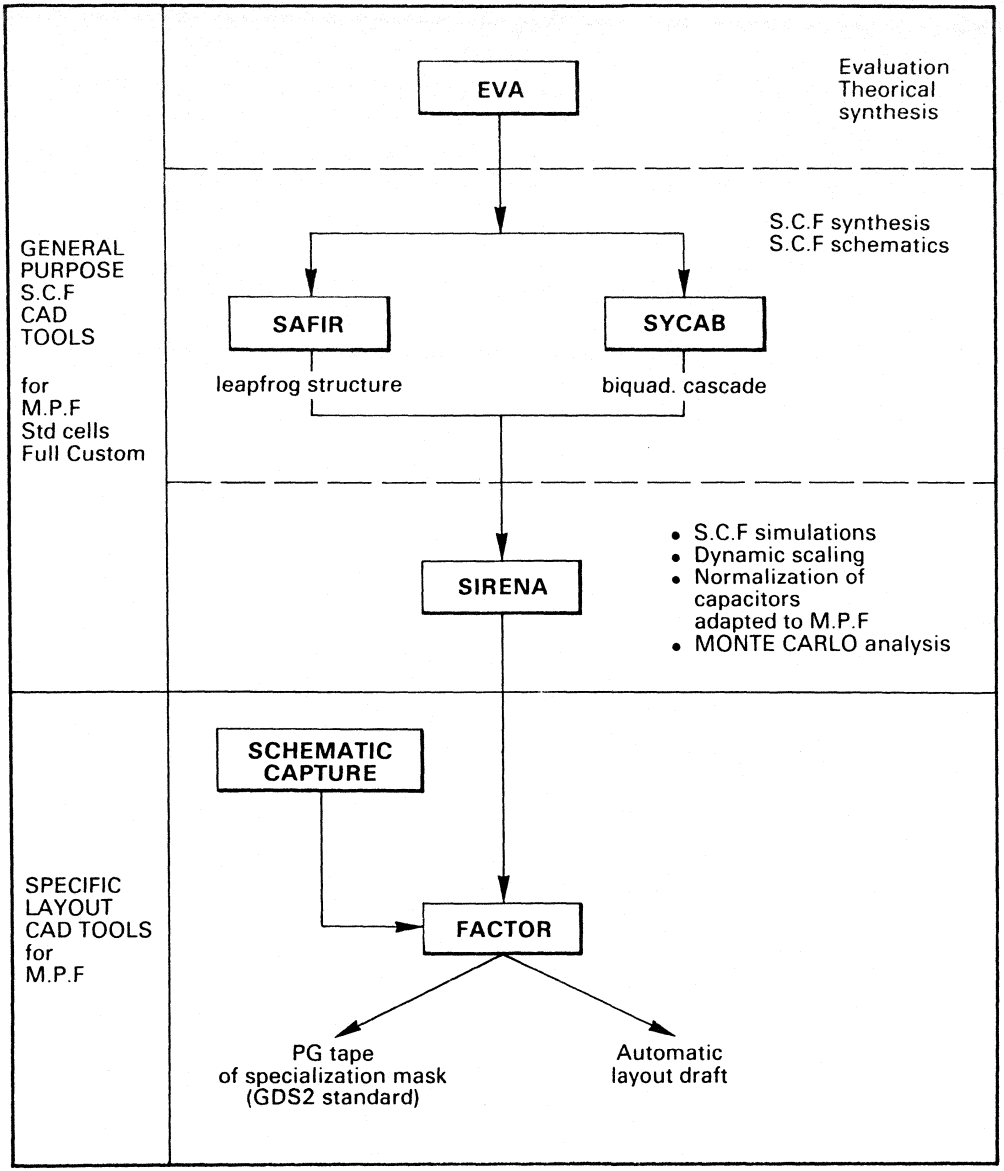
TSG8550: 6th order CAUER (Q = 7)
TSG8551: 8th order (Q = 35)

Voice-grade dual filter for telephone line interface:

TSG8670: 4th order low-pass
8th order band-pass

For every M.P.F, the cutoff frequency (or center frequency for band-pass and notch) is clock programmable: frequency response is shiftable simply by clock tuning.

FILCAD is a software package developed by THOMSON SEMICONDUCTEURS available for its Switched Capacitor Filter designs: M.P.F, but also Full Custom or Semi Custom Circuits containing such Filter cells.



THOMSON COMPONENTS SEMICONDUCTEURS

STANDARD FILTERS TSG85XX
CUSTOMER IDENT.: SEMI CUSTOM FILTERS TSGF08

The TSG85XX circuits are HCMOS universal filters containing a mask programmable switched-capacitor cascadable structure and two uncommitted general purpose operational amplifiers.

The specifications of the internal filter are obtained during the last step of chip realization. The specialization method (Patented) used by THOMSON SEMICONDUCTEURS is close to the one used for gate array integrated circuits.

For semi custom filters, the SCF specialization is implemented either by THOMSON SEMICONDUCTEURS designers in accordance with the user template either by the customer himself thanks to the FILCAD package.

Most filters can be realized. Samples are available 4 to 8 weeks after the filter template definition.

This technique has also been used to define THOMSON SEMICONDUCTEURS family of general purpose filters.

Based on the switched-capacitor structure, these circuits exhibit all the advantages of this technique, namely precise template, high temperature and long-range stability, almost no external component, no adjustment, low consumption, high density, easy customization, low cost and high security of use.

- Available order: 4 to 8 (any type).
- Input signal frequency range: 0 to 30 kHz.
- S/N ratio (depends on the internal structure): 60 to 85 dB.
- Clock tunable cutoff frequency
- Power supply requirements: ±5 V or 0-10 V.
- Power consumption: adjustable from 0.5 mW to 20 mW per order.

AVAILABLE PRODUCTS:

- Standard *

  Low pass:
  TSG8510: 5th order Cauer (PCM)
  TSG8511: 7th order Cauer (50 dB)
  TSG8512: 7th order Cauer (75 dB)
  TSG8513: 8th order Chebychev
  TSG8514: 8th order Butterworth

  Notch:
  TSG8540: 6th order (Q = 7).

  High pass:
  TSG8530: 3rd order Cauer
  TSG8531: 6th order Cauer
  TSG8532: 6th Chebychev

  Bandpass:
  TSG8550: 6th order Cauer
  TSG8551: 8th order (Q = 35)

- Semi Custom
  TSGF08/Customer identification.

TYPICAL APPLICATIONS:

- Telecommunications.
- Robotic.
- Sonar detection.
- Data acquisition (before A/D and after D/A conversions).
- Speech processing.
- Audio processing.
- Instrumentation (portable, medical,...).
- Spectrum analysis (noise, speech)
- Industrial applications (process control,...).
- All low frequency classical applications where low power and small sizes are researched.

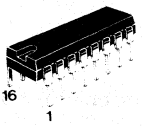
* The standard circuits TSG8512, TSG8532 and TSG8540 are respectively equivalent to R5609, R5611 and R5612 (Reticon).

LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

(Order: up to eight)

CASE CB-79

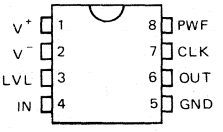


CASE CB-98

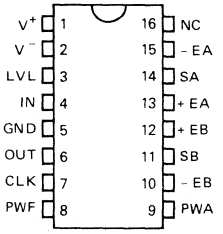
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix)
and Cerdip package (J suffix)
are also available

PIN ASSIGNMENT



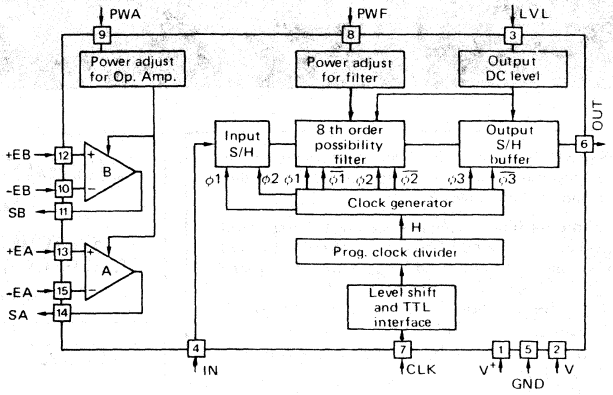
8 pins: FILTER ONLY



16 pins: FILTER+2 OP-AMPs

43, Avenue de l'Europe - 78140 VÉLIZY-VILLACOUBLAY - FRANCE - Tel. : (1) 39.46.97.19 - Telex TCSF 204780F - Telecopie : (1) 39.46.52.64

BLOCK DIAGRAM



PIN DESCRIPTION (8 pin package)
(minimal version : filter only)

Name	Type	N°	Function	Description
V^+	I	1	Positive supply	
V^-	I	2	Negative supply	
LVL	I	3	Output DC level adjustement	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed LVL pin is connected to GND.
IN	I	4	Filter input	
GND	I	5	General ground	
OUT	O	6	Filter output	
CLK	I	7	Clock input	TTL levels
PWF	I	8	Filter power adjustement	Filter power consumption can be choosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^- (or non connected).

PIN DESCRIPTION (16 pin package)
(extended version : filter + 2 op Amps)

Name	Type	N°	Function	Description
V^+	I	1	Positive supply	
V^-	I	2	Negative supply	
LVL	I	3	Output DC level adjustment	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed, LVL pin is connected to GND.
IN	I	4	Filter input	
GND	I	5	General ground	
OUT	O	6	Filter output	
CLK	I	7	Clock input	TTL levels
PWF	I	8	Filter power adjustment	Filter power consumption can be choosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^- (or non connected)
PWA	I	9	Op Amp power adjustment	Idem PWF but for Op Amp (PWA)
-EB	I	10	Inverting input Op Amp B	
SB	O	11	Output Op Amp B	
$^+$EB	I	12	Non inverting input Op Amp B	
$^+$EA	I	13	Non inverting input Op Amp A	
SA	O	14	Output Op Amp A	
$^-$EA	I	15	Inverting input Op Amp A	
NC		16	Non connected	

FUNCTIONAL DESCRIPTION

The filtering unit is formed by eight connectable switched capacitor integrators.
Each integrator can be specialized with capacitor fields and switching cells.
The interconnections between each integrator and the realization of the desired capacitors are achieved during the last step of the process to form the filter.
For this operation, the aluminium interconnection mask is used (like in gate-arrays structures).

The clock generator delivers the different phases needed for the internal switching. The internal clock is performed through an internal mask programmable divider which adapts if required the external clock (given from a cristal oscillator for example) to obtain the filter clock. As the clock input is TTL compatible, level shifts are used inside the chip to obtain the correct voltage swings.

The output sample and hold buffer is connected to the filter output and so allows a low impedance signal delivery.

The output DC level adjustment is also possible with an external voltage source (obtained for example through a resistor divider).

Two uncommitted general purpose operational amplifiers are also available.
They can be used by the customer to implement other analog functions (for example gain, pre or post filtering...).

Power adjustment is possible for the filter unit and for the two free op. amps. This facility is performed with a resistor connected between the V^+ supply (or ground) and the power adjustment pins. So the consumption of the structure can be chosen to adapt it to the application. The stand-by mode can be obtained by connecting the corresponding pins to the V^- supply (or non connected).

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Positive supply voltage	V^+	- 0.15 to + 7	V
Negative supply voltage	V^-	- 7 to + 0.15	V
Voltage to any pin (exept for ground)	V	V^- - 0.3 to V^+ + 0.3	V
DC current per pin (except for supplies)	Io	150	mA
Temperature Operating t° range Storage t° range	 T oper T stg	 - 60 to + 130 - 60 to + 150	°C

ELECTRICAL CHARACTERISTICS FOR FILTER ONLY $T = 25°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Positive supply voltage	V^+	4	5	6	V
Negative supply voltage	V^-	- 6	- 5	- 4	V
Output voltage swing	V_{out}	V^- + 0.5		V^+ - 1.5	V_{pp}
Input voltage (with filter gain = OdB)	V_{in}	V^- + 0.5		V^+ - 1.5	V_{pp}
Bias current on PWF (stand by mode by connecting PWF to V^-) (or non connected)	I_{PWF}	50		250	µA
TTL clock input "0"	V_{IL}			+ 0.8	V
TTL clock input "1"	V_{IH}	2			V
External clock pulse width	t_{cp}	80			nS
Input resistance	R_{IN}	1	3		MΩ
Input capacitance	C_{IN}			20	pF
Output resistance	R_{OUT}		10		Ω
Load capacitance	C_L			100	pF
Load resistance	R_L	0.1	1		KΩ

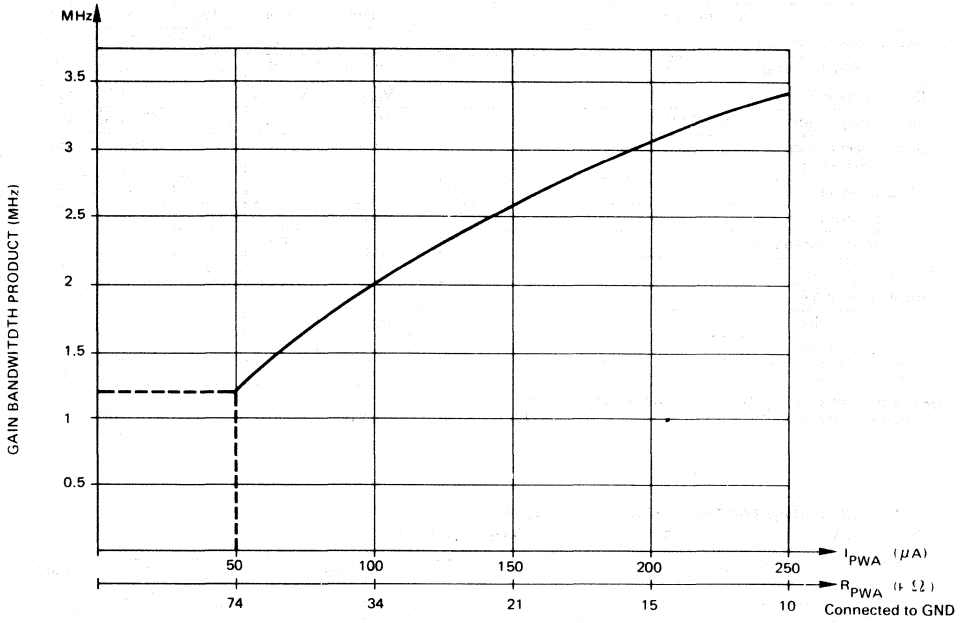
NB) With single supply (0 - 10 V) : same specifications
With single supply (0 - 5 V) : specifications can be asked to Thomson Semiconducteurs commercial office

ELECTRICAL CHARACTERISTICS FOR OP. AMP.

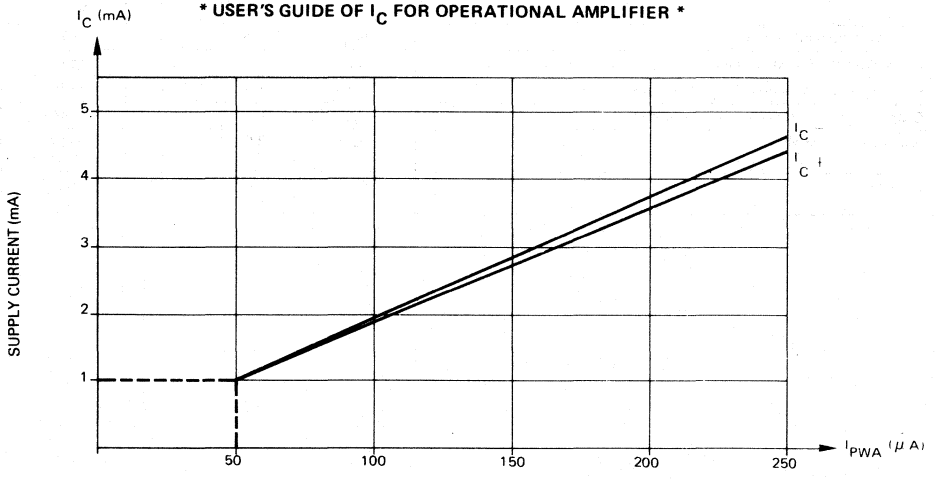
$V^+ = +5$ V $V^- = -5$ V $T = 25$ °C $R_L = 2$ KΩ $I_{PWA} = 100$ µA

Characteristic	Symbol	Typ	Tested limits	Unit
DC open loop gain (without load)	G_o^+ G_o^-	75 75	60 60	dB (min) dB (min)
Gain-band with product (without load)	G_o BW	2	1	MHz (min)
Input offset voltage (without load)	V_{ioFF}	± 5	± 10	mV (max)
Output swing	V_{ouT}	- 4.5 3.5	- 4.2 3.5	V (min) V (max)
Input bias current (without load)	I_{bias}	± 5	± 10	nA (max)
Supply rejection (without load)	SVR	65	60	dB (min)
Common mode rejection $V_{CM} = 1$ V (without load)	CMR	65	60	dB (min)
Output short circuit current (without load)	I_{os}	100		mA
Power consumption	P_a + -	2.6 2.6	3.2 3.2	mA (max) mA (max)
Slew rate	SR + -	5 6		V/µS V/µS

*** USER'S GUIDE OF I_{PWA} AND R_{PWA} FOR OPERATIONAL AMPLIFIER ***



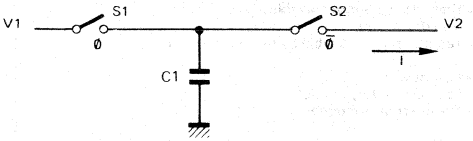
*** USER'S GUIDE OF I_C FOR OPERATIONAL AMPLIFIER ***



SWITCHED CAPACITOR FILTER GENERALITIES

BASIC PRINCIPLE

These are active filters in which resistors are replaced by capacitors which are switched with a frequency, named sampling frequency (Fs), as follows:



The two switches (S_1 and S_2) are controlled by two complementary and non overlapping clock phases.

During the phase $\varnothing = 1$ (S_1 on, S_2 off), the charge stored in C_1 is:

$$Q_1 = C_1 V_1 \quad (1)$$

During the phase $\overline{\varnothing} = 1$ (S_1 off, S_2 on), the charge stored in C_2 becomes:

$$Q_2 = C_1 V_2 \quad (2)$$

During a complete clock period $T_S = \frac{1}{F_S} = \varnothing + \overline{\varnothing}$,

the transferred charge is:

$$\Delta Q = Q_1 - Q_2 = C_1 (V_1 - V_2) \quad (3)$$

During a period T_S, this charge flow is equivalent to a current I, such as:

$$\Delta Q = C_1 (V_1 - V_2) = I \cdot T_S \quad (4)$$

and so: $I = C_1 \cdot F_S (V_1 - V_2) = \frac{C_1 (V_1 - V_2)}{T_S}$ (5)

Comparing (5) with Ohm law applied to a resistance:

$$I = \frac{V_1 - V_2}{R} \quad (6)$$

The equivalent resistor is:

$$R = Req = \frac{T_S}{C_1} \quad (7)$$

Then, with (7), a RC product becomes:

$$Req.C = \frac{C}{C_1} \cdot T_S \quad (8)$$

WHY THIS TECHNIQUE CAN BE USED TO REPLACE CLASSICAL ACTIVE FILTERS?

In active filters, the time constants are fixed by RC products. But the component values R and C used are absolutely uncorrelated, so trimmings are often needed to obtain an accurate template.

On the other hand, in switched capacitor networks, only capacitor ratios are used. These ratios are obtained with capacitors integrated on the same chip. The available accuracy is 0.1% to 0.5% whatever the temperature conditions may be.

As the time constants are fixed by capacitor ratios, fully integrated filters are achievable without trimming. In addition, as shown in (8), the time constant RC is proportional to the sampling period T_S. Another important property of switched capacitor filters is that cut-off frequency can be shifted by shifting the sampling clock without any change on the shape of response curves.

SWITCHED CAPACITOR ACTIVE FILTER FEATURES

The main features are summarized in the following table:

Key points	Results
• Monolithic filter • Every time constant defined by : — capacitor ratios — clock frequency	• Board size reduction • Precise template. • Stability in temperature and time • High order filter achievable • No adjustment • Template transposable by tuning the clock
• Fully integrated filters with CMOS technology	• Low power • Ease and safety of use • No external component
• Switched capacitor networks are sampled and hold systems	• Antialiasing pre-filtering is needed if the input signal is wide band (See Application note) • Smoothing post-filtering may be used to avoid spectral rays around the sampling frequency (See Application note)

HOW TO CHOOSE HIS TYPE OF FILTER?

A number of nomographs, tables and curves provide, for each type of function and according to its order, the amplitude response curves, the phase response curves, the group delay curves, and also the pulse and step responses. All these characteristics, and a few others, are summarized in the following table:

Kind of performance \ Kind of filter	Butterworth	Legendre	Chebychev	Bessel	Cauer
Cut-off, abruptness for a given order	oo	o	**	ooo	***
Regularity of the "amplitude - frequency" curve	***	**	Ripple within the passband/regular within the notch	**	Ripple within the passband and the notch
Regularity of the group Delay	*	o	oo	***	ooo
Sensitivity	**	**	o	**	oo
Transient condition distortions	**	**	oo	***	ooo
Transmission zeros	None	None	None	None	Yes
Required overvoltage factors	Very low	Low	Medium	Medium	High

ooo : Very mediocre
oo : Mediocre
o : Medium

*** : Excellent
** : Very good
* : Good

We will keep in mind the following:

- the BUTTERWORTH filters are interesting because of the regularity of their passband (no ripple) but their cut-off is not very abrupt,
- the LEGENDRE filters associate a convenient regularity of the amplitude response curve with a cut-off abruptness and a transient behaviour that are of good quality,
- the CHEBYCHEV filters present, at least within the first octave, an abrupt cut-off, but their transient behaviour is not performing,
- the BESSEL filters present a very good transient behaviour (constant group delay in passband), but their cut-off is not very abrupt,
- the CAUER filters allow an extremely abrupt cut-off to be obtained, but their group delay regularity is mediocre. They present transmission zeros.

CUT-OFF FREQUENCY DEFINITION

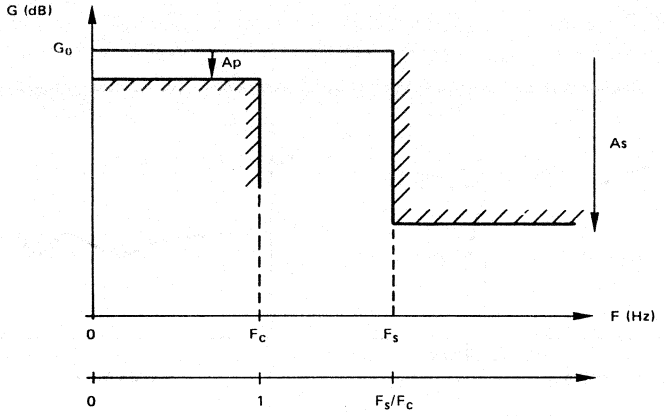


FIGURE 1 – DESIGN SPECIFICATIONS

The cut-off frequency Fc is the passband limit frequency as defined on the design specifications above mentioned.

The maximum value of the attenuation variation in the passband: Ap is 3 dB for Butterworth, Bessel and Legendre filters (figure 2a), and is called passband ripple for Chebychev (figure 2b) and Cauer filters (figure 2c).

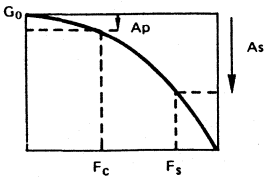


FIGURE 2a

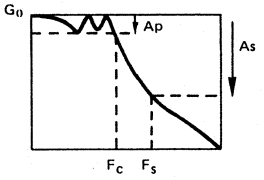


FIGURE 2b

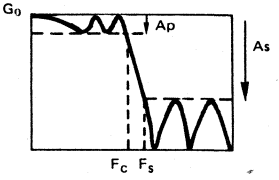
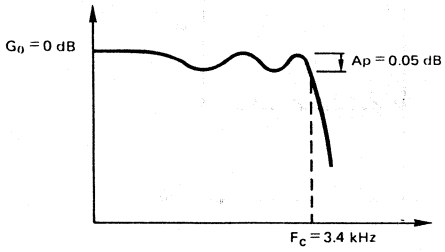


FIGURE 2c

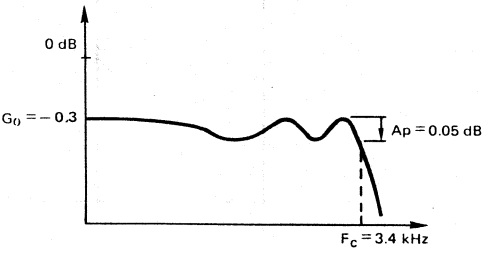
The passband ripple is design dependant and between 0.05 dB and 0.2 dB with TSG85XX standard filters.

The parameter G_0 called passband gain is the maximum value of the gain in the passband, and may have low variation from part to part:

Example:
TSG8510 with Fe = 256 kHz → Fc = 3.4 kHz
G_0 min = - 0.3 dB
G_0 max = 0 dB
Ap = 0.05 dB



FILTER No. 1



FILTER No. 2

This two cases show that the two filters TSG8510 (No. 1 and No. 2) has the same cut-off frequency with different values of gain :
- 0.05 dB for filter No. 1
- 0.35 dB for filter No. 2

The passband ripple remains constant, only the frequency response curve is shifted with G_0 variation.

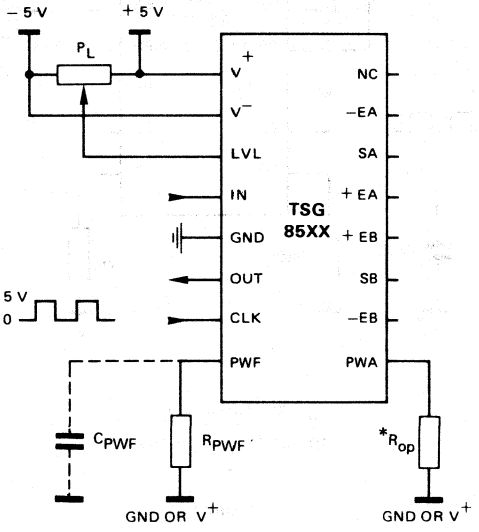
TYPICAL APPLICATION

Typical use of the M.P.F. (Figure 3)

The M.P.F is fed in dual supply: ±5 V.
The adjustment of the DC output level of the M.P.F is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F). If no output DC adjustment is required, the LVL pin can be directly connected to GND.
The consumption of the filter can be also adjusted by means of an external resistance connected between V^+ (or GND) and the PWF pin of the circuit.
The consumption can thus be chosen to match the particular application.

The stand-by mode is obtained by strapping the PWF pin to V^- (or non connected).
The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V^- (or non connected).
The clock levels are TTL, but CMOS levels are accepted.
With these previous conditions, the output linear dynamic range of the M.P.F is about 8 V, between − 4.5 V and +3.5 V.

A capacitor C_{PWF} can be added in parallel with R_{PWF} in order to improve the clock feedthrough rejection: (Typical value C_{PWF} = 33 pF).



P_L = 20 kΩ (multiturn)

10 kΩ ≤ R_{PWF}, R_{op} ≤75 kΩ

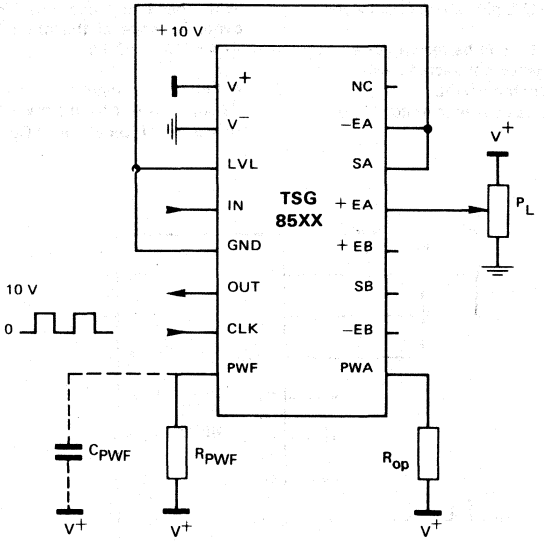
FIGURE 3

* If the OP AMPS are not used, R_{op} must not be connected between PWA and GND.

Use of the M.P.F. with 0-10 V (Figure 4)

The M.P.F is fed in single supply: 0-10 V.
In this case, V^- is the reference ground of the circuit and GND must be adjusted to +5 V by means of the potentiometer P_L $((V^+ - V^-)/2)$.
The adjustments of the DC output level of the M.P.F, of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.

The high level of the clock must be at least 1.4 V upper the GND level.
With these previous conditions, the output linear dynamic range of the M.P.F is about 8 V between 0.5 and 8.5 V.



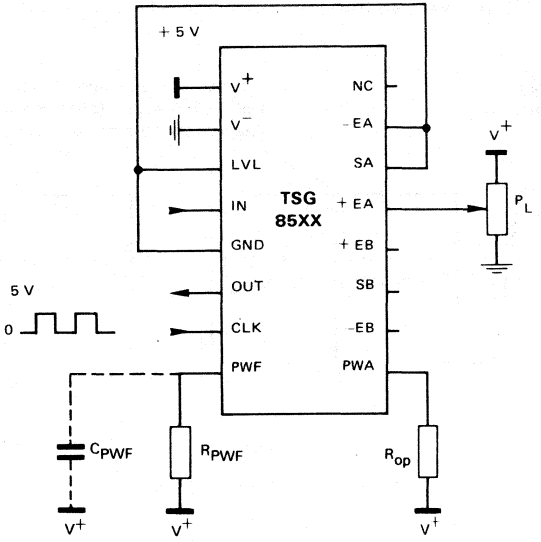
$P_L = 20\ k\Omega$ (multiturn)

$10\ k\Omega \leqslant R_{PWF}, R_{op} \leqslant 75\ k\Omega$

FIGURE 4

Use of the M.P.F. with 0-5 V (Figure 5)

The M.P.F is fed in single supply: 0-5 V.
In this case, V^- is the reference ground of the circuit and GND must be adjusted to + 2.5 V by means of the potentiometer P_L $((V^+ - V^-)/2)$.
The other adjustments are achieved exactly like previously except for bias resistances of the filter and of the operational amplifiers (Rf and Rop), whose must be exclusively to V^+.
The clock levels must be TTL levels. With these previous conditions, the output linear dynamic range of the M.P.F is about 2.2 V, between 1.2 and 3.4 V.



P_L = 20 kΩ (multiturn)

10 kΩ ≤ R_{PWF}, R_{op} ≤75 kΩ

FIGURE 5

Anti-aliasing and smoothing (Figure 6)

- Anti-aliasing: The switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (Fs) equal, at least, to the double of the upper frequency (Fc) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 6, where the entire spectrum to transmit appears around Fs, 2Fs, 3Fs,... and so on.

Thus, all spectrum components of the signal contained around these frequencies are transmited by the M.P.F., oppositively to the desired result.
To cancel the effects of this phenomenon, it is required, before all sampled system, to filter all the spectrum components of the input signal upper than Fs — Fc. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.

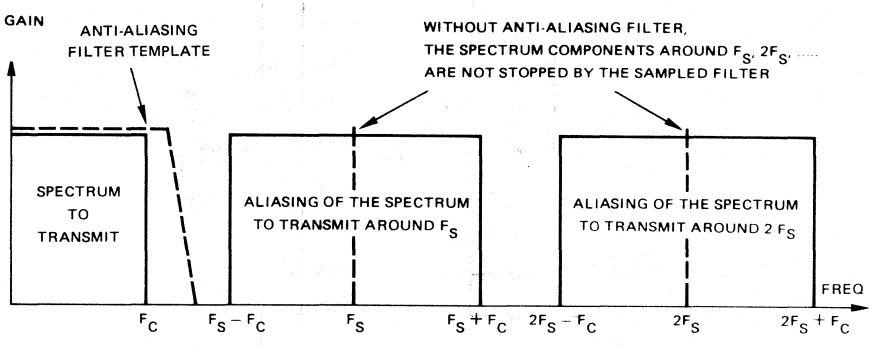


FIGURE 6

Phenomenon of the spectrum aliasing

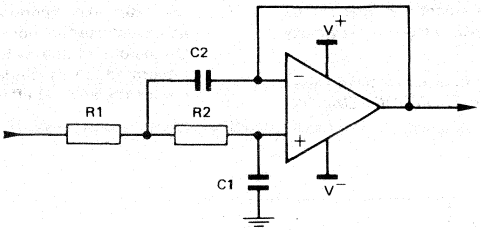
. Without anti-aliasing filter : Spectrum to transmit $\neq$ transmitted spectrum

. With anti-aliasing filter : Spectrum to transmit = transmitted spectrum

The selectivity of this filter depends upon the Fs/Fc ratio.

If Fs/Fc > 200 a RC filter (first order low-pass) is sufficient.

If Fs/Fc < 200, a SALLEN-KEY structure (second order low-pass) must be used. This structure and its relationships are described (figure 7). In these relationships, Fc is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and without overvoltage around it, ξ must have a value around 0.7.



$$C1 = \frac{\xi}{2\pi R1\ Fc}$$

$$(C1 = \xi^2 \cdot C2)$$

$$C2 = \frac{1}{2\pi\xi\ R1\ Fc}$$

R1 = R2 = arbitrary value

Fc = cut-off frequency for the antialiasing filter.
An optimal choice is Fc = 1.2 x cut-off frequency of the main filter

ξ = damping coefficient; the optimal value is 0.7

FIGURE 7

SALLEN-KEY structure (second order low-pass Filter) for anti-aliasing and smoothing.

N.B) If Fs/Fc < 2 (figure 8), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.

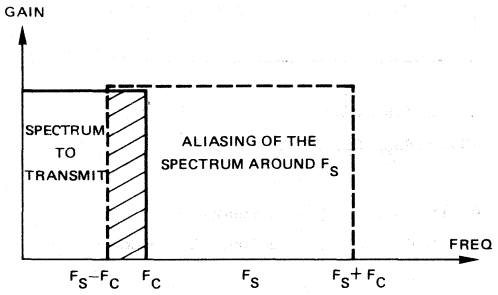
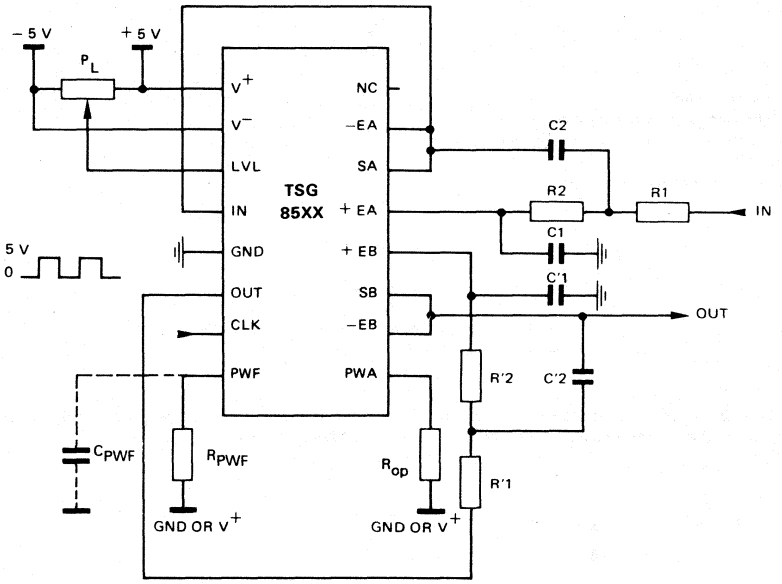


FIGURE 8

When Fs/Fc < 2, the spectrum components included between Fs-Fc and Fc and which are due to spectrum aliasing are not stopped by the sampled filter

- Smoothing: As the signal obtained at the output of the M.P.F is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (figure 7).
- Hardware implementation: In order to make easier anti-aliasing and smoothing, THOMSON SEMICONDUCTEURS has designed, on the even chip of the M.P.F, two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (figure 9).
On the other hand, in the most of M.P.F's, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around Fs.



$P_L = 20\ k\Omega$ (multiturn)

$10\ k\Omega \leq R_{PWF}, R_{op} \leq 75\ k\Omega$

R1, R2, C1, C2 } See anti-aliasing
R'1, R'2, C'1, C'2 } and smoothing considerations

FIGURE 9

M.P.F with anti-aliasing and smoothing filters

Nonetheless, if the application allows it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator,...).
In this case, the circuit shown figure 10 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described figure 7 (second order low-pass), in the same way as the corresponding relationships.

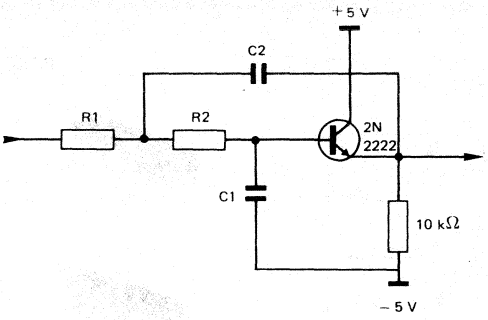
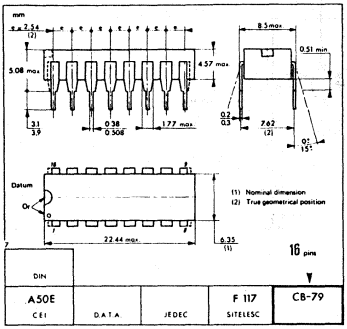


FIGURE 10

Second order low-pass Filter (SALLEN-KEY STRUCTURE) with a transistor replacing the operational amplifier.

PHYSICAL DIMENSIONS



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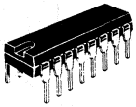
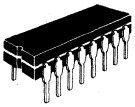
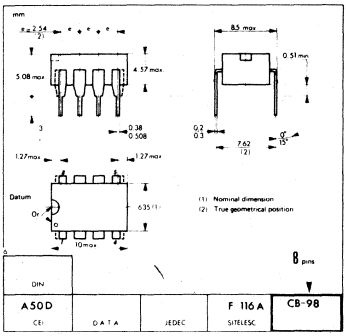


P SUFFIX
PLASTIC PACKAGE



J SUFFIX
CERDIP PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

TSG85XX

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

Those MPF standard products are HCMOS universal filter containing a mask programmable switched capcitor cascadable structure, and two uncommitted general purpose operational amplifiers. Every filter is obtained by TSG8508 base specialization; for pin description and free operational amplifier specifications, see TSG85XX general characteristics.

Here is the description of this family:

Part number	Function	Type	Order	Clock to cut-off freq. ratio
TSG8510	Low - Pass	Cauer	5	75.3
TSG8511	Low - Pass	Cauer	7	75.3
TSG8512	Low - Pass	Cauer	7	100
TSG8513	Low - Pass	Chebychev	8	60
TSG8514	Low - Pass	Butterworth	8	80
TSG8530	High - Pass	Cauer	3	320
TSG8531	High - Pass	Cauer	6	400
TSG8532	High - Pass	Chebychev	6	500
TSG8540*	Notch	Q = 7	6	930
TSG8550	Band - Pass	Cauer Q = 7	6	48
TSG8551	Band - Pass	Selective Q = 35	8	187.2

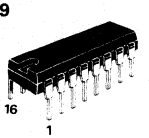
* Preliminary

Note: Except for TSG8551 (Go = 30 dB)
Go = 0 dB for all M.P.F.

LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER (STANDARD FILTER)

CASE CB-79



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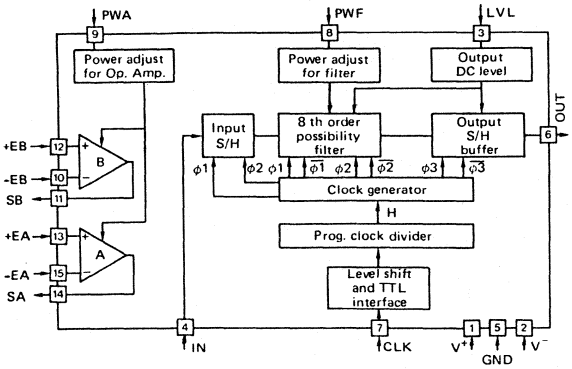
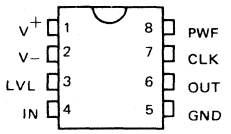
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix)
and Cerdip package (J suffix)
are also available

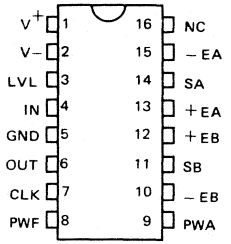
BLOCK DIAGRAM



PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

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NOTES

Printed in France

THOMSON COMPONENTS SEMICONDUCTEURS

TSG8510

MPF LOW PASS ELLIPTIC FILTER. CAUER TYPE. 5th ORDER

The TSG8510 is a HCMOS lowpass elliptic filter.

- CAUER type.
- 5th order.
- Stopband attenuation: 33 dB (typ).
- Passband ripple: 0.05 dB (typ).
- Clock to cut-off freq. ratio: 75.3.
- Clock frequency range: 1 to 1500 kHz.
- Cut-off frequency range: 13 Hz to 20 kHz.

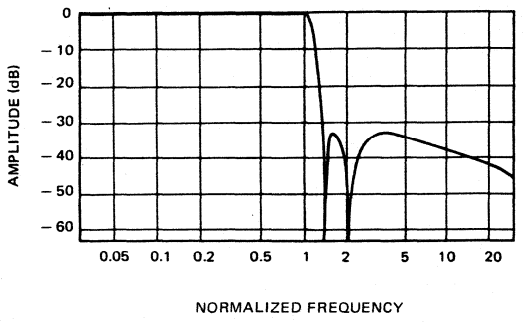
Ordering information:

- Plastic 16 pins package: TSG8510XP.
- Ceramic 16 pins package: TSG8510XC.
- Cerdip 16 pins package: TSG8510XJ.
- Plastic 8 pins package: TSG85101XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M: -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

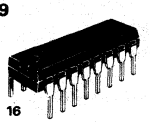
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

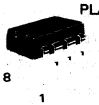
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-79



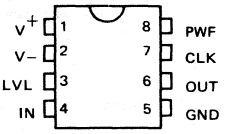
P SUFFIX
PLASTIC PACKAGE

CASE CB-98

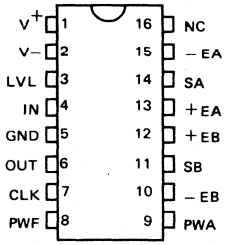


Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

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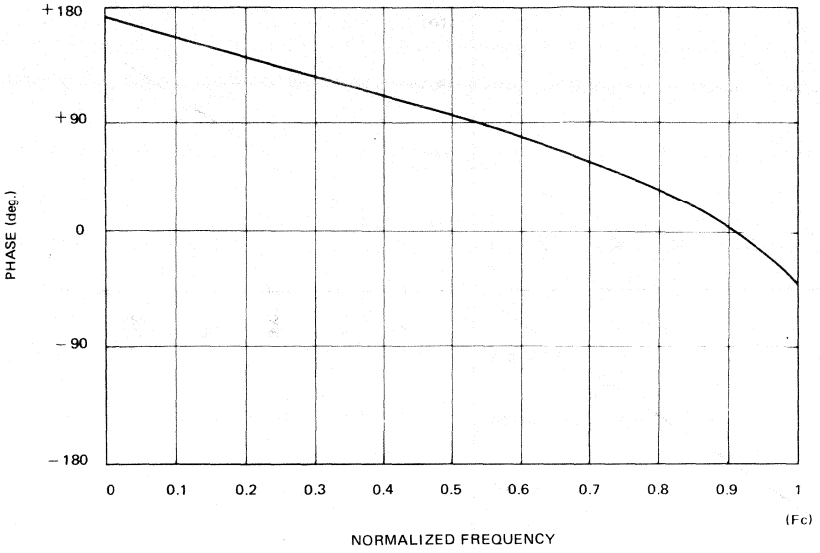
FILTER SPECIFICATIONS

Lowpass filter: TSG8510; Type: Cauer; Order: 5.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 kOhm, CL = 100 pF, $I_{PWF} = 100\ \mu A$

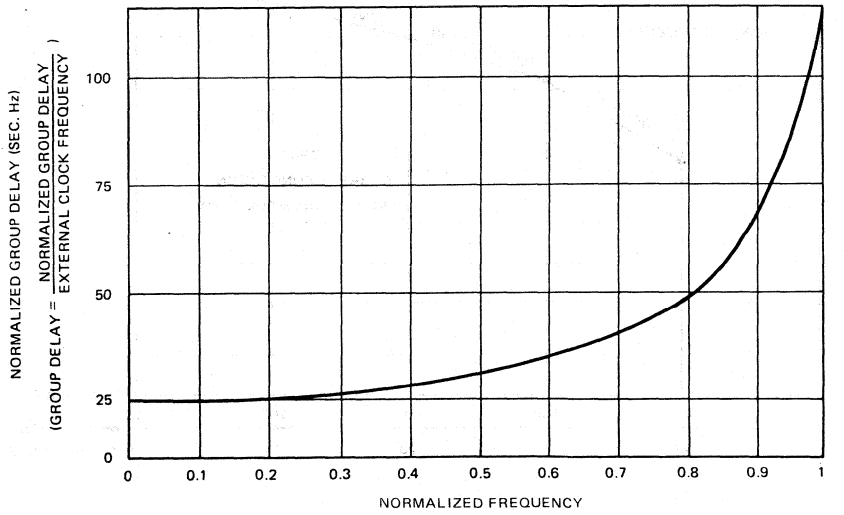
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1500 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	0.5 750 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	75.3 ± 1 %		—	
Cutoff frequency	Fc	0.013 20 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.05	0.4	dB (max)	Fe = 256 kHz
Stopband attenuation	As	33	32	dB (min)	Fe=256 kHz, F>1.37 Fc
Output DC offset voltage	Voff	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 60		mV	
Level gain	LG	3.3		—	
PWF resistance	R_{PWF}	10 72		kOhm (min) kOhm (max)	
Input current on PWF	I_{PWF}	50 250		μA (min) μA (max)	
V^+ supply current	I^+	3	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3	5	mA (max)	Ipwa = 0 μA
V^+ supply rejection ratio	$PSRR^+$	35		dB	Fe = 256 kHz
V^- supply rejection ratio	$PSRR^-$	55		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	89		μV rms	BW = 3.4 kHz
Signal to noise ratio	SNR	87		dB	Fe = 256 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation As > 32 dB for F > 1.37 Fc
(with Ipwf = 250 μA) - passband ripple : Ap = 0.8 dB
- passband gain: $G_o = -0.4$ dB

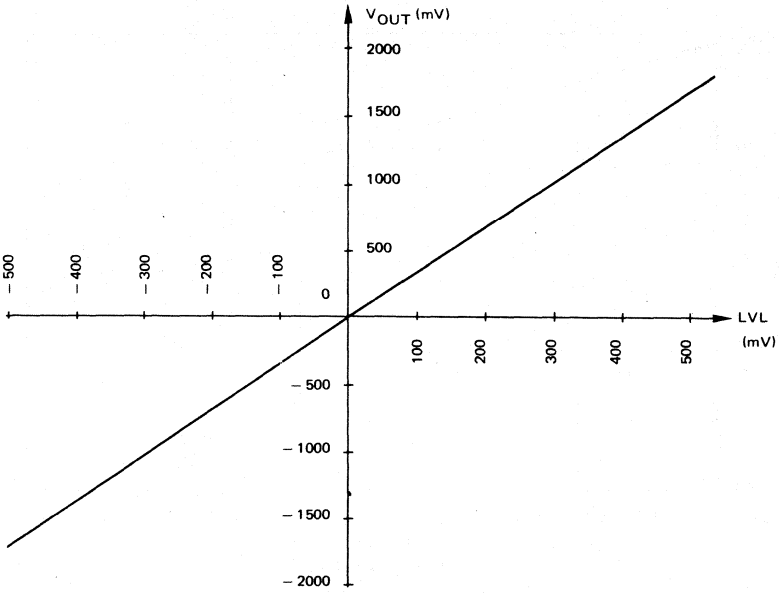
PHASE RESPONSE CURVE (IN PASSBAND)



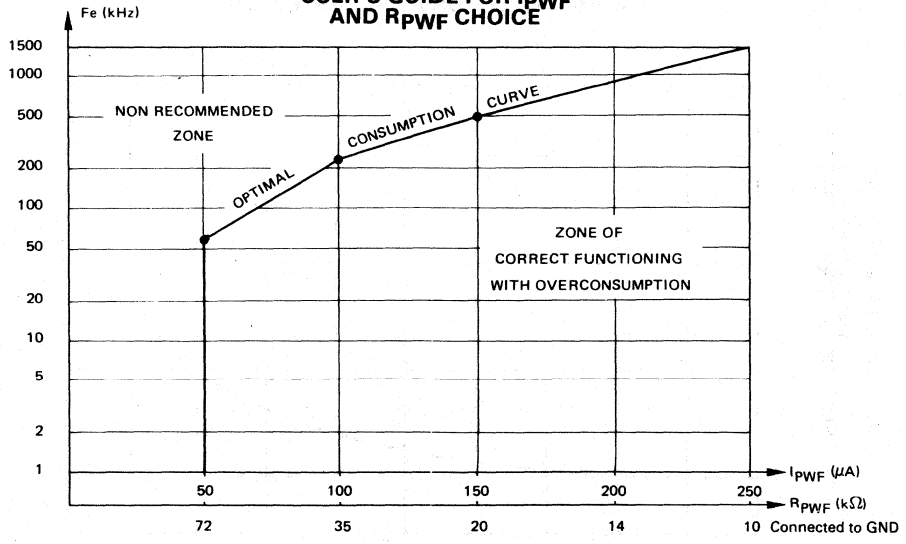
GROUP DELAY CURVE (IN PASSBAND)



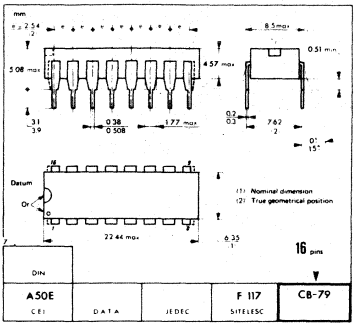
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



PHYSICAL DIMENSIONS



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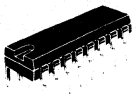
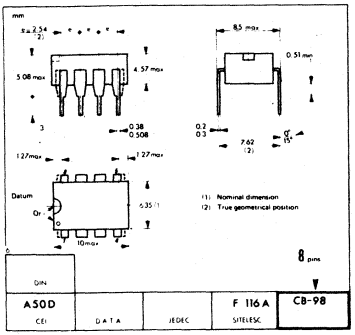


P SUFFIX
PLASTIC PACKAGE



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P SUFFIX
PLASTIC PACKAGE

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NOTES

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HOMSON COMPONENTS EMICONDUCTEURS

TSG8511

MPF LOW PASS ELLIPTIC FILTER. CAUER TYPE. 7th ORDER

The TSG8511 is a HCMOS lowpass elliptic filter

- CAUER type.
- 7th order.
- Stopband attenuation: 55 dB (typ).
- Passband ripple: 0.1 dB (typ).
- Clock to cut-off freq. ratio: 75.3.
- Clock frequency range: 1 to 1300 kHz.
- Cut-off frequency range: 13 Hz to 17.3 kHz.

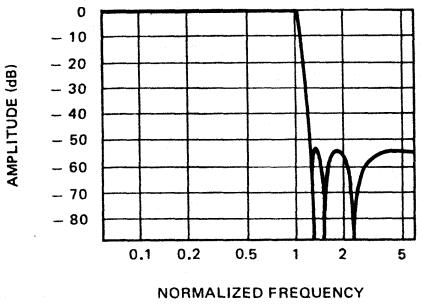
Ordering informations:

- Plastic 16 pins package: TSG8511XP.
- Ceramic 16 pins package: TSG8511XC.
- Cerdip 16 pins package: TSG8511XJ.
- Plastic 8 pins package: TSG85111XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

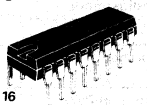
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-79

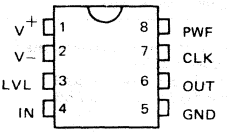


P SUFFIX
PLASTIC PACKAGE

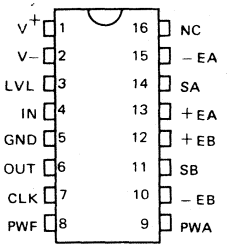
CASE CB-98

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP. AMPs

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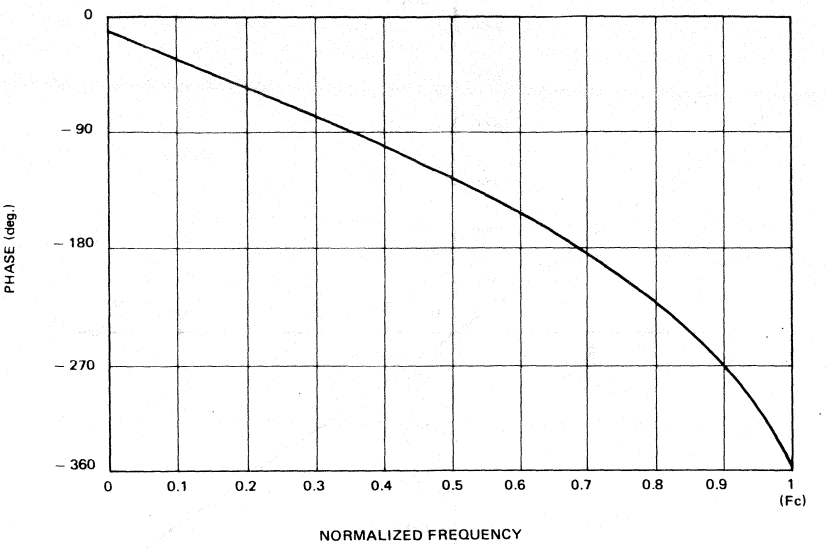
FILTER SPECIFICATIONS
Lowpass filter: TSG8511; Type: Cauer; Order: 7.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μA

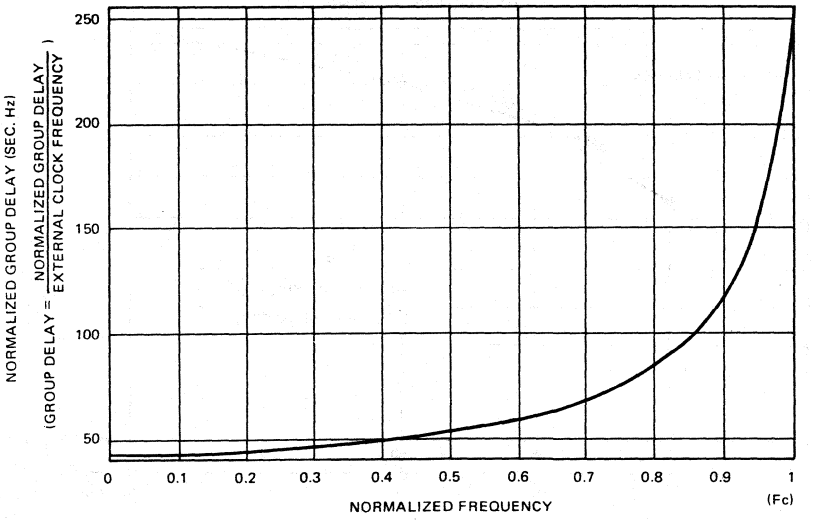
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1300 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	0.5 650 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	75.3 ± 1 %		—	
Cutoff frequency	Fc	0.013 17.3 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.1	0.5	dB (max)	Fe = 256 kHz
Stopband attenuation	As	55	50	dB (min)	Fe = 256 kHz F>1.3 Fc ;
Output Dc offset voltage	V off	± 150	± 300	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 64		mV	
Level gain	LG	-4.7		—	
PWF resistance	R_{PWF}	10 72		K Ohm (min) K ohm (max)	
Input current on PWF	I_{PWF}	50 250		µA (min) µA (max)	
V+ supply current	I+	3.5	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.5	5	mA (max)	Ipwa = 0µA
V+ supply rejection ratio	PSRR +	32		dB	Fe = 256 kHz
V- supply rejection ratio	PSRR-	47		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input Capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp-p (max)	
Output noise	Vn	158		µV rms	BW = 3.4 kHz
Signal to noise ratio	SNR	82		dB	Fe = 256 kHz Vin = 2 Vrms

(*) At maximum Fe: stopband attenuation AS > 50 dB for F>1.3 Fc
(with Ipwf = 250µA)
passband ripple : Ap = 0.5 dB
passband gain : G_o = -0.7 dB

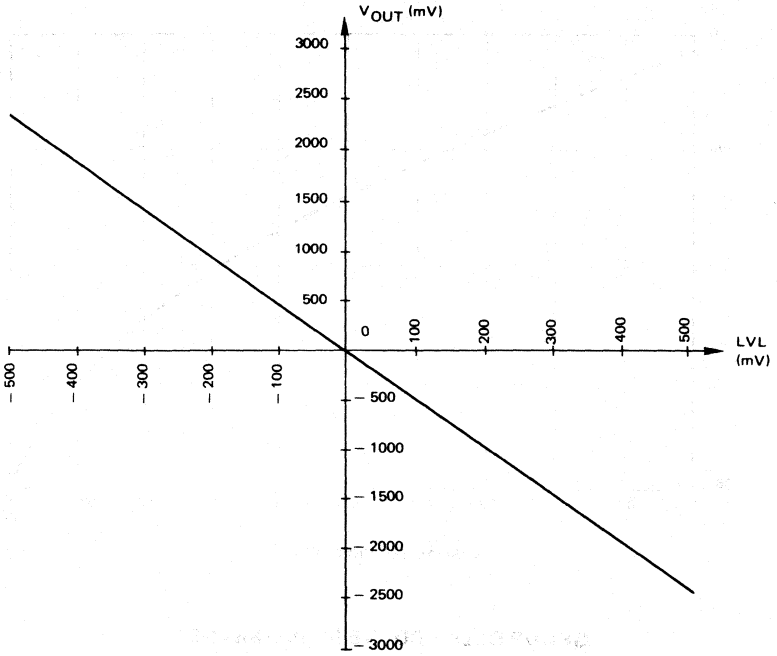
PHASE RESPONSE CURVE (IN PASSBAND)



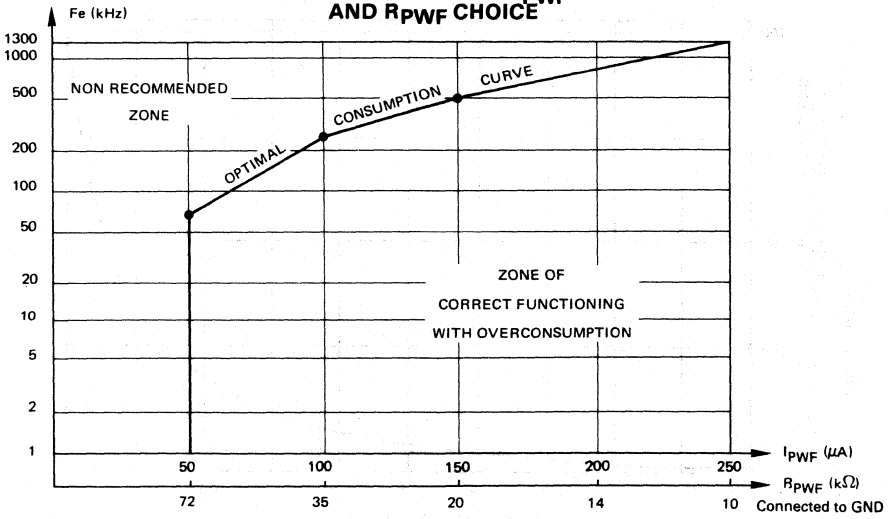
GROUP DELAY CURVE (IN PASSBAND)



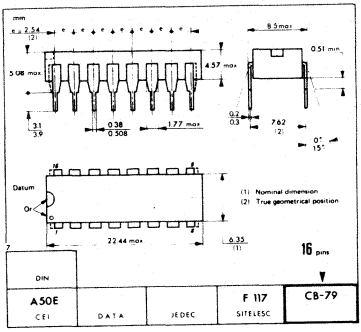
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



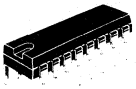
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



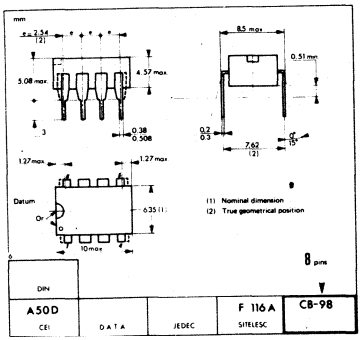
PHYSICAL DIMENSIONS



CASE CB-79



P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

THOMSON COMPONENTS SEMICONDUCTEURS

TSG8512

MPF LOW PASS ELLIPTIC FILTER. CAUER TYPE. 7th ORDER

The TSG8512 is a HCMOS lowpass elliptic filter.

- CAUER type.
- 7th order.
- Stopband attenuation: 85 dB (typ).
- Passband ripple: 0.15 dB (typ).
- Clock to cut-off freq. ratio: 100.
- Clock frequency range: 1 to 2000 kHz.
- Cut-off frequency range: 10 Hz to 20 kHz.

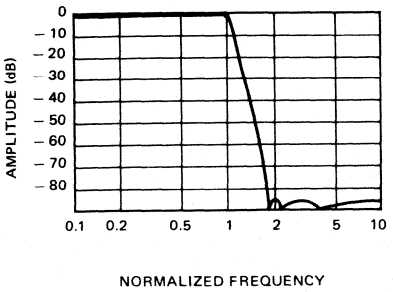
Ordering informations:

- Plastic 16 pins package: TSG8512XP.
- Ceramic 16 pins package: TSG8512XC.
- Cerdip 16 pins package: TSG8512XJ.
- Plastic 8 pins package: TSG85121XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

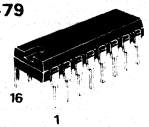
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-79

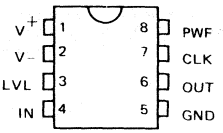


CASE CB-98

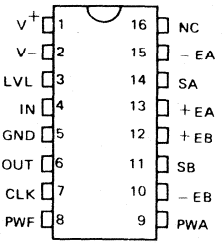
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP. AMPs

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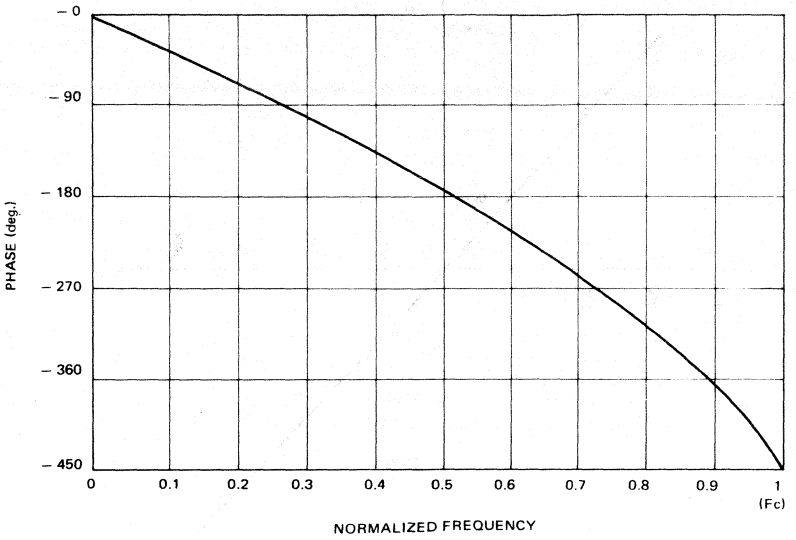
FILTER SPECIFICATIONS

Lowpass filter: TSG8512; Type: Cauer; Order: 7.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μ A

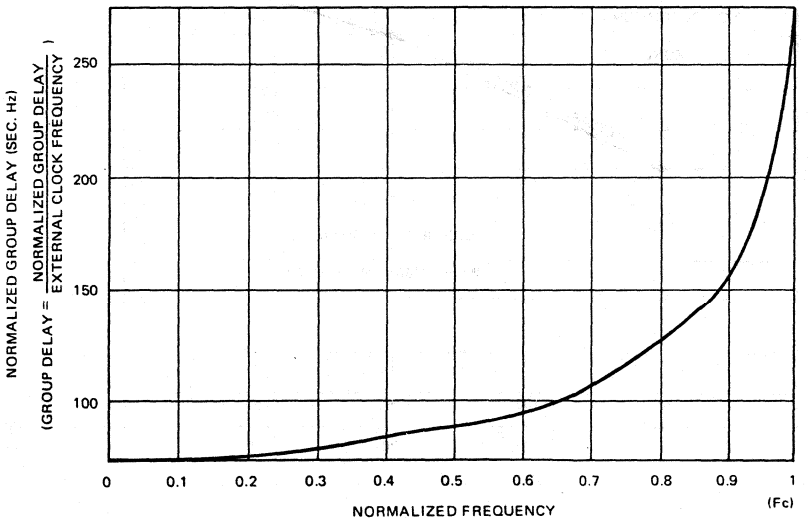
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 2000 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	0.5 1000 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	100 ± 1 %		—	
Cutoff frequency	Fc	0.010 20 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.15	0.5	dB (max)	Fe = 100 kHz
Stopband attenuation	As	85	75	dB (min)	Fe = 100 kHz, F > 1.8 Fc
Output DC offset voltage	Voff	± 150	± 250	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 22,5		mV	
Level gain	LG	- 11.1		—	
PWF resistance	R_{PWF}	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	I_{PWF}	50 250		μ A (min) μ A (max)	
V^+ supply current	I^+	3.5	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3.5	5	mA (max)	Ipwa = 0 μ A
V^+ supply rejection ratio	$PSRR^+$	20		dB	Fe = 200 kHz
V^- supply rejection ratio	$PSRR^-$	35		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	112		μ V rms	BW = 1 kHz
Signal to noise ratio	SNR	85		dB	Fe = 100 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation : As > 62 dB for F > 1.8 Fc
(with Ipwf = 250 μ A) - passband ripple : Ap = 0.6 dB
- passband gain : G_o = - 0.4 dB

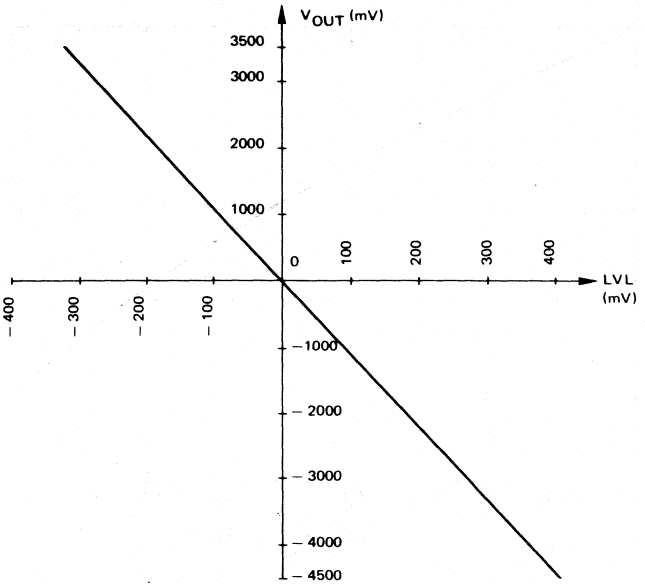
PHASE RESPONSE CURVE (IN PASSBAND)



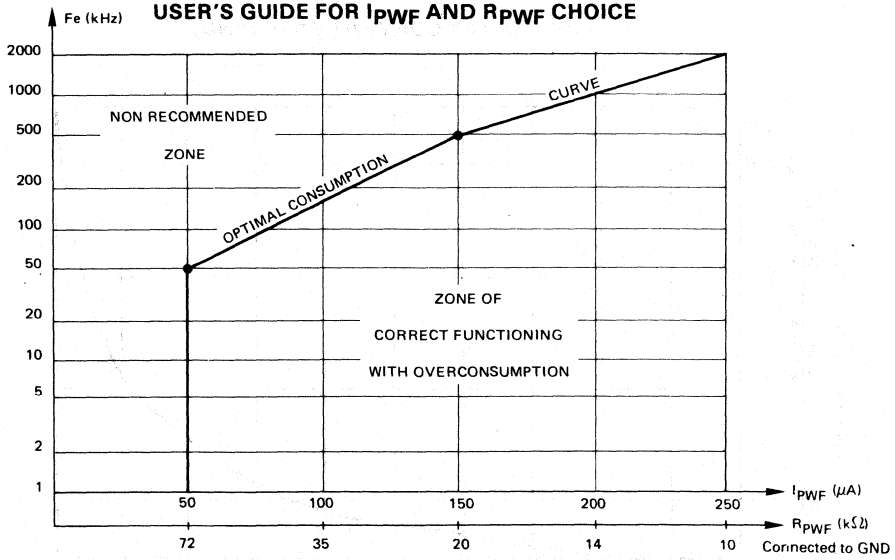
GROUP DELAY CURVE (IN PASSBAND)



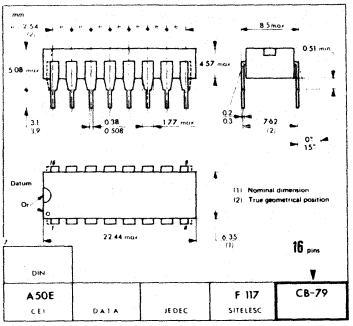
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



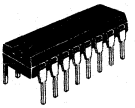
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



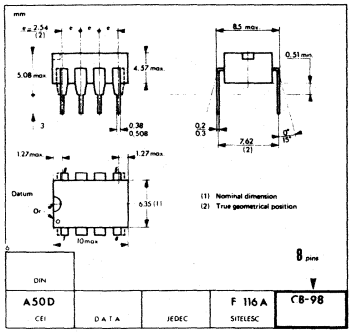
PHYSICAL DIMENSIONS



CASE CB-79



P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

HOMSON COMPONENTS
EMICONDUCTEURS

TSG8513

MPF LOW PASS POLYNOMIAL FILTER. CHEBYCHEV TYPE. 8th ORDER

The TSG8513 is a HCMOS lowpass polynomial filter.

- CHEBYCHEV type.
- 8th order.
- Stopband attenuation: 69 dB (typ). at 2 x F_C
- Passband ripple: 0.15 dB (typ).
- Clock to cut-off freq. ratio: 60.
- Clock frequency range: 1 to 1500 kHz.
- Cut-off frequency range: 16 Hz to 25 kHz.

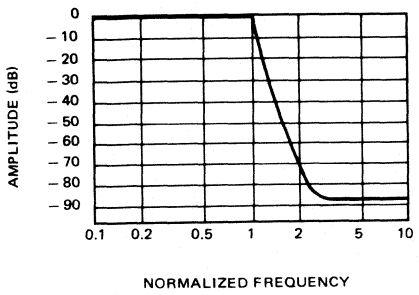
Ordering informations:

- Plastic 16 pins package: TSG8513XP.
- Ceramic 16 pins package: TSG8513XC.
- Cerdip 16 pins package: TSG8513XJ.
- Plastic 8 pins package: TSG85131XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M: -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

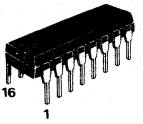
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

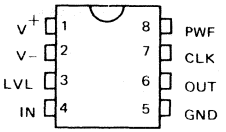
CASE CB-79



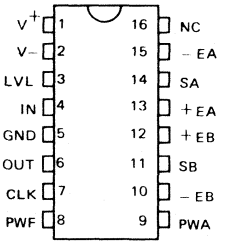
CASE CB-98 **P SUFFIX** PLASTIC PACKAGE

Ceramic package (C Suffix) and Cerdip package (J Suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP. AMPs

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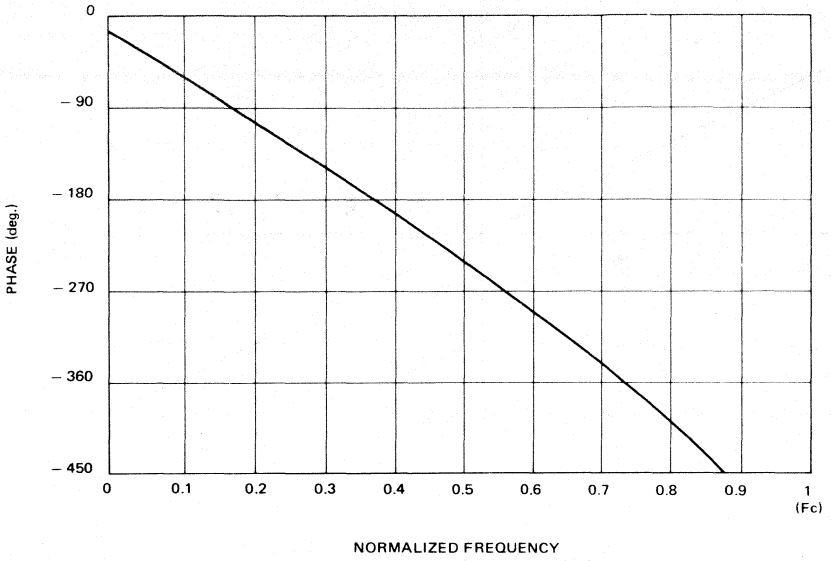
FILTER SPECIFICATIONS
Lowpass filter: TSG8513; Type: Chebychev; Order: 8.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μ A

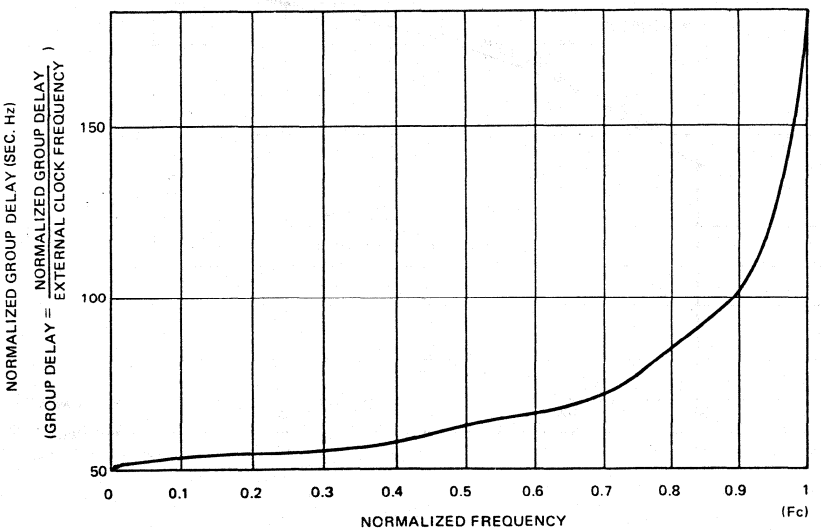
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1500 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	0.5 750 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	60 ± 1 %		—	
Cutoff frequency	Fc	0.016 25 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.15	0.5	dB (max)	Fe = 60 kHz
Stopband attenuation	As	69	65	dB (min)	Fe = 60 kHz, F>2 Fc
Output DC offset voltage	Voff	± 100	± 250	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 100		mV (max)	
Level gain	LG	- 2.5		—	
PWF resistance	R_{PWF}	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	I_{PWF}	50 250		μ A (min) μ A (max)	
V^+ supply current	I^+	3.8	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3.8	5	mA (max)	Ipwa = 0 μ A
V^+ supply rejection ratio	$PSRR^+$	25		dB	Fe = 120 kHz
V^- supply rejection ratio	$PSRR^-$	40		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	107		μ V rms	BW = 1 kHz
Signal to noise ratio	SNR	85		dB	Fe = 60 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation : As>55 dB for f>2 Fc
(with Ipwf = 250 μ A) - passband ripple : Ap = 0.8 dB
- passband gain : $G_o = -0.6$ dB

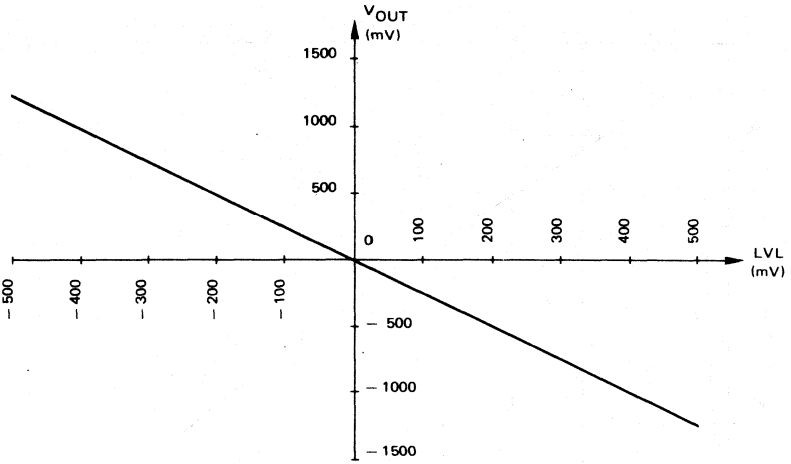
PHASE RESPONSE CURVE (IN PASSBAND)



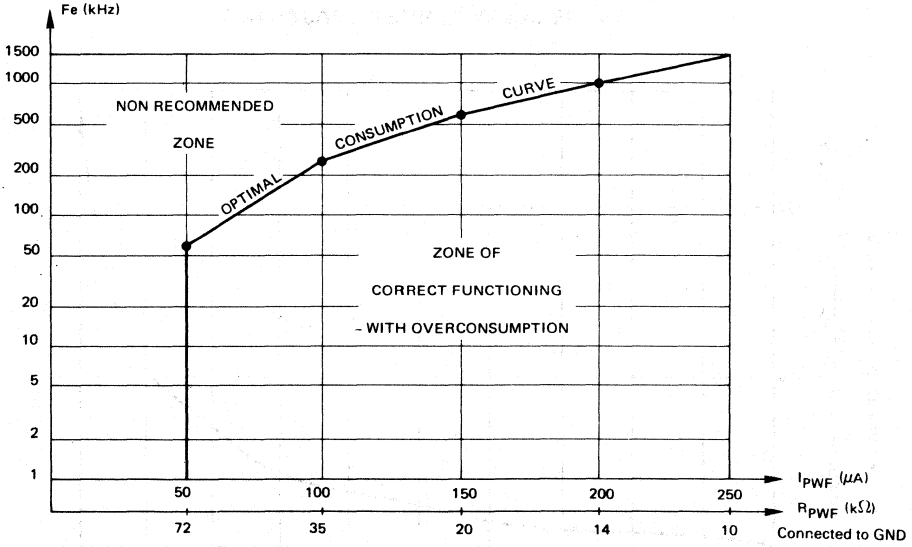
GROUP DELAY CURVE (IN PASSBAND)



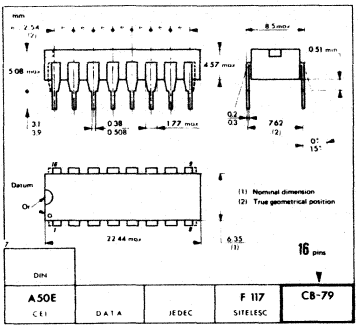
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



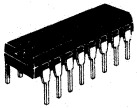
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



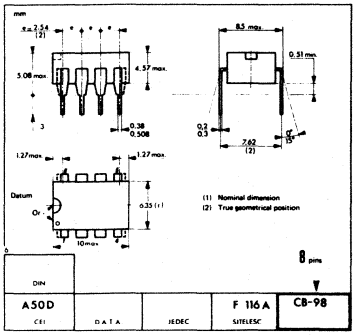
PHYSICAL DIMENSIONS



CASE CB-79



P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

THOMSON COMPONENTS MICONDUCTEURS

TSG8514

MPF LOW PASS POLYNOMIAL FILTER. BUTTERWORTH TYPE. 8th ORDER

The TSG8514 is a HCMOS lowpass polynomial filter.

- BUTTERWORTH type.
- 8th order.
- Stopband attenuation: 74 dB (typ). at 3.6 x F_C
- Passband ripple: maximally flat
- Clock to cut-off freq. ratio: 80.
- Clock frequency range: 1 to 1000 kHz.
- Cut-off frequency range: 12.5 Hz to 12.5 kHz.

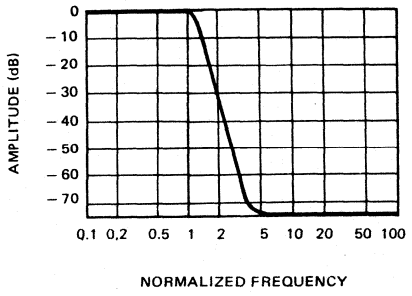
Ordering informations:

- Plastic 16 pins package: TSG8514XP.
- Ceramic 16 pins package: TSG8514XC.
- Cerdip 16 pins package: TSG8514XJ.
- Plastic 8 pins package: TSG85141XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M: -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

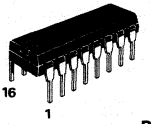
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-79

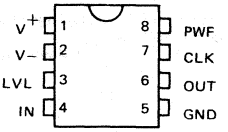


CASE CB-98

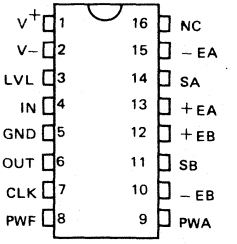
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

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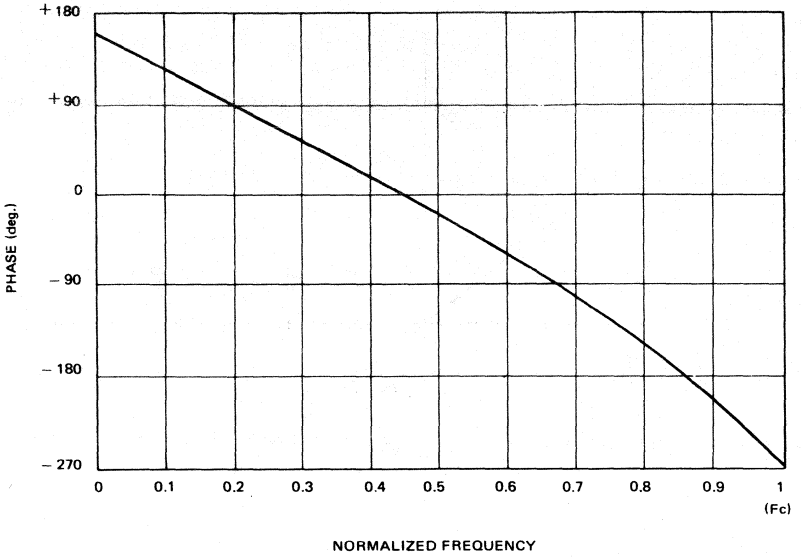
FILTER SPECIFICATIONS

Lowpass filter: TSG8514; Type: Butterworth; Order: 8.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μ A

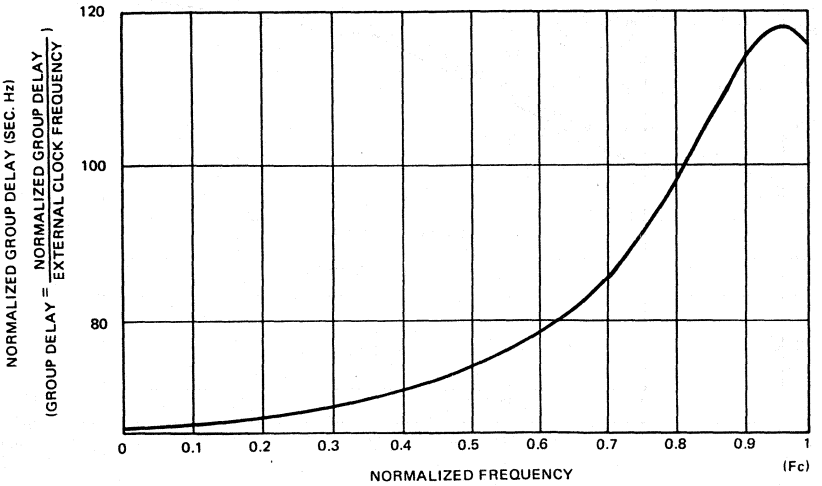
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1000 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	0.5 500 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	80 ± 1 %		—	
Cutoff frequency	Fc	0.0125 12.5 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	maxi mally Flat		dB (max)	Fe = 80 kHz
Stopband attenuation	As	74	68	dB (min)	Fe = 80 kHz, F>3.6 Fc
Output DC offset voltage	Voff	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 100		mV	
Level gain	LG	- 2		—	
PWF resistance	R_{PWF}	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	I_{PWF}	50 250		μ A (min) μ A (max)	
V^+ supply current	I^+	3.8	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	3.8	5	mA (max)	Ipwa = 0 μ A
V^+ supply rejection ratio	$PSRR^+$	30		dB	Fe = 160 kHz
V^- supply rejection ratio	$PSRR^-$	42		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	86		μ V rms	BW = 1 kHz
Signal to noise ratio	SNR	87		dB	Fe = 80 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation : As>50 dB for F>3.6 Fc
(with Ipwf = 250 μ A)
- passband gain : $G_o = -0.5$ dB

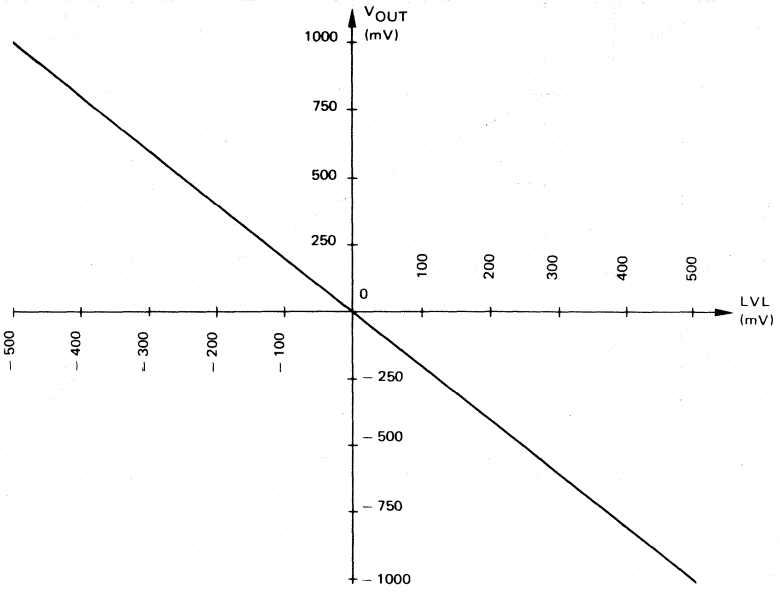
PHASE RESPONSE CURVE (IN PASSBAND)



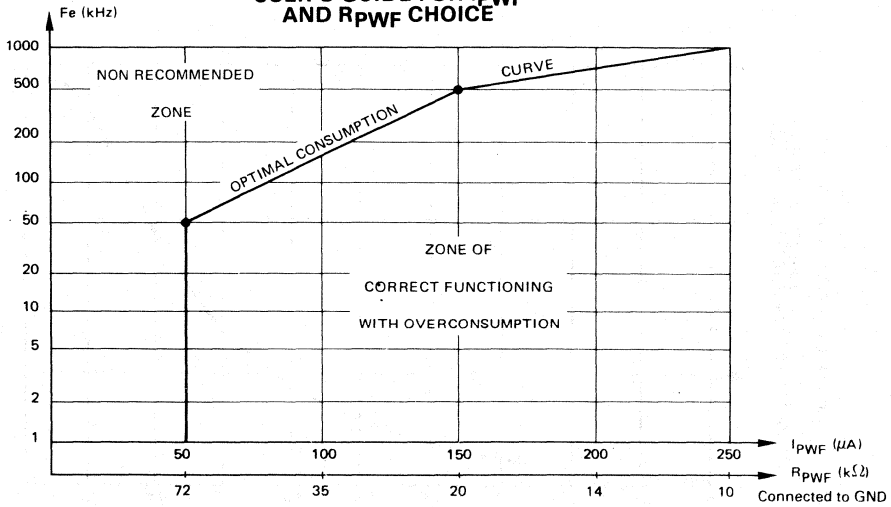
GROUP DELAY CURVE (IN PASSBAND)



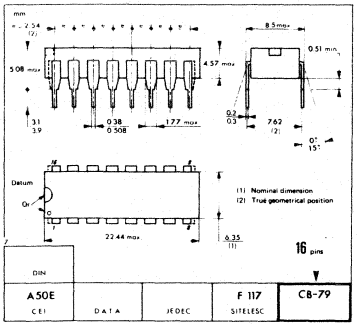
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



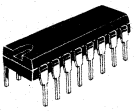
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



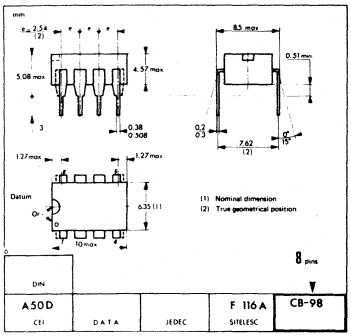
PHYSICAL DIMENSIONS



CASE CB-79



P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

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NOTES

Printed in France

THOMSON COMPONENTS MICONDUCTEURS

TSG8530

MPF HIGH PASS ELLIPTIC FILTER. CAUER TYPE. 3th ORDER

The TSG8530 is a HCMOS highpass* elliptic filter.

Main features:

- CAUER type.
- 3th order.
- Stopband attenuation: 15 dB (typ).
- Passband ripple: 0.2 dB (typ).
- Clock to cut-off freq. ratio: 320.
- Clock frequency range: 4 to 2400 kHz.
- Cut-off frequency range: 12 Hz to 7.5 kHz.

* According to spectrum aliasing phenomenon, the TSG8530 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

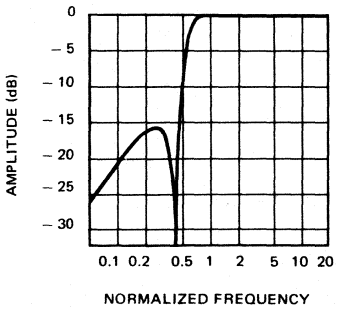
Ordering informations:

- Plastic 16 pins package: TSG8530XP.
- Ceramic 16 pins package: TSG8530XC.
- Cerdip 16 pins package: TSG8530XJ.
- Plastic 8 pins package: TSG85301XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

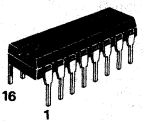
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-79

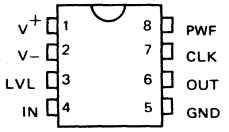


CASE CB-98

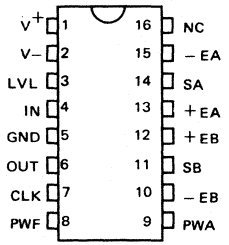
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

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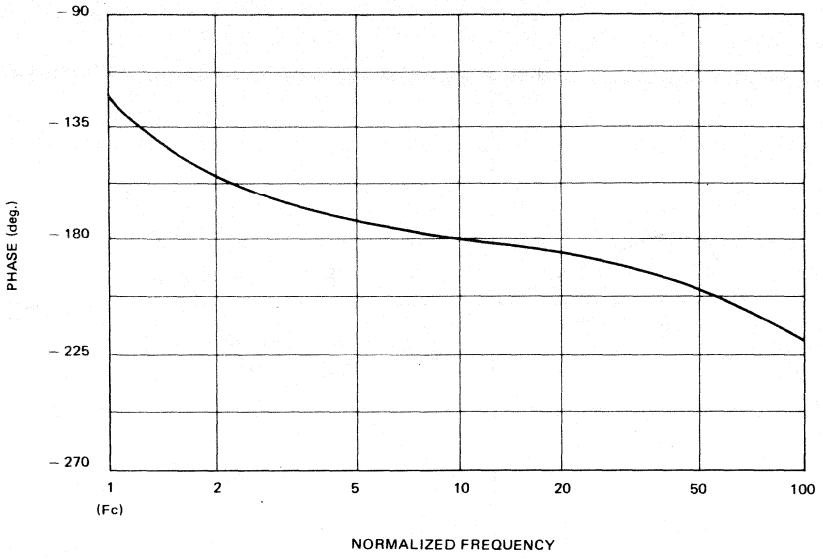
FILTER SPECIFICATIONS

Highpass filter: TSG8530; Type: Cauer; Order: 3.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, $I_{PWF} \neq 100\ \mu A$

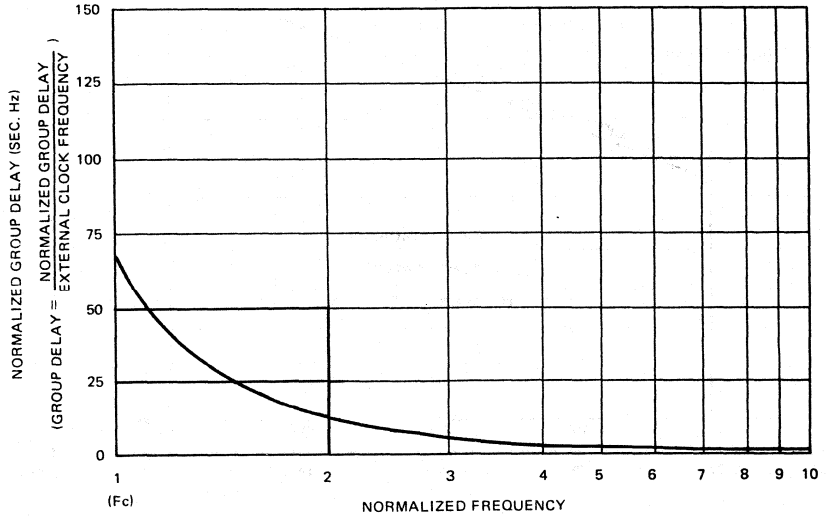
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	4 2400 (*)		kHz (min) kHz (max)	
Internal sampling freq.	Fi	2 1200 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	320 ± 1 %		—	
Cutoff frequency	Fc	0.0125 7.5 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.3 0		dB (min) dB (max)	
Passband ripple	Ap	0.2	0.5	dB (max)	[Fc, 30 Fc], Fe = 320 kHz
Stopband attenuation	As	15	14	dB (min)	F<0.49 Fc ; Fe = 320 kHz
Output DC offset voltage	Voff	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 40		mV	
Level gain	LG	- 6		—	
PWF resistance	R_{PWF}	10 72		k Ohm (min) k Ohm (max)	
Input current on PWF	I_{PWF}	50 250		μA (min) μA (max)	
V^+ supply current	I^+	2.8	5	mA (max)	Fe = 100 kHz
V^- supply current	I^-	2.8	5	mA (max)	Ipwa = 0 μA
V^+ supply rejection ratio	$PSRR^+$	33		dB	Fe = 32 kHz
V^- supply rejection ratio	$PSRR^-$	38		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp - p (max)	
Output noise	Vn	80		μV rms	BW = 2 kHz
Signal to noise ratio	SNR	85		dB	Fe = 32 kHz Vin = 2 Vrms

(*) At maximum Fe : - stopband attenuation : As>14 dB for f<0.49 Fc
(with Ipwf = 250 μA) - passband ripple : Ap = 0.2 db
- passband gain : G_o = - 0.6 dB

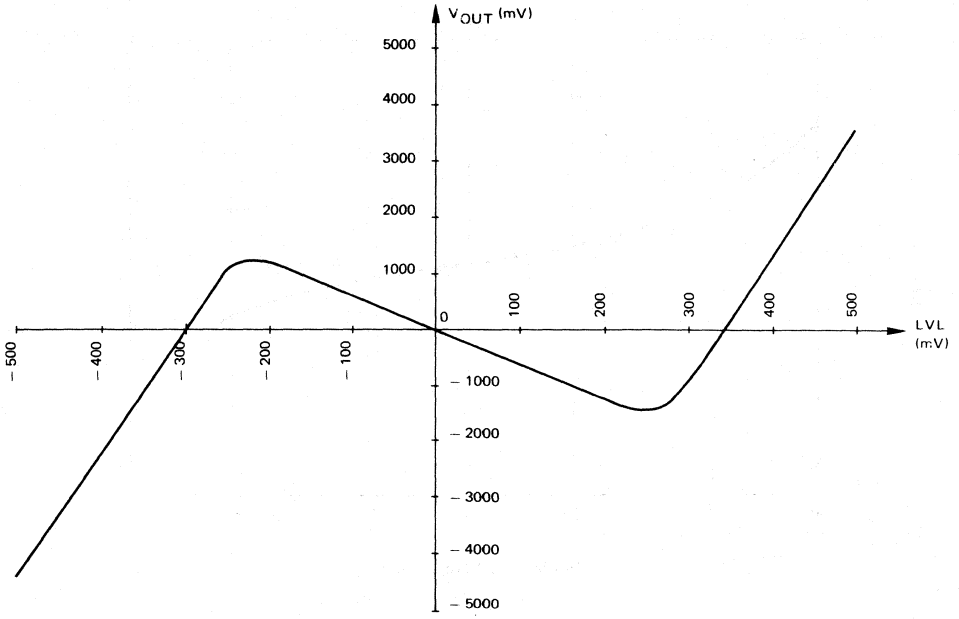
PHASE RESPONSE CURVE (IN PASSBAND)



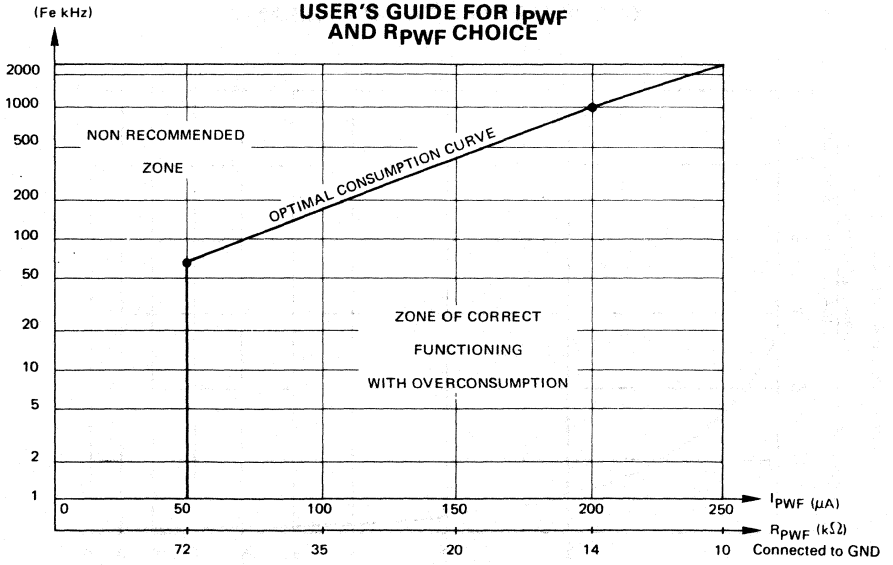
GROUP DELAY CURVE (IN PASSBAND)



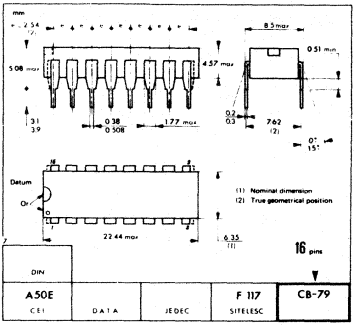
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



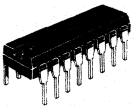
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



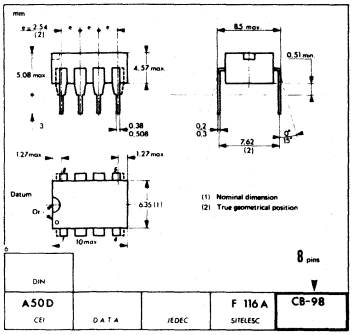
PHYSICAL DIMENSIONS



CASE CB-79



P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

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THOMSON COMPONENTS SEMICONDUCTEURS

TSG8531

MPF HIGH PASS ELLIPTIC FILTER. CAUER TYPE. 6th ORDER

The TSG8531 is a HCMOS highpass* elliptic filter.

Main features:

- CAUER type.
- 6th order.
- Stopband attenuation: 32 dB (typ).
- Passband ripple: 0.15 dB (typ).
- Clock to cut-off freq. ratio: 400.
- Clock frequency range: 4 to 1800 kHz.
- Cut-off frequency range: 10 Hz to 4.5 kHz.

* According to spectrum aliasing phenomenon, the TSG8531 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

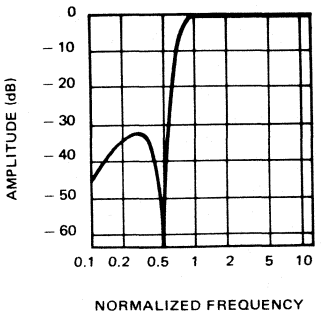
Ordering informations:

- Plastic 16 pins package: TSG8531XP.
- Ceramic 16 pins package: TSG8531XC.
- Cerdip 16 pins package: TSG8531XJ.
- Plastic 8 pins package: TSG85311XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

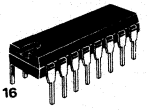
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-79

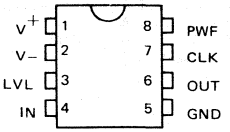


P SUFFIX
PLASTIC PACKAGE

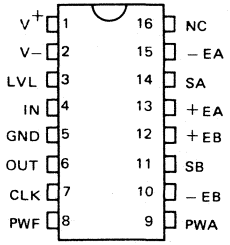
CASE CR-98

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

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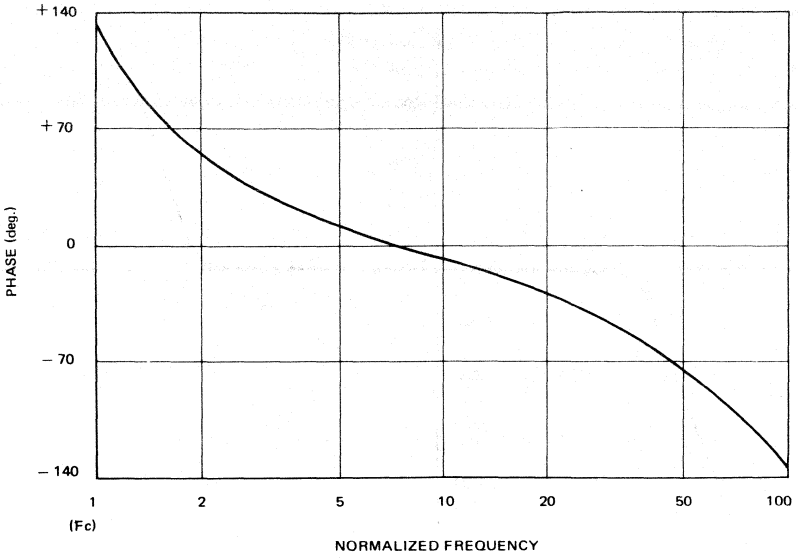
FILTER SPECIFICATIONS
Highpass filter: TSG8531; Type: Cauer; Order: 6.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, Ipwf = 100 μ A

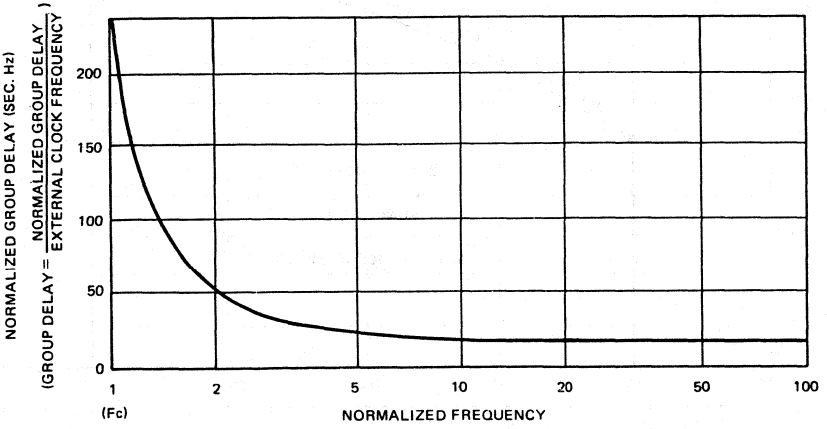
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	4 1800 (*)		kHz (min) Khz (max)	
Internal sampling freq.	Fi	2 900 (*)		kHz (min) Khz (max)	
Clock to cutoff fr. ratio	Fe /Fc	400 ± 1 %		—	
Cutoff frequency	Fc	0.01 4.5 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.1 0.1		dB (min) dB (max)	
Passband ripple	Ap	0.15	0.4	dB (max)	|Fc, 30 Fc| ; Fe = 400 kHz
Stopband attenuation	As	32	30	dB (min)	F < 0.55 Fc Fe = 400 kHz
Output Dc offset voltage	V off	± 100	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 300		mV	
Level gain	LG	0.1		—	
PWF resistance	R_{PWF}	10 72		K Ohm (min) K ohm (max)	
Input current on PWF	I_{PWF}	50 250		μA (min) μA (max)	
V+ supply current	I+	3.5	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.5	5	mA (max)	Ipwa = 0μA
V+ supply rejection ratio	PSRR +	36		dB	Fe = 40 kHz
V- supply rejection ratio	PSRR-	48		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input Capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp-p (max)	
Output noise	Vn	178		μV rms	BW = 2 kHz
Signal to noise ratio	SNR	80		dB	Fe = 40 kHz Vin = 2 Vrms

(*) At maximum Fe: stopband attenuation As > 30 dB for F < 0.55 Fc
(with Ipwf = 250μA)
passband ripple : Ap = 0.3 dB
passband gain : G_o = -1 dB

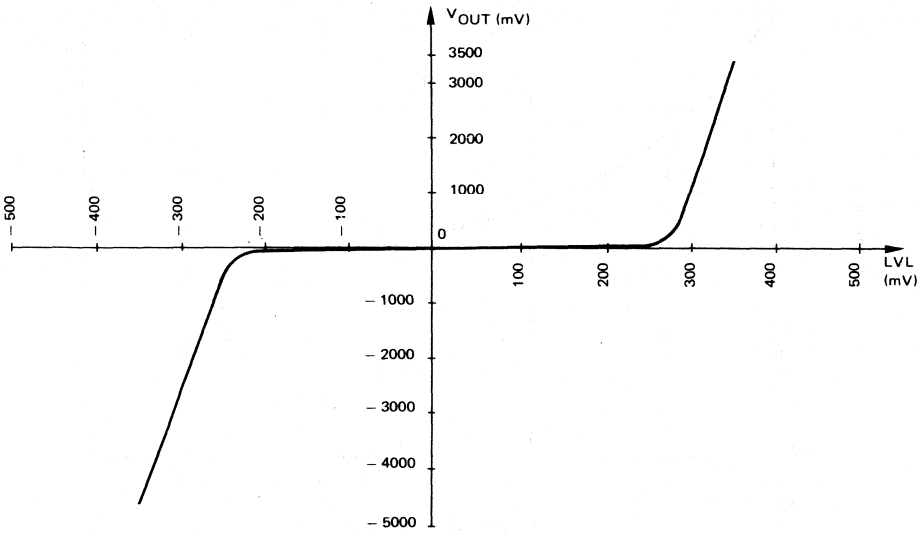
PHASE RESPONSE CURVE (IN PASSBAND)



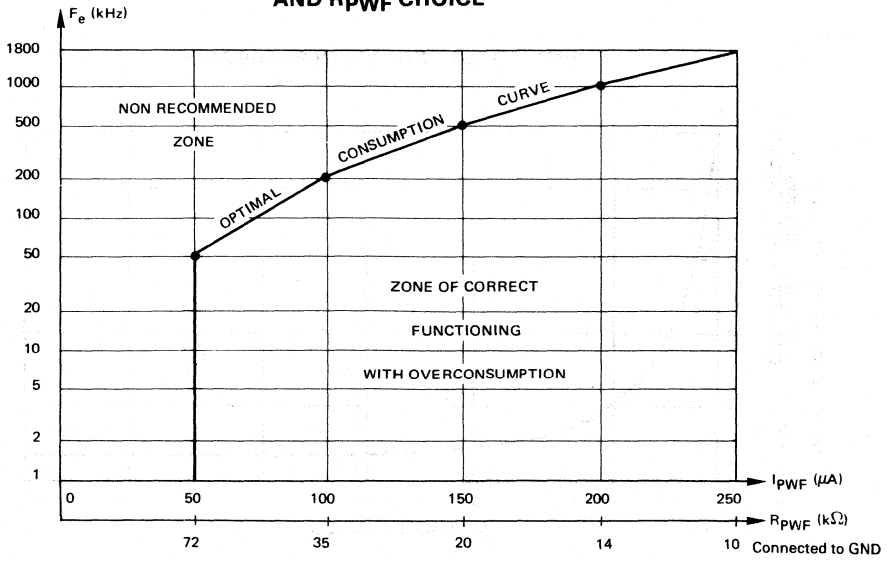
GROUP DELAY CURVE (IN PASSBAND)



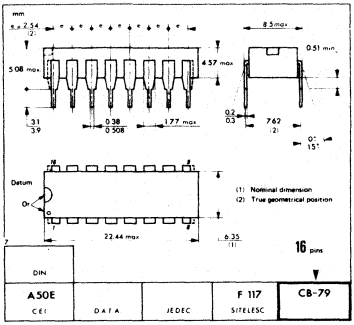
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



PHYSICAL DIMENSIONS



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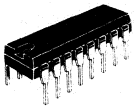
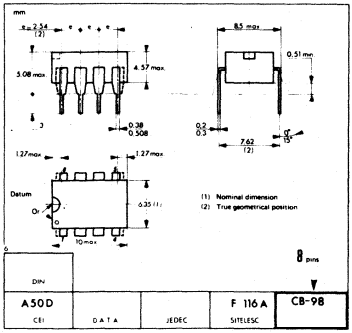


P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

THOMSON COMPONENTS SEMICONDUCTEURS

TSG8532

MPF HIGH PASS POLYNOMIAL FILTER. CHEBYCHEV TYPE. 6th ORDER

The TSG8532 is a HCMOS highpass* polynomial filter.

Main features:

- CHEBYCHEV type.
- 6th order.
- Stopband attenuation: 60 dB (typ). at 0.25 x F_C
- Passband ripple: 0.45 dB (typ).
- Clock to cut-off freq. ratio: 500.
- Clock frequency range: 5 to 1800 kHz.
- Cut-off frequency range: 10 Hz to 3.6 kHz.

* According to spectrum aliasing phenomenon, the TSG8532 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

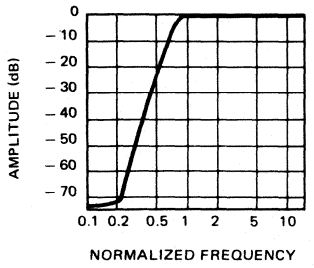
Ordering informations:

- Plastic 16 pins package: TSG8532XP.
- Ceramic 16 pins package: TSG8532XC.
- Cerdip 16 pins package: TSG8532XJ.
- Plastic 8 pins package: TSG85321XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

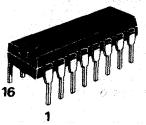
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-79



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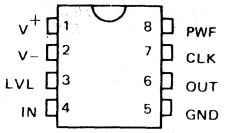
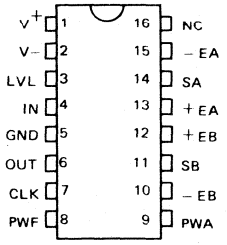
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix) and Cerdip package (J suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

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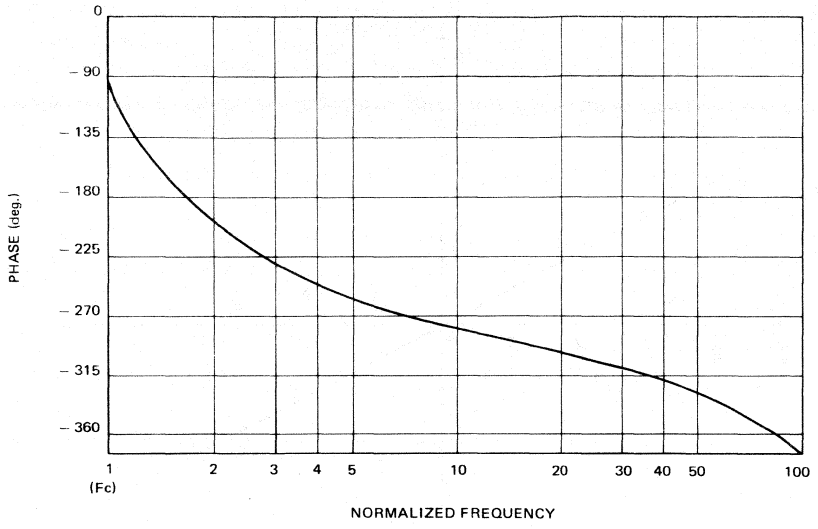
FILTER SPECIFICATIONS
Highpass filter: TSG8532; Type: Chebychev; Order: 6.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, $I_{PWF} = 100\ \mu A$

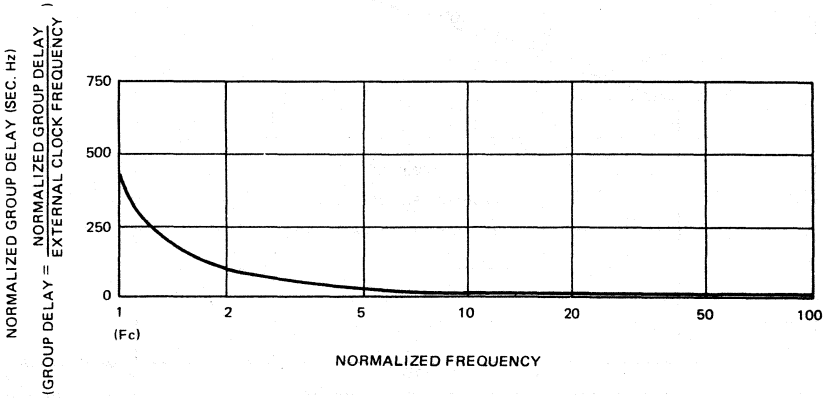
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	5 1800 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	2.5 900 (*)		kHz (min) kHz (max)	
Clock to cutoff fr. ratio	Fe/Fc	500 ± 1 %		—	
Cutoff frequency	Fc	0.01 3.6 (*)		kHz (min) kHz (max)	
Passband gain	G_o	- 0.4 0		dB (min) dB (max)	
Passband ripple	Ap	0.45	0.8	dB (max)	[1Fc,45 Fc] Fe = 500 kHz
Stopband attenuation	As	60	55	dB (min)	F < 0.25Fc; Fe = 500 kHz
Output DC offset voltage	V off	± 80	± 200	mV (max)	LVL = 0 Volt
DC level adjustment	LVL	± 75		mV (max)	
Level gain	LG	-2.7		—	
PWF resistance	R_{PWF}	10 72		K Ohm (min) K Ohm (max)	
Input current on PWF	I_{PWF}	50 250		μA (min) μA (max)	
V+ supply current	I+	3.4	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.4	5	mA (max)	Ipwa = 0μA
V+ supply rejection ratio	PSRR +	49		dB	Fe = 50 kHz
V- supply rejection ratio	PSRR-	46		dB	Fin = 1 kHz
Input resistance	R_{IN}	3		M Ohm	
Input Capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+ 3.5 - 4.5		Vp-p (max)	
Output noise	Vn	88		μV rms	BW = 2 kHz
Signal to noise ratio	SNR	85		dB	Fe = 50 kHz Vin = 2 Vrms

(*) At maximum Fe :
(with Ipwf = 250μA)
passband ripple : Ap = 0.8 dB
passband gain : $G_o = -0.8$ dB

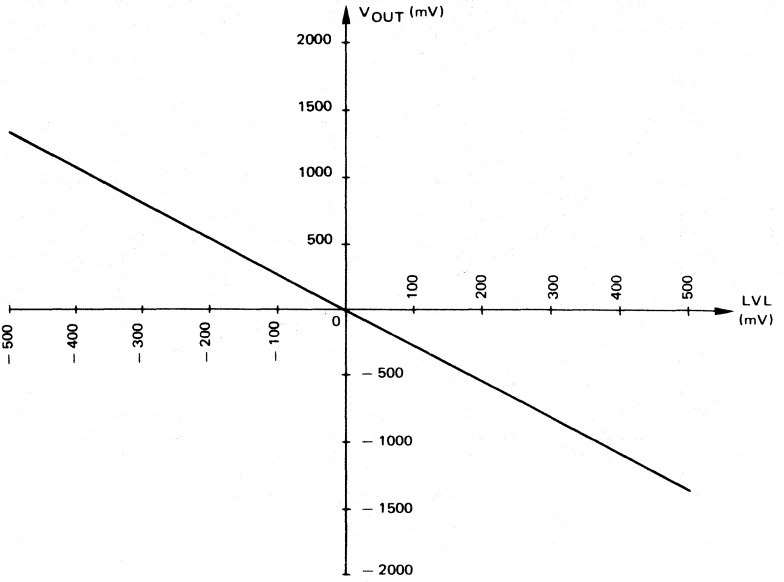
PHASE RESPONSE CURVE (IN PASSBAND)



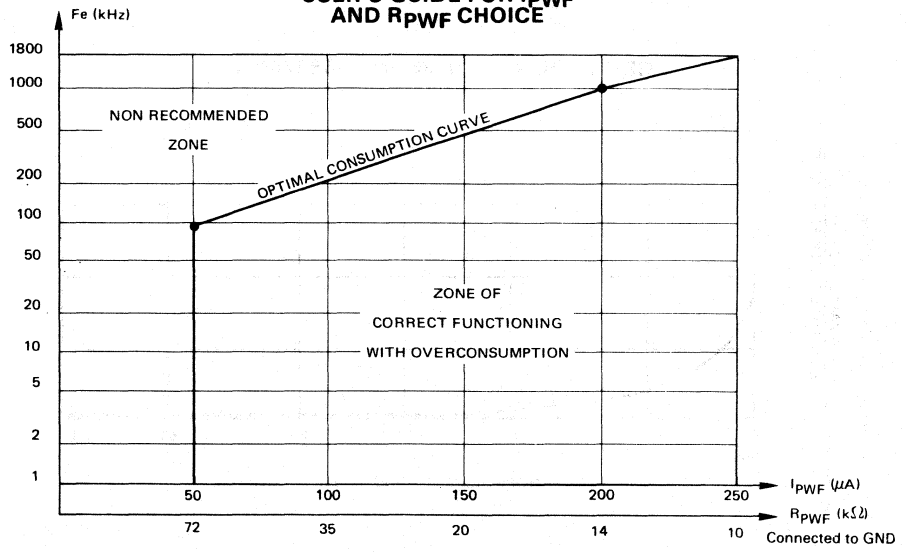
GROUP DELAY CURVE (IN PASSBAND)



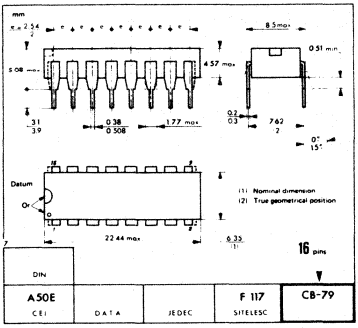
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



PHYSICAL DIMENSIONS



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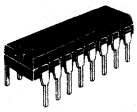
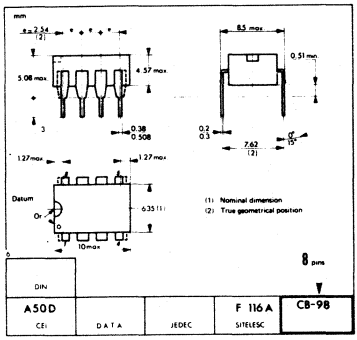


P SUFFIX
PLASTIC PACKAGE



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P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

Printed in France

THOMSON COMPONENTS SEMICONDUCTEURS

TSG8550

MPF BAND PASS FILTER. CAUER TYPE. 6th ORDER

The TSG8550 is a HCMOS Cauer band-pass filter.

Main features:

- 6th order.
- Selectivity factor: Q = 7.
- Gain at center frequency: 0 dB (typ).
- Low stopband attenuation: 40 dB (typ).
- High stopband attenuation: 40 dB (typ).
- Clock to center freq. ratio: 48.
- Clock frequency range: 1 to 1200 kHz.
- Center frequency range: 20.8 Hz to 25 kHz.

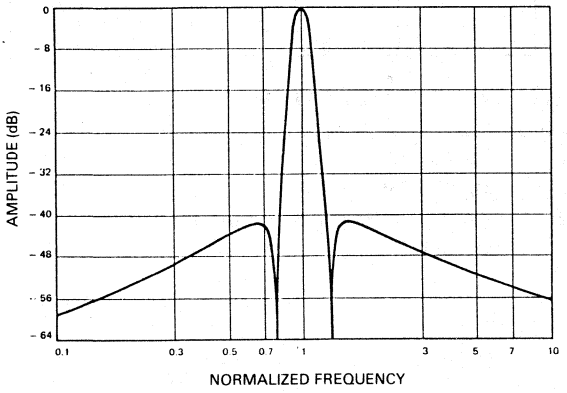
Ordering informations:

- Plastic 16 pins package: TSG8550XP.
- Ceramic 16 pins package: TSG8550XC.
- Cerdip 16 pins package: TSG8550XJ.
- Plastic 8 pins package: TSG85501XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

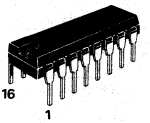
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-79

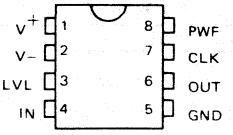


CASE CB-98

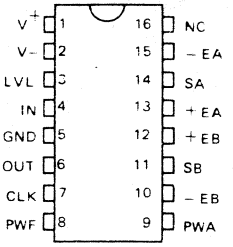
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C Suffix) and Cerdip package (J Suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

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FILTER SPECIFICATIONS

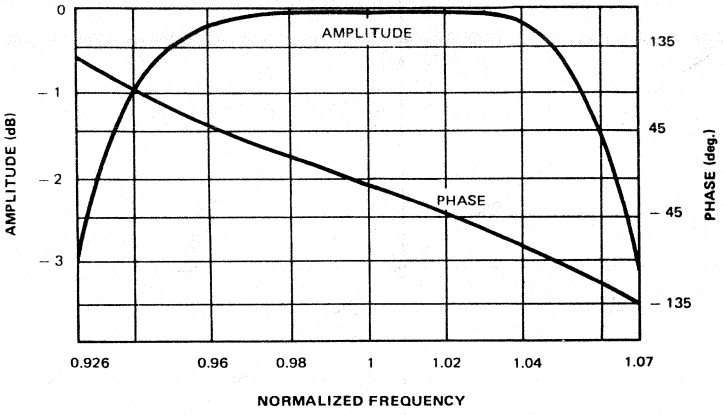
Band-pass filter: TSG8550; Type: CAUER; Order: 6
$V^+ = 5$ V, $V^- = -5$ V, T = 25°C, RL = 5 kohm, CL = 100 pF, $I_{PWF} = 50\ \mu A$

Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	1 1200 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	0.5 600 (*)		kHz (min) kHz (max)	
Clock to center frequency ratio	Fe/Fo	48 ± 1%		—	
Center frequency	Fo	0.0208 25 (*)		kHz (min) kHz (max)	
Gain at center frequency	G_o	0	0 -2	dB (max) dB (min)	Typ. G_o = -0.2 dB for Fe = 48 kHz
Low cutoff frequency	Flc	0.0204 24.5 (*)		kHz (min) kHz (max)	Flc = 0.971 Fo
High cutoff frequency	Fhc	0.0216 25.9 (*)		kHz (min) kHz (max)	Fhc = 1.035 Fo
-3 dB bandwidth	BW	0.003 3.15 (*)		kHz (min) kHz (max)	[0.926 Fo, 1.07 Fo]
Selectivity coefficient	Q	7		—	Q = Fo/BW
Passband ripple	Ap	0.05	0.3	dB (max)	
Low stopband attenuation	Als	40.5	40	dB (min)	F < 0.8 Fo
High stopband attenuation	Ahs	40.5	40	dB (min)	F > 1.24 Fo
Output DC offset voltage	V off	± 100	± 200	mV (max)	LVL = 0 volt
DC level adjustment	LVL	± 118		mV (max)	
Level gain	LG	-1,7		—	
PWF resistance	R_{PWF}	10 72		kohm (min) kohm (max)	
Input current on PWF	I_{PWF}	50 250		μA (min) μA (max)	
V^+ supply current	I^+	1.7	5	mA (max)	Fe = 48 kHz
V^- supply current	I^-	1.7	5	mA (max)	Ipwa = 0 μA
V^+ supply rejection ratio	$PSRR^+$	9		dB	Fe = 48 kHz
V^- supply rejection ratio	$PSRR^-$	20		dB	Fin = 1 kHz
Input resistance	Rin	3		Mohm	
Input capacitance	Cin	20		pF	
Output voltage swing	Vo	+ 3.5 -4.5		Vp-p (max)	
Output noise	Vn	272		μV rms	BW = 144 Hz C_{PWF} = 33 pF Fe = 48 kHz Vin = 2 Vrms
Signal to noise ratio	SNR	78		dB	

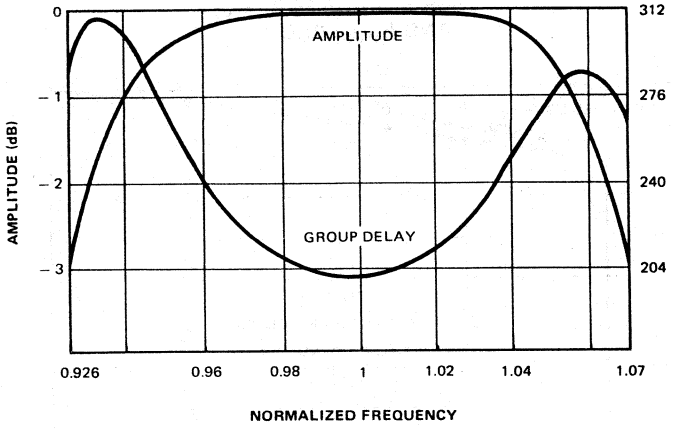
(*) At maximum Fe :
(with $I_{PWF} = 250\ \mu A$)

Stopband attenuation	Als > 39 dB for f < 0.8 Fo
Stopband attenuation	Ahs > 42 dB for f > 1.24 Fo
Passband ripple	Ap = 0.3 dB
Gain at center freq.	G_o = - 1.5 dB
-3 dB bandwidth	BW = 3.15 kHz [0.926 Fo, 1.052 Fo]
Selectivity	Q = 7.9

PHASE RESPONSE CURVE (IN PASSBAND)

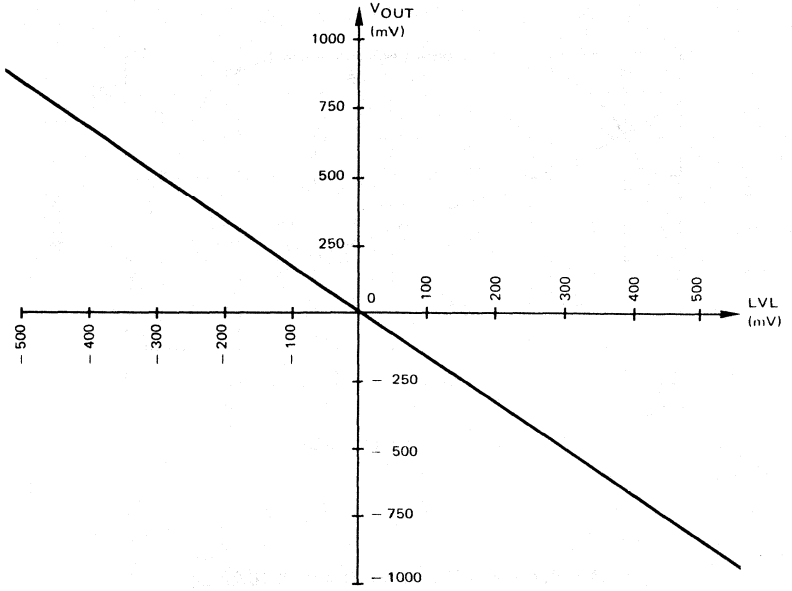


GROUP DELAY CURVE (IN PASSBAND)

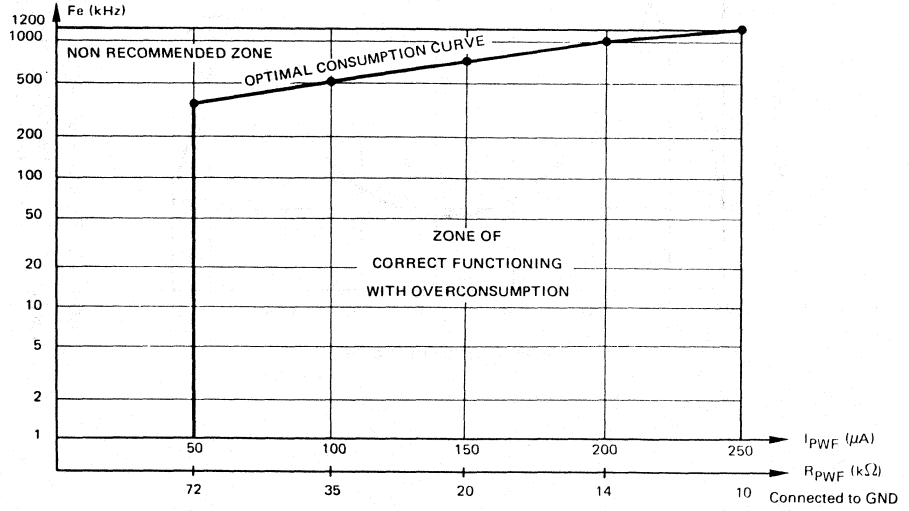


NORMALIZED GROUP DELAY (SEC. Hz) = $\frac{\text{NORMALIZED GROUP DELAY}}{\text{EXTERNAL CLOCK FREQUENCY}}$

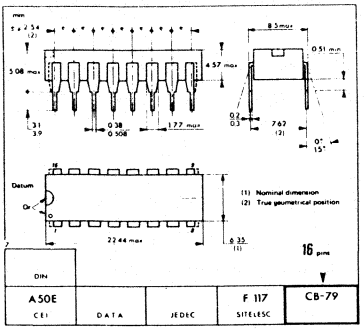
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



PHYSICAL DIMENSIONS



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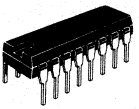
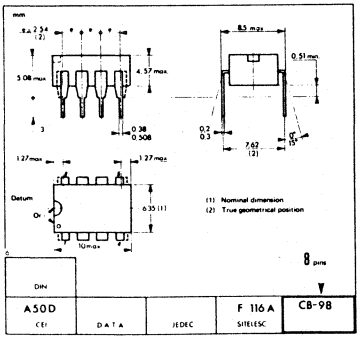


P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

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THOMSON COMPONENTS SEMICONDUCTEURS

TSG8551

MPF BAND PASS FILTER. CHEBYCHEV TYPE. 8th ORDER

The TSG8551 is a HCMOS high selectivity bandpass filter.

Main features:

- 8th order.
- Selectivity factor: Q = 35.
- Gain at center frequency: 30 dB (typ).
- Low stopband attenuation: 70 dB (typ).
- High stopband attenuation: 70 dB (typ).
- Clock to center freq. ratio: 187.2.
- Clock frequency range: 4 to 3800 kHz.
- Center frequency range: 22 Hz to 20.3 kHz.

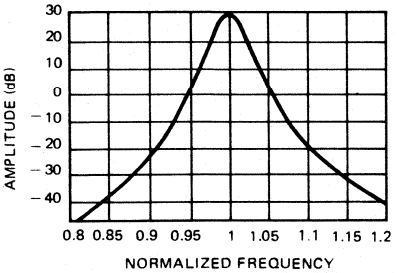
Ordering informations:

- Plastic 16 pins package: TSG8551XP.
- Ceramic 16 pins package: TSG8551XC.
- Cerdip 16 pins package: TSG8551XJ.
- Plastic 8 pins package: TSG85511XP.

X: Temperature range = C : 0°C, + 70°C
I : -25°C, + 85°C
V : -40°C, + 85°C
M : -55°C, + 125°C

Note: For general characteristics, see TSG85XX specifications. For non standard quality level, consult THOMSON SEMICONDUCTEURS general ordering information.

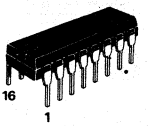
AMPLITUDE RESPONSE CURVE



LINEAR HCMOS1 M.P.F

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

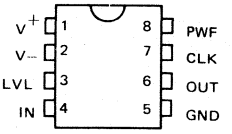
CASE CB-79



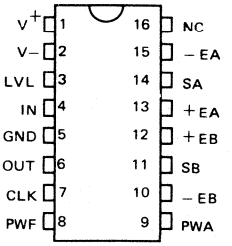
CASE CB-98 **P SUFFIX** PLASTIC PACKAGE

Ceramic package (C Suffix) and Cerdip package (J Suffix) are also available

PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

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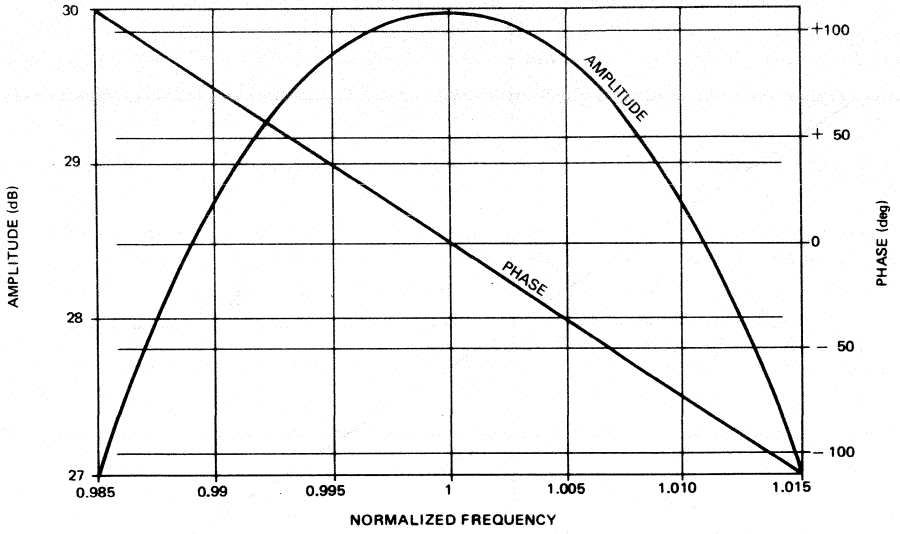
FILTER SPECIFICATIONS

Bandpass filter: TSG8551; Type: High Q; Order: 8.
$V^+ = 5$ V, $V^- = -5$ V, T = 25 °C, RL = 5 k Ohm, CL = 100 pF, $I_{PWF} = 100\ \mu A$

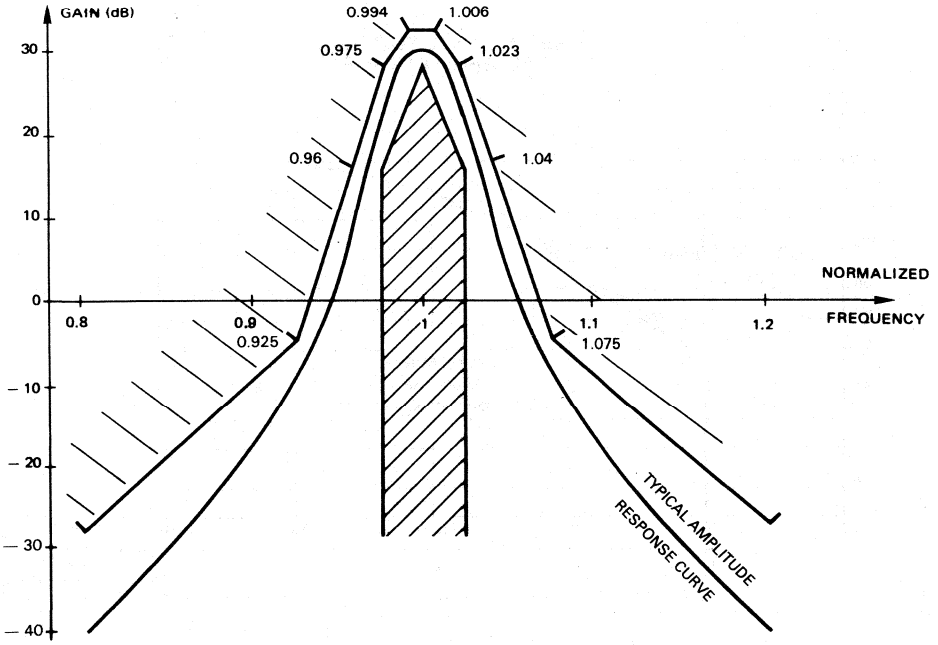
Characteristic	Symbol	Typ.	Tested limits	Unit	Conditions
External clock frequency	Fe	4 3800 (*)		kHz (min) kHz (max)	
Internal sampling frequency	Fi	0.5 475 (*)		kHz (min) kHz (max)	
Clock to center frequency ratio	Fe/Fo	187.2 ± 1 %		—	
Center frequency	Fo	0.022 20.3(*)		kHz (min) kHz (max)	
Gain at center frequency	G_o	30	32 28	dB (max) dB (min)	Fe = 400 kHz
Selectivity coefficient	Q	35		—	
Passband ripple	Ap	—		dB (max)	
Low stopband attenuation	Als	70	55	dB (min)	F < 0.8 Fo
High stopband attenuation	Ahs	70	55	dB (min)	F > 1.2 Fo
Output DC offset voltage	V off	± 100	± 200	mV (max)	LVL : 0 volt
DC level adjustment	LVL	± 70		mV (max)	
Level gain	LG	- 3.3		—	
PWF resistance *	R_{PWF}	10 72		K Ohm (min) K Ohm (max)	
Input current on PWF	I_{PWF}	50 250		µA (min) µA (max)	
V+ supply current	I+	3.8	5	mA (max)	Fe = 100 kHz
V- supply current	I-	3.8	5	mA (max)	Ipwa = 0 µA
V+ supply rejection ratio	PSRR+	10**		dB	Fe = 187.2 kHz
V- supply rejection ratio	PSRR-	19**		dB	Fin = 1 Khz
Input resistance	R_{IN}	3		M Ohm	
Input capacitance	C_{IN}	20		pF	
Output voltage swing	Vo	+3.5 -4.5		Vp-p (max)	
Output noise	Vn	56**		µV rms	BW = 3 Hz
Signal to noise ratio	SNR	90**		dB	Fe = 187.2 kHz Vin = 2 Vrms

* $I_{PWF} \doteq 200\ \mu A$
** Value divided by the gain

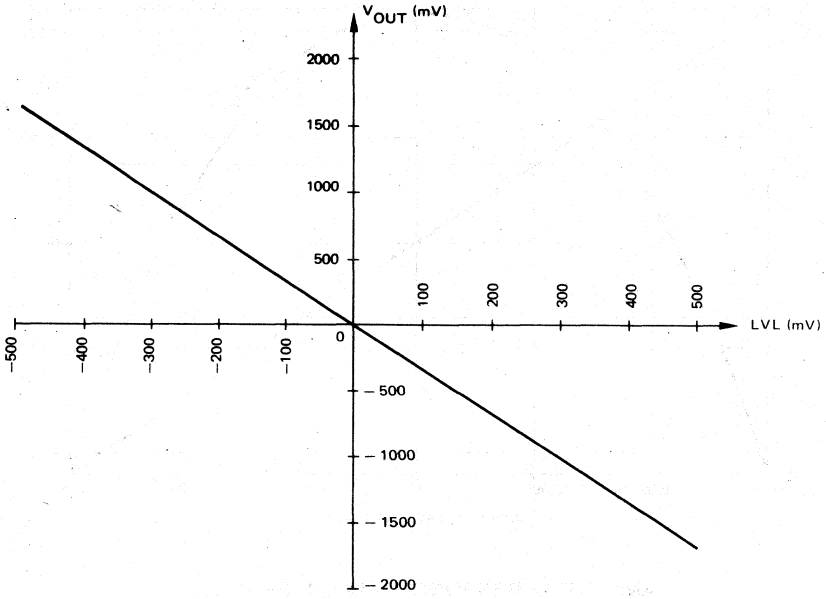
PHASE RESPONSE CURVE (IN PASSBAND)



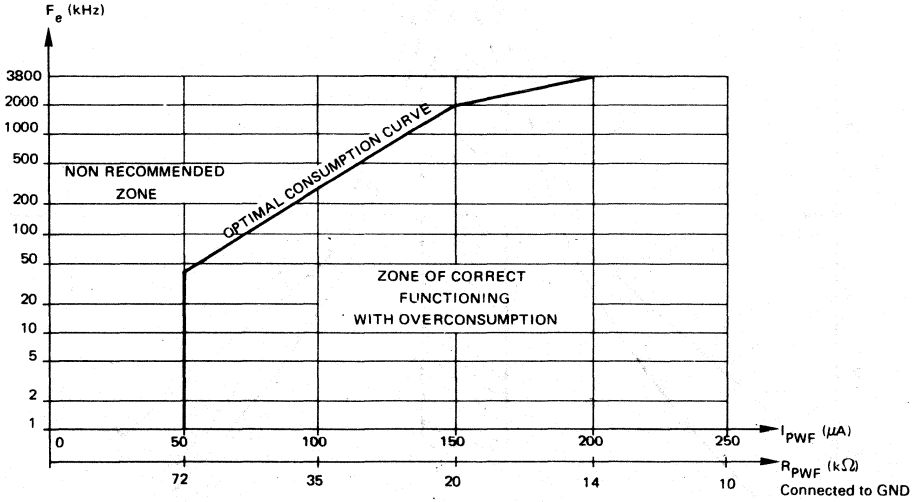
AMPLITUDE RESPONSE TEMPLATE (TESTED)



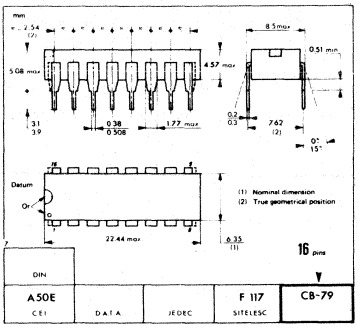
OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



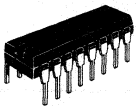
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



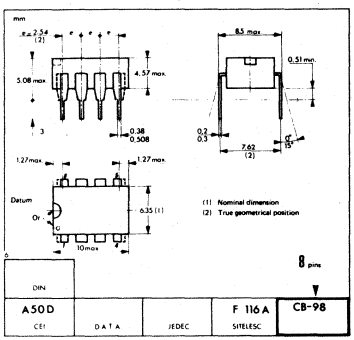
PHYSICAL DIMENSIONS



CASE CB-79



P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

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Please inquire with our sales offices about the availability of the different packages

NOTES

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THOMSON COMPONENTS SEMICONDUCTEURS

TSG8670

MPF VOICE-GRADE DUAL FILTER FOR TELEPHONE LINE INTERFACE

The TSG8670 is a HCMOS voice-grade dual filter for telephone line interface.

OUT1: RECEIVE LOW-PASS FILTER.
- CAUER type.
- 4th order.
- Stopband attenuation: 34 dB.
- Passband ripple: 0.3 dB.
- Clock to cutoff frequency ratio: 85.33.
- Clock frequency range: 1 to 1500 kHz.
- Cutoff frequency range: 12 Hz to 17 kHz.

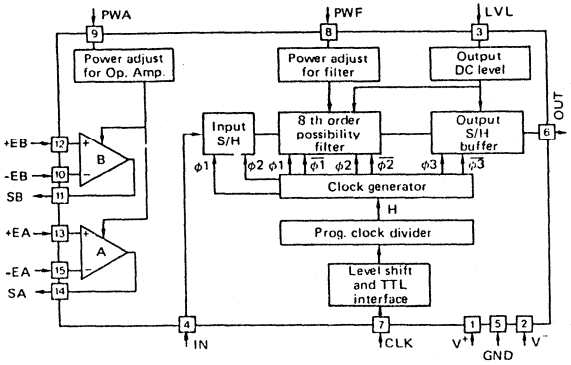
OUT2: TRANSMIT BAND-PASS FILTER.
- 8th order (5th order CAUER low-pass + 3rd order CHEBYCHEV high-pass).
- Selectivity factor: Q = 0.22.
- Upper stopband attenuation: 42 dB.
- Passband ripple: 0.2 dB.
- Clock to center frequency ratio: 342.
- Clock frequency range: 10 to 1000 kHz.
- Center frequency range: 29 Hz to 2.9 kHz.

Ordering informations:

- Plastic 18 pins package: TSG8670XP.
- Ceramic 18 pins package: TSG8670XC.
- Cerdip 18 pins package: TSG8670XJ.

X: Temperature range = C: 0°C, + 70°C, I: -25°C, + 85°C
V: -40°C, + 85°C, M: -55°C, + 125°C

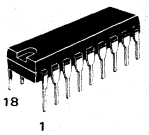
BLOCK DIAGRAM



LINEAR HCMOS1 M.P.F

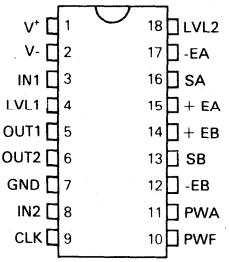
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

CASE CB-181



P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT



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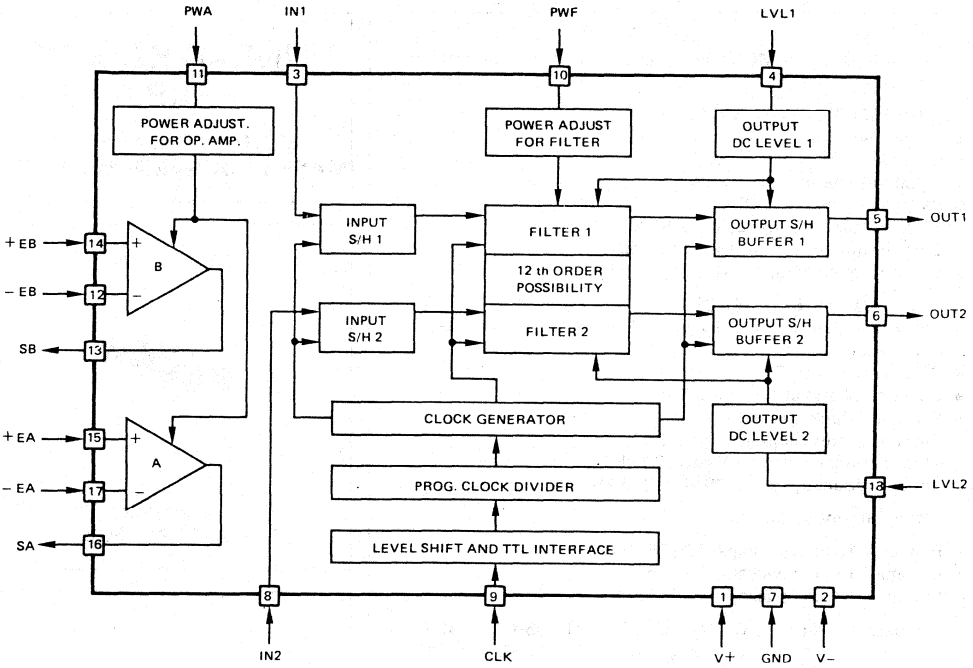
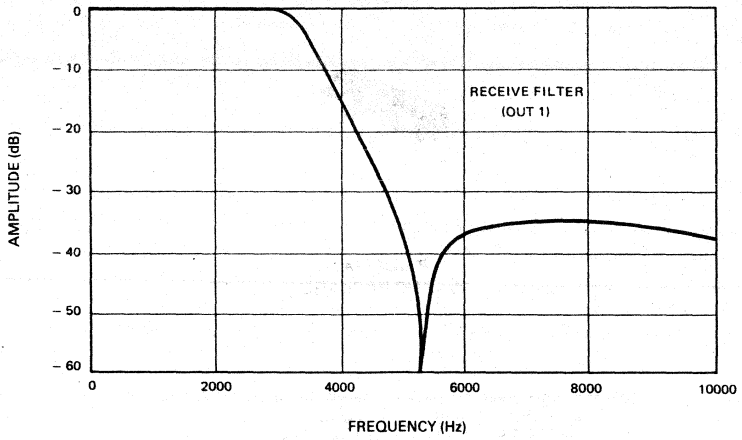
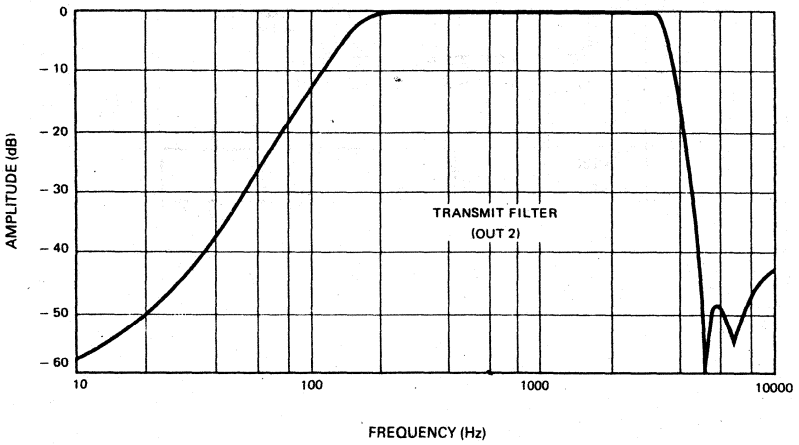
BLOCK DIAGRAM



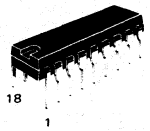
AMPLITUDE RESPONSE CURVE FOR TELEPHONE APPLICATION (CLK = 256 kHz)



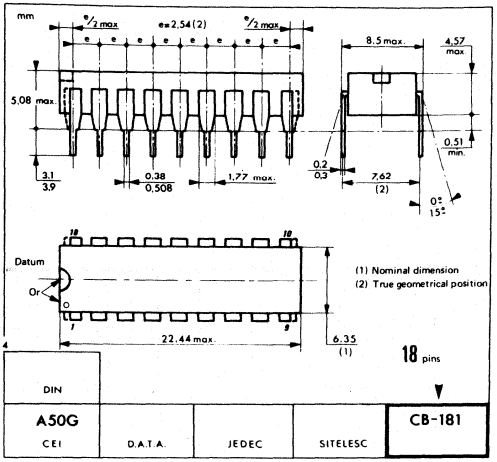


PHYSICAL DIMENSIONS

CB-181



P SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice
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LINEAR HCMOS1 M.P.F

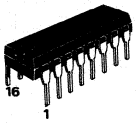
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER (SEMI CUSTOM FILTER)

THOMSON SEMICONDUCTEURS supplies the first samples 4 to 8 weeks after the customer's definition of the M.P.F specifications. All types of filters may be provided (BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL, CAUER) for conventional applications (low-pass, high-pass, bandpass, notch, group delay equalizers) or for simultaneous optimization of the amplitude and phase templates.

Main features:

- Technology: HCMOS1.
- Available orders: 4 to 8 (whatever the type of M.P.F).
- Input signal frequency range: 0 to 30 kHz
- Clock frequency range: 1 to 2000 kHz
- Clock to cut-off frequency ratio: 20 to 400 (depending on the M.P.F considered).
- Signal to noise ratio: 60 to 85 dB (depending on the internal structure of the M.P.F considered).
- Power supply: ±5 V or 0-10 V.
- Consumption adjustable between 0.5 to 20 mW per order.
- Accuracy of the cut-off frequencies: 0.5%.
- Response curves (amplitude and phase) translatable by changing the clock frequency.

CASE CB-79

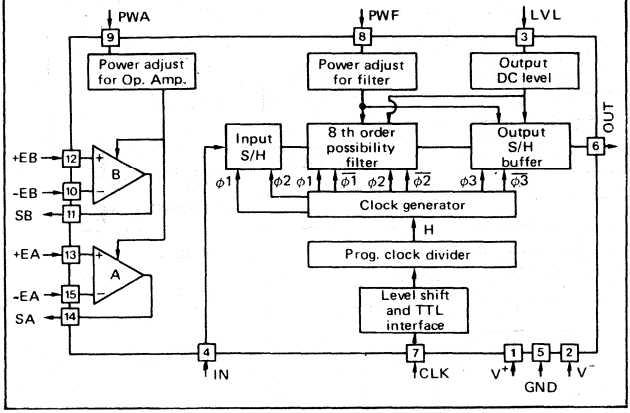


CASE CB-98

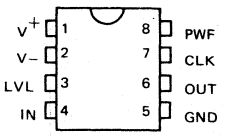
P SUFFIX
PLASTIC PACKAGE

Ceramic package (C suffix)
and Cerdip package (J suffix)
are also available

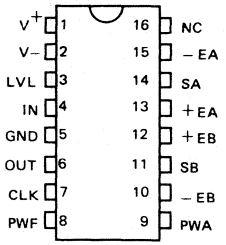
BLOCK DIAGRAM



PIN ASSIGNMENT



8 pins: FILTER ONLY



16 pins: FILTER + 2 OP-AMPs

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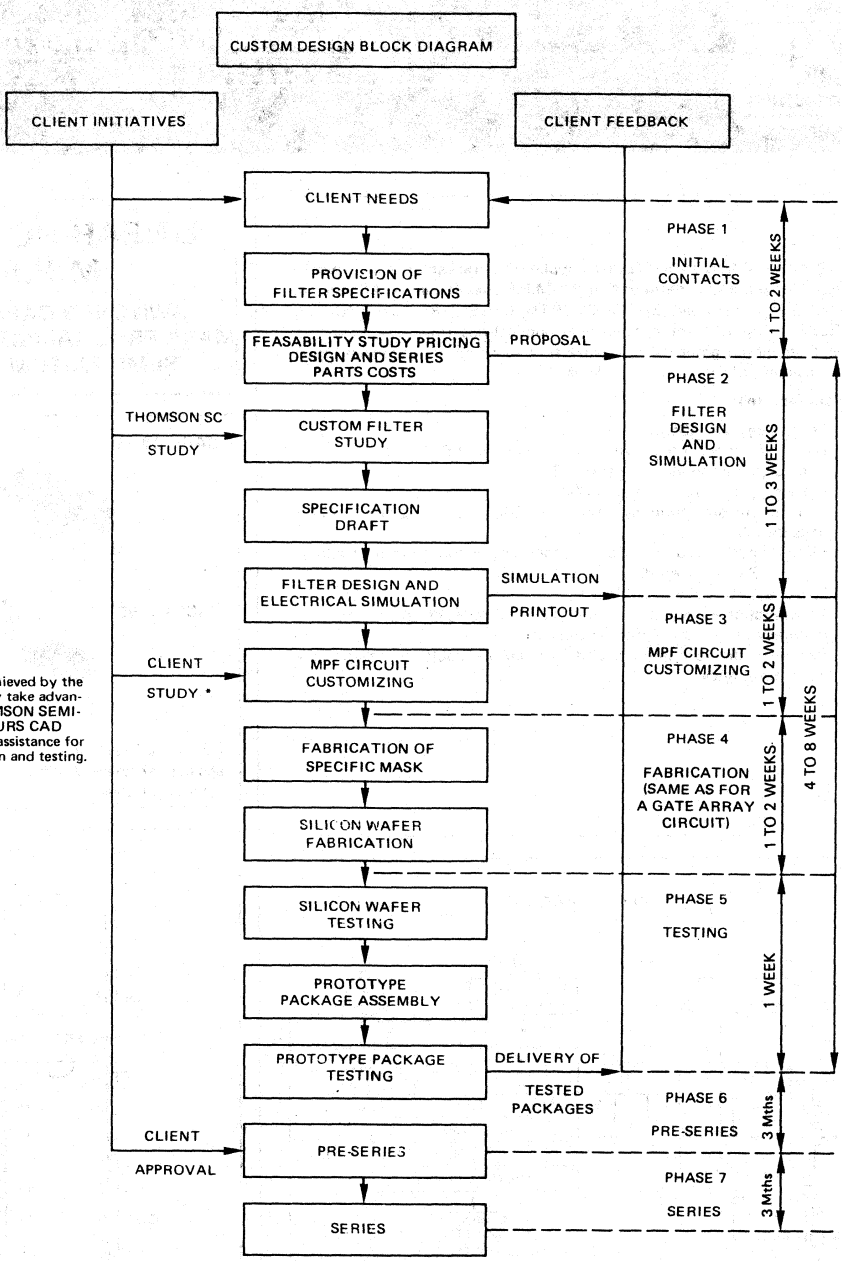
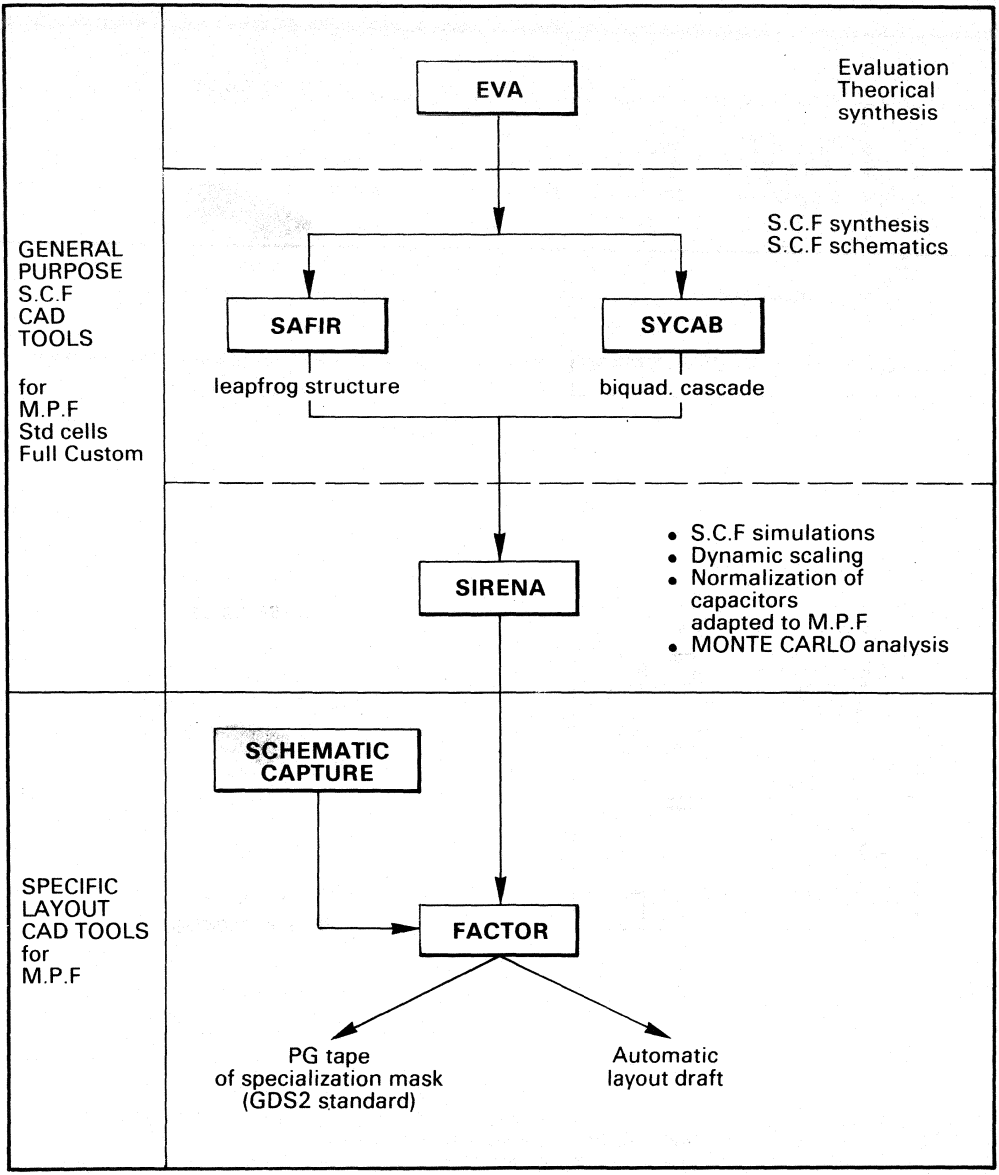
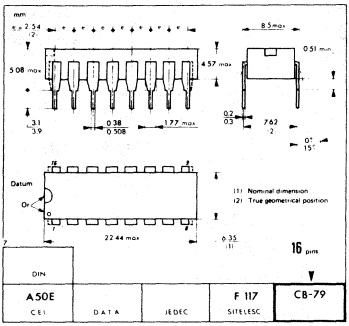


* If study is achieved by the client, he may take advantage of THOMSON SEMICONDUCTEURS CAD facilities and assistance for protype design and testing.

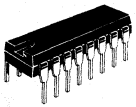
FILCAD is a software package developed by THOMSON SEMICONDUCTEURS available for its Switched Capacitor designs: M.P.F, but also Full Custom or Semi Custom Circuits containing such Filter cells.



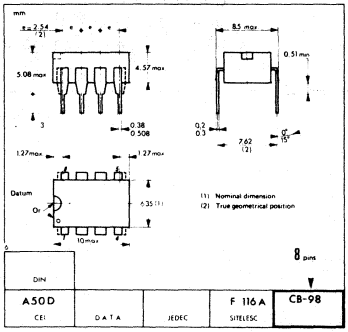
PHYSICAL DIMENSIONS



CASE CB-79



P SUFFIX
PLASTIC PACKAGE



CASE CB-98

P SUFFIX
PLASTIC PACKAGE

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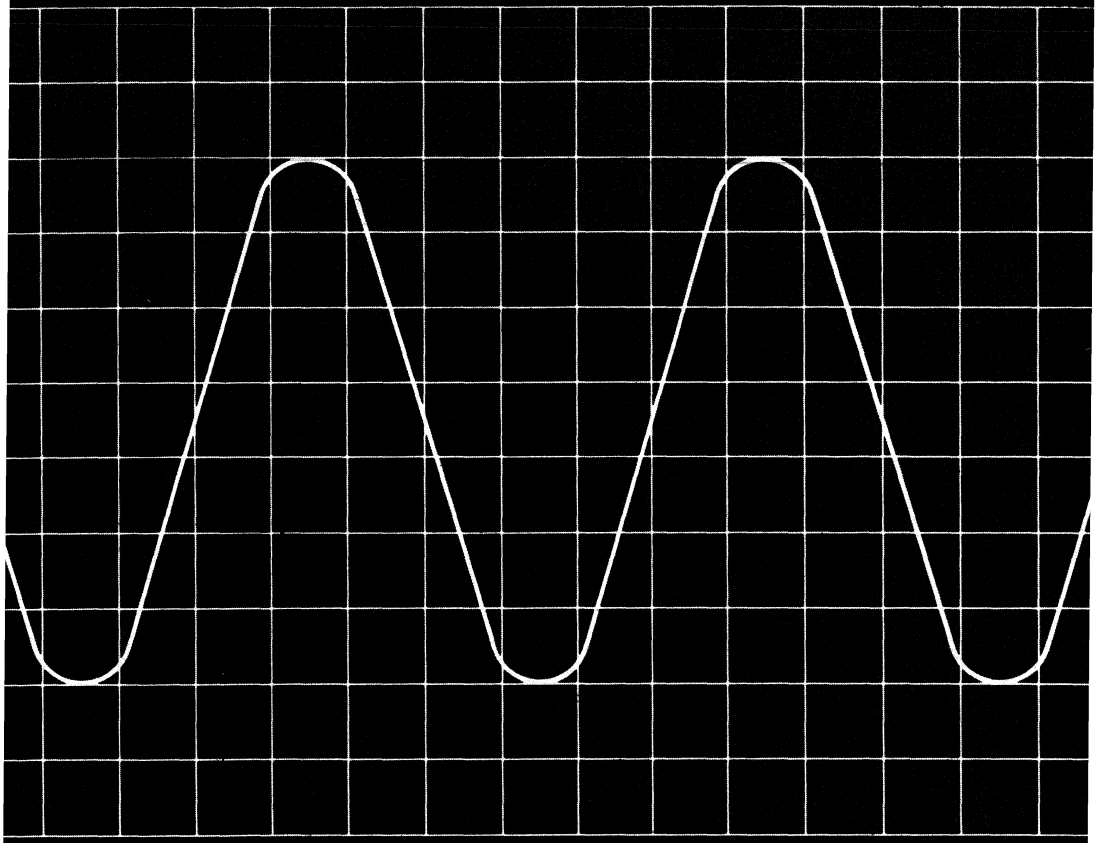
HOW TO CHOOSE A FILTER IN A SPECIFIC APPLICATION

APPLICATION NOTES AN-052



THOMSON
COMPONENTS
SEMICONDUCTEURS

O. LEENHARDT - Applications laboratory

Object of this application note:

The approach of THOMSON SEMICONDUCTEURS regarding filtering is aimed at providing all the information required for designing the filter best tailored for a given application. The first step in this approach, and undoubtedly the most important since it is essential for all the others, therefore consists in indicating how, starting from this application, the complete system specifications of a filter must be written. This is the purpose of this application note.

Reminders about the present status of the THOMSON SEMICONDUCTEURS filters

The THOMSON SEMICONDUCTEURS approach consists in manufacturing Mask Programmable Filters (M.P.F.). These filters are of the switched capacitor type. They all have the same structure, up to the last mask level (interconnection level). This level is therefore the only one differenciating these filters from one another. We will not describe in full detail the structure of these filters, but simply remind their main features, and then briefly describe the presently available M.P.F.'s.

MAIN FEATURES:

The main features of these M.P.F.'s are as follows:

- Technology: HCMOS1 (high-density linear CMOS)
- Available orders: 2 to 8 (whatever the type of M.P.F.)
- Input signal frequency: 0 to 30 KHz
- Internal sampling frequency: 500 Hz to 1 MHz (depending on the M.P.F. considered)
- Internal sampling frequency/cut-off frequency ratio: 10 to 200 (depending on the M.P.F. considered)
- The response curves (amplitude and phase) may be translated by changing the sampling frequency
- Signal/noise ratio: 70 to 85 dB (depending on the internal structure of the M.P.F. considered)
- Power supplies: ± 5 V or 0 - 10 V
- Consumption may be adjusted between 0.5 to 20 mW per order
- Accuracy of the capacitor ratios: 0.1 %
- Accuracy of the cut-off frequencies: 0.5 % (max.).

STANDARD M.P.F.'S AND CUSTOM M.P.F.'S:

THOMSON SEMICONDUCTEURS manufactures two types of M.P.F.'s:

- **Standard M.P.F.'s:**

They make up a family presently consisting of 10 models, but this family will expand in the future, according to the evolution of requirements. These M.P.F.'s are the following:

— 5 Low-pass M.P.F.'s:

TS 8510 (CAUER, 5th order: 32 dB attenuation)
TS 9511 (CAUER, 7th order: 50 dB attenuation)
TS 8512 (CAUER, 7th order: 75 dB attenuation)
TS 8513 (CHEBYCHEV, 8th order)
TS 8514 (BUTTERWORTH, 8th order)

— 3 High-pass M.P.F.'s:

TS 8530 (CAUER, 3rd order: 15 dB attenuation)
TS 8531 (CAUER, 6th order: 15 dB attenuation)
TS 8532 (CHEBYCHEV, 6th order)

— 1 Notch M.P.F.'s:

TS 8540 (8th order: Q=7)

— 2 Band-pass M.P.F.'s:

TS 8550 (CAUER, 3rd order: Q=5)
TS 8551 (high-selectivity filter: Q=35)

NOTE: The detailed description of these M.P.F.'s has been the subject of a previous application note.

● **Custom M.P.F.'s:**

THOMSON SEMICONDUCTEURS commits itself to supply the first samples 6 to 8 weeks after the customer's definition of the template. All types of filters may be provided (BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL, CAUER), for conventional applications (low-pass, high-pass, bandpass, notch filters, group delay equalizers) or for simultaneous optimization of the amplitude and the phase templates.

How to define the complete system specifications of a filter

● **FILTER SYSTEM SPECIFICATIONS:**

The system specifications of a filter are complete when they indicate:

— the amplitude template (amplitude response curve)
— the phase template (phase response curve)
— the group delay curve
— the pulse and step responses
— the dynamics
— the noise factor
— the input and output impedances
— the load impedance (resistance and capacitance)
— the type of signals to filter (level, spectrum,...)
— the value of the power supply sources
— the operating temperature range
— the size (the dimensions)
— the price
— ...

Amongst all these parameters, the knowledge of three of them is essential from the technical point of view:

— the amplitude template
— the phase template
— the group delay curve.

As we shall see later on, the following definitions may be used, with minor modifications, for all types of filters. Our definitions are given only for low-pass filters, since we can always relate back to this type when studying any other kind of filter (see 3. B).

● **Amplitude template (figure 1):**

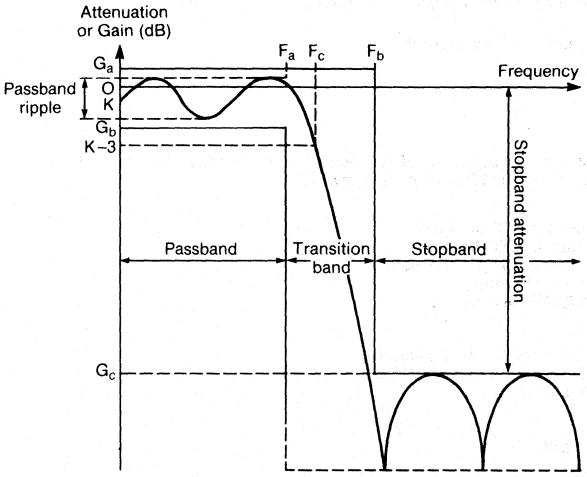


FIGURE 1: DIFFERENT PARAMETERS USED FOR DEFINING AN AMPLITUDE TEMPLATE

We cannot expect two filters, assumed to be similar, to have exactly identical response curves. This is the reason why we use the concept of template, which is a sort of envelope of the response curve limits in terms of the frequency. The amplitude template is therefore the graphical representation of the filter's "amplitude - frequency" limiting conditions. Its definition is based on the following parameters (low-pass filter):

— maximum passband attenuation (or gain) (G_a): maximum level the signal may reach within the passband (in dB)

— minimum passband attenuation (or gain) (G_b): minimum level the signal may reach within the passband (in dB)

— minimum stopband attenuation (G_c): minimum attenuation level of the signal within the stopband (in dB)

— passband: band of frequencies for which the attenuation (or the gain) must fall between G_a and G_b

— transition band: band of frequencies for which the attenuation must fall between G_b and G_c

— stopband: band of frequencies for which the attenuation must be less than G_c

— cut-off frequency (F_a): passband upper limit

— selectivity factor k: equal to the ratio F_a/F_b, it defines the width of the template transition band, and therefore of the filter selectivity. It is always less than 1.

Other parameters must be added when the response curve considered falls within this template:

— passband transfer factor (K): attenuation (or gain) factor of the response curve within the passband, relative to the 0 dB (in dB)

— passband ripple: maximum amplitude difference between two points of the response curve within the passband

— cut-off frequency (F_c): frequency corresponding to a 3 dB attenuation relative to the passband transfer factor.

Note: The template of a filter is therefore completely determined once the values of G_a, G_b, G_c, F_a and F_b are known.

- **Phase template:**

Within a real filter, all the frequencies are not transmitted at the same velocity. A non-constant phase shift results (and therefore a distortion) between the output signal and the filter input signal. The phase response curve of a filter is the phase shift curve due to this filter, in terms of the frequency. As with the amplitude response curve, it must be within a phase template, sort of graphical representation of the "phase — frequency" limiting conditions of the filter.

- **Group delay curve:**

As a consequence of what we have seen above, the group delay concept is preferred to that of propagation velocity of each of the frequencies of a spectrum. We shall thus no longer speak of the propagation velocity for a given frequency, but for a group of frequencies. This group delay is related to the phase shift by the following relationship:

$$\tau = \frac{d\Phi}{d\omega}$$

with ω = pulsation.

We may infer from this relationship that the steeper the slope of the phase response curve in terms of the frequency, and therefore the more abrupt the filter cut-off, the greater the group delay of a filter will be.

Note: On the group delay curve of the different filters shown below (see 3. D), the value to read on the y-axis corresponds to a normalized group delay ω_c . T equal to T_o, that is an actual group delay expressed in seconds equal to: $T = T_o/\omega_c$, with ω_c = cut-off pulsation of the filter.

- **Other parameters:**

— pulse and step responses:

The pulse response of a filter is its response to a DIRAC pulse. It can be shown that:

- x(t) any type of signal: $y(t) = h(t) \star x(t)$ with $\star$ = convolution product
  $\rightarrow Y(p) = H(p) \cdot X(p)$ with H(p) = transfer function
- x(t) DIRAC pulse ($\delta(t)$) : $y_\delta(t) = h(t) \star \delta(t)$
  $\rightarrow Y_\delta(p) = H(p)$

The pulse response $y_\delta(t)$ of a filter is the time representation of its transfer function H(p). It is an intrinsic feature of the filter. It contains all the information relative to the response of the filter to any type of signal.

The step response of a filter is its response to a HEAVISIDE step (unit step). On figure 2, we can see the concept of filter settling time. In effect, if a signal having a spectrum within the filter passband is applied to the filter, the settling time is equal to the time elapsed between the time the signal was applied at the filter input and the output signal obtained, to within a given percentage of the final value (1%). This settling time is closely related to the width (B) of the filter passband (1/B for a bandpass, 1/2B for a low-pass)

— dynamics:

The dynamics of a filter is the ratio between the maximum level of the output signal and its minimum level, that is, the noise level. It is expressed in dB.

— noise factor:

The noise factor is the ratio between the total filter output noise power and the output noise power due only to the noise applied at the input. It is expressed in dB. For a given structure, the filter output noise mainly depends on the amplitude template, since it is an exponential function of the overvoltage factor Q (see 3. C). In the active filters, the noise is not "white", or at least not throughout the band considered. It is therefore necessary to split this band up into several frequency areas, and to define the corresponding noise features for each of them. We may then speak of a noise power (or voltage) per Hertz (or Hertz square root), for a given frequency (nW/Hz or nV/$\sqrt{Hz}$). The noise optimization of a filter is not always easy, and this should be kept in mind at system specifications definition time, especially for filters requiring high dynamics ($>$ 60 dB).

— type of signals to be filtered:

Although this may seem obvious, it is not useless to remind the importance of knowing accurately the type of signal to filter, before defining the system specifications of the filter. The signal amplitude curve must be studied in detail (regarding the compatibility with the authorized filter input swing), as well as its frequency spectrum, in order to suppress the possible interaction of undesired frequencies (50 Hz, various harmonic components,...) during system specifications definition time.

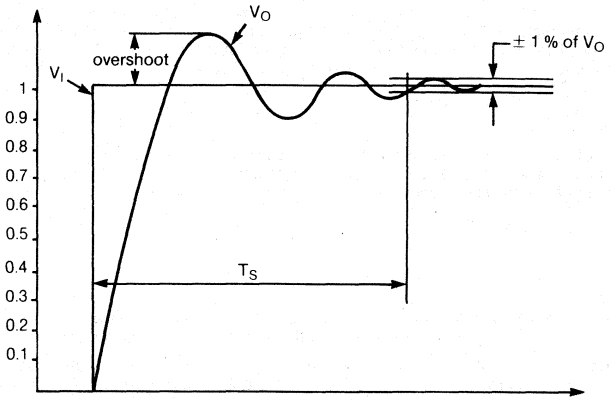


FIGURE2: SETTLING TIME (t_s) OF THE STEP RESPONSE OF A FILTER (V_O) FOR A UNIT STEP (V_I)

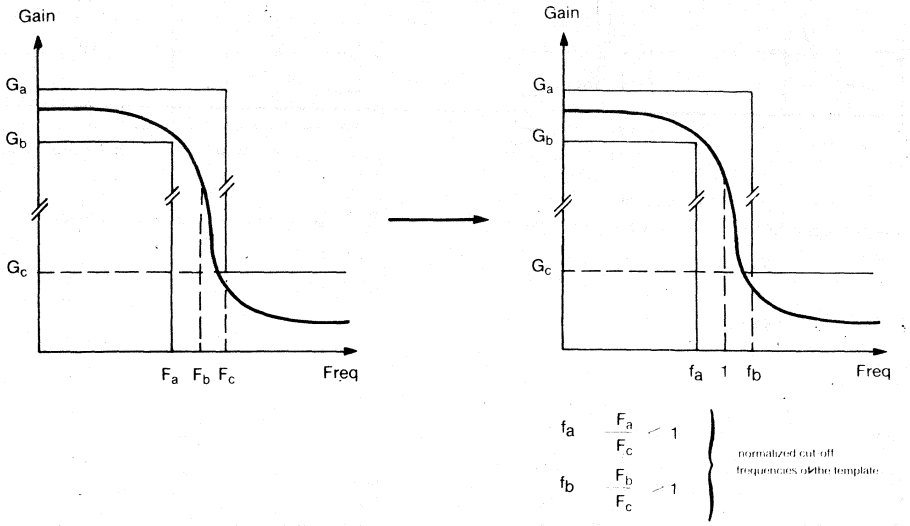
● **PROTOTYPE LOW-PASS FILTER:**

● **Frequency standardization:**

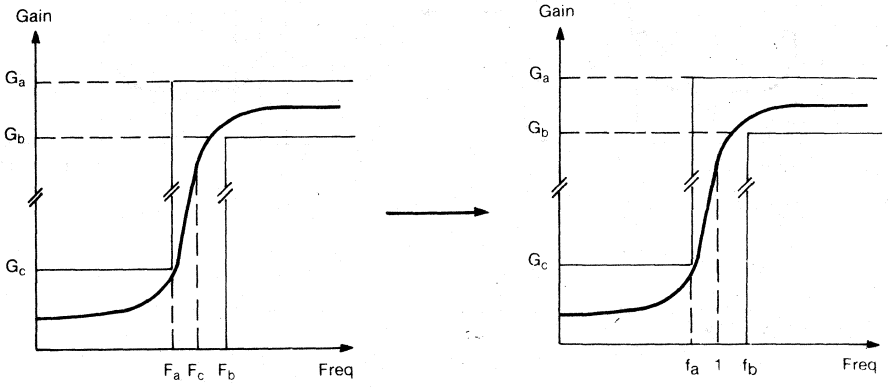
By standardizing the frequency units, the template of any filter may be related back to an template for which only the frequency ratios intervene.

Examples:

— low-pass:

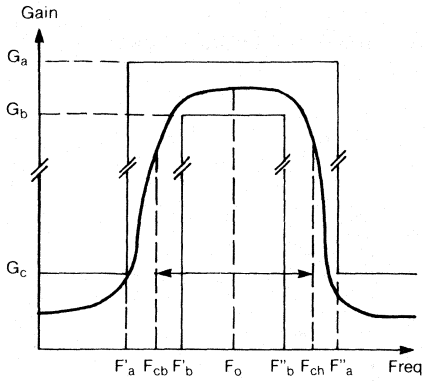


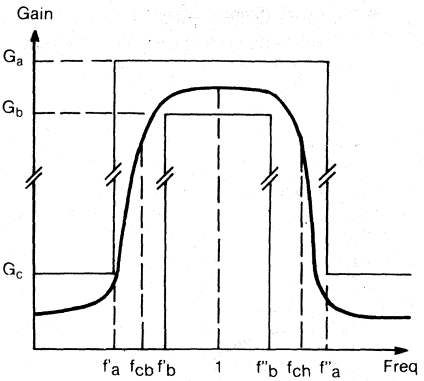
— high-pass:



Same relationships as above

— **bandpass:**





$F_o = \sqrt{F_{cb} \cdot F_{ch}}$ characteristic frequency

B $F_{ch} - F_{cb}$ passband

$\Delta \quad \frac{B}{F_o}$ relative band

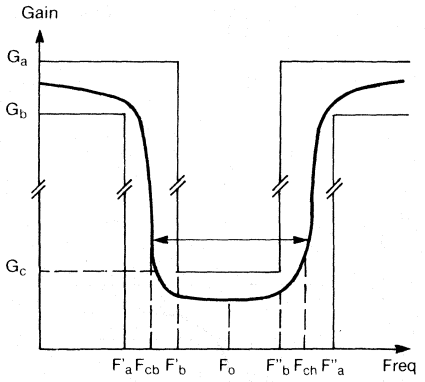
k $\frac{F''_b - F'_b}{F''_a - F'_a}$ selectivity factor

$f'_a = \frac{F'_a}{F_o} < 1$ $\qquad f''_a = \frac{F''_a}{F_o} > 1$

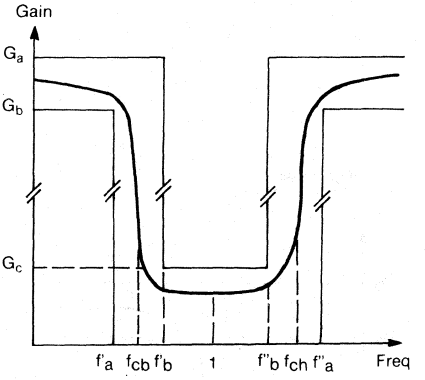
$f_{cb} = \frac{F_{cb}}{F_o} < 1$ $\qquad f_{ch} = \frac{F_{ch}}{F_o} > 1$

$f'_b = \frac{F'_b}{F_o} < 1$ $\qquad f''_b = \frac{F''_b}{F_o} > 1$

— **notch:**



Same relationships as above



Same relationships as above

● **Prototype low-pass filter:**

Once the standardizations above have been performed, some transformations allow the high-pass, bandpass and notch filter template to relate back to that of a so-called "prototype" low-pass filter. These frequency transformations are as follows:

— low-pass ⟶ high-pass:

It consists in replacing p by 1/p in the low-pass filter transfer function. Thus, conversion from the low-pass template to the high-pass template is performed in the following way:

$f_a \longrightarrow f'_a \quad 1/f_a$

$f_b \longrightarrow f'_b \quad 1/f_b$

— low-pass ⟶ bandpass:

It consists in replacing p by $\frac{1}{\Delta} \cdot (p + 1/p)$ in the low-pass filter transfer function. Thus, conversion from the low-pass template to the bandpass template is performed in the following way:

$f_{cb} \cdot f_{ch} \quad f'_a \cdot f''_a = f'_b \cdot f''_b = 1$

— low-pass ⟶ notch filter:

It consists in replacing p by $\frac{1}{\frac{1}{\Delta} \cdot (p + 1/p)}$ in the low-pass filter transfer function. Thus, conversion from the low-pass template to the notch filter template is performed in the following way:

$f_{cb} \cdot f_{ch} = f'_a \cdot f''_a = f'_b \cdot f''_b = 1$

Therefore, in the remaining parts of this notice, all the calculations and examples will be related back to a (prototype) frequency-standardized low-pass filter template, since conversion to the template of any other type of filter can be obtained using the transformations above.

● **FILTER TRANSFER FUNCTION:**

● **General definitions:**

The transfer function is the mathematical representation of the filter amplitude response curve. It is an obligatory intermediate, allowing the calculations of the different filter factors to be carried out. It is expressed as a ratio between the output level and the input level of the filter, in terms of the frequency. This ratio may be expressed as a function of the complex variable p:

$$H(p) = K \frac{N(p)}{D(p)} \qquad (1)$$

with N(p) and D(p): p polynomials.

This expression may therefore be written in the following way:

$$H(p) = K \frac{a_m \cdot p^m + \ldots\ldots + a_1 \cdot p + a_0}{b_n \cdot p^n + \ldots\ldots + b_1 \cdot p + b_0} \qquad (2)$$

In this form, the order of the filter is defined as being equal to the degree of the denominator D(p) (in this case, n). The stability criterium for a filter dictates that the degree of D(p) (the order of the filter) be greater or equal to the degree of N(p). On the other hand, the higher the order of a filter, the more abrupt its cut-off, as can be seen on the relationship providing the asymptotic slope of a filter at the cut-off, in terms of its order:

P = 6.n (dB per octave)

We may also express the transfer function in another way, by replacing the coefficients $a_o, \ldots, a_m, b_o, \ldots, b_n$ by the roots $z_1, \ldots, z_m, p_1, \ldots, p_n$ of the N(p) and D(p) polynomials:

$$H(p) = K \frac{(p - z_1) \cdot \ldots\ldots \cdot (p - z_m)}{(p - p_1) \cdot \ldots\ldots \cdot (p - p_n)} \qquad (3)$$

The zeros of the transfer function are the $z_1, \ldots, z_m$ constants and the poles are the $p_1, \ldots, p_n$, constants. These constants are either real or imaginary-conjugated.

It can be shown that if n is even, the poles of H(p) are all imaginary conjugated, two by two; and that if n is odd, there is a single negative real root. D(p) may therefore be written in the form of a product of 2nd order factors, if n is even; and in the form of a product of 2nd order factors and of a 1st order factor, if n is odd. A new expression can then be obtained for the transfer function:

$$H(p) = K \cdot \frac{(p - z_1) \cdot \ldots \cdot (p - z_m)}{(p - p_0) \cdot (p^2 + 2 \cdot \sigma_1 \cdot p + \rho_1^2) \cdot \ldots \cdot (p^2 + 2 \cdot \sigma_k \cdot p + \rho_k^2)} \quad (4)$$

with $k = \frac{n-1}{2}$ if n is odd, and $k = \frac{n}{2}$ and without $(p - p_0)$ if n is even

It can then be shown that any filter can be obtained by cascading 2nd order cells if n is even, or 2nd order cells and one 1st order cell if n is odd.

- **General transfer function for a 1st order cell:**

It may be expressed as: $H(p) = K \cdot \frac{N(p)}{1 + a \cdot p}$

with: • p complex pulsation
• a time constant

This last parameter allows the cut-off pulsation (and therefore the cut-off frequency) of the cell to be defined as its reciprocal ($\omega_c = 1/a$ and $F_c = 1/(2 \cdot \pi \cdot a)$).

a is a time value such that 3.a (5.a) characterises the time after which the response has reached 95% (99%) of its final value.

Note: The expression of N(p) depends on the type of filter considered:

— polynomial low-pass filter: N(p) = 1

— polynomial high-pass filter: N(p) = p/a (with $p \longrightarrow 1/p$)

- **General transfer function for a 2nd order cell:**

It may be written as follows: $H(p) = K \cdot \frac{N(p)}{1 + 2 \cdot \xi \cdot p/\omega_0 + p^2/\omega_0^2}$

with: — p: complex pulsation
— K: passband transfer factor

— low-pass and high-pass cells:

The relationship above allows the following parameters to be defined:

• the undamped natural pulsation ω_0 (or characteristic pulsation) used as a standardization pulsation (F_0: characteristic frequency)

• the damping factor ξ, magnitude without units specifying the shape of the filter responses:

if $\xi < 0.707$	distinct, transient, ωp pulsation oscillations for the unit response; resonance on the frequency response,
if $0.707 < \xi < 1$	not very distinct, transient oscillations; the final value of the unit response is overstepped. No resonance on the frequency response,
if $\xi = 1$	damping factor critical value,
if $\xi > 1$	no oscillation, aperiodic response without overstepping the final value of the unit response.

• the natural pulsation of the filter $\omega_p = \omega_0 \cdot \sqrt{1 - \xi^2}$ characterising the pulsation of the filter transient oscillations,

• the resonance pulsation $\omega_r = \omega_0 \cdot \sqrt{1 - 2 \cdot \ ^2}$, specifying the resonance position,

• the overvoltage or resonance factor $Q = \frac{|H(j\omega r)|}{|H(O)|} = \frac{1}{2 \cdot \xi \sqrt{1 - \xi^2}}$

specifying the value of the gain of the filter for the resonance pulsation.

• the relative band Δ related to the overvoltage factor by the relationship Q $\frac{1}{\Delta}$

Note: The expression of N(p) depends on the type of filter considered:
— polynomial low-pass filter: N(p) = 1
— polynomial high-pass filter: $N(p) = p^2 / \omega^2$
— low-pass elliptic filter: $N(p) = p^2 + \omega^2_\infty$ with $\omega_\infty > \omega_0$
— high-pass elliptic filter: $N(p) = p^2 + \omega^2_\infty$ with $\omega_\infty < \omega_0$
— bandpass and notch filter cells:

The relationships above are slightly different for a bandpass and notch filter, 2nd order cell. In this case:

- $F_o = \sqrt{F_{cb} \cdot F_{ch}}$ with F_{cb} and F_{ch}: low and high cut-off frequencies of the cell.
- $Q = F_o/\Delta F$ with $\Delta F = F_{ch} - F_{cb}$, called relative band

We may infer from this relationship:

$$Q = \frac{F_{ch} - F_{cb}}{F_o}$$

Note: The expression of N(p) depends on the type of filter considered:

— bandpass filter: $N(p) = 2\xi \cdot p/\omega_0$

— notch filter: $N(p) = p^2 + \omega^2$

• Conclusion

Figure 3 shows the shapes of the amplitude response curves of the 1st and 2nd order low-pass cells, for different values of ξ. Let us keep in mind that a 2nd order filter presenting interesting features is obtained for $\xi = 0.707$. In effect, the transient oscillations and the resonance ($Q > 1$) no longer appear, and the frequency response presents a passband equal to the value $F_0 = \omega_0/(2 \cdot \pi)$.

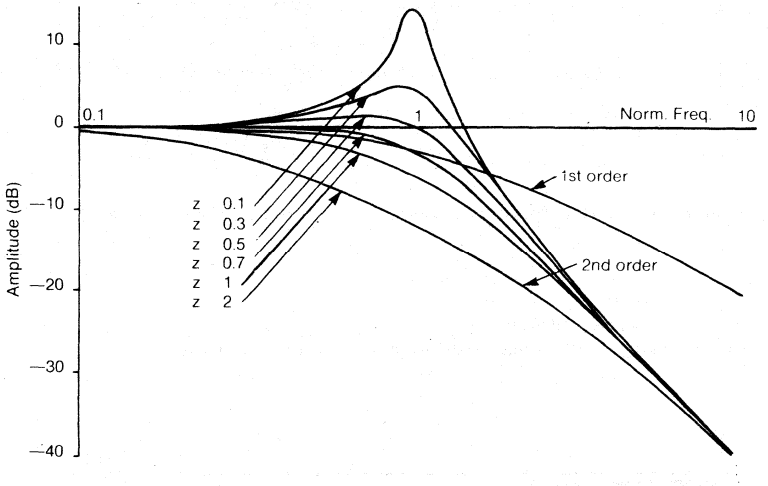


FIGURE3: AMPLITUDE RESPONSE CURVES OF A 1ST AND A 2ND ORDER LOW PASS CELLS IN TERMS OF THE DAMPING FACTOR (CALLED Z ON THIS FIGURE)

• CHARACTERISTIC FUNCTIONS:

The major problem when designing a filter consists in factorising N(p) and D(p), in order to write the transfer function in the form shown on expression 4. To simplify the calculations, it is often preferrable to start from the template considered and to try to have a well known characteristic function pass within it. As there are a great number of functions that may be inscribed within a given template, the selection of one of them will depend on the following features:

— it must be possible to synthesize it

— it must be possible to split it up into a product (or an addition) of functions, and it must be possible to carry each one out

— it must comply with the filter system specifications (phase, group delay,...)

The filter designer must therefore optimize his selection, taking into account all these constraints. A relatively great number of well known characteristic functions simplifies this task.

● **Low-pass polynomial filters:**

Their transfer functions comply with N(p) = 1. The following are the most often used:

— BUTTERWORTH filters:

They correspond to amplitude response curves with the following features (figure 4):

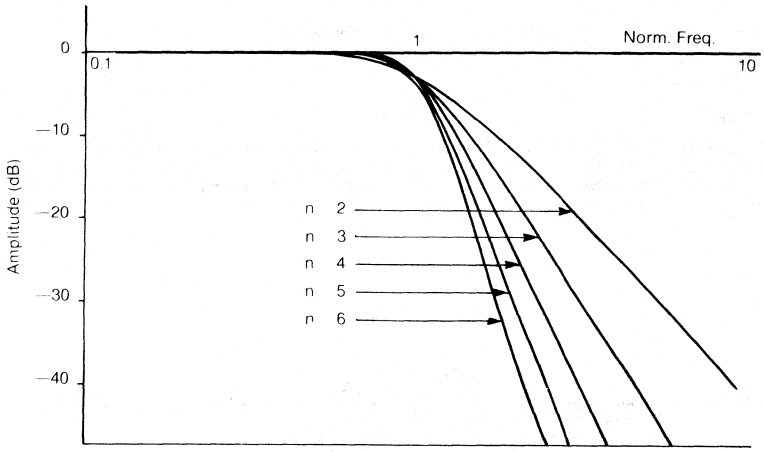


FIGURE 4. AMPLITUDE RESPONSE CURVES OF THE BUTTERWORTH LOW PASS FILTERS

— no ripple within the passband

— not very rapid cut-off near the cut-off frequency.

The phase response curves of these filters present relatively small phase rotations (figure 5).

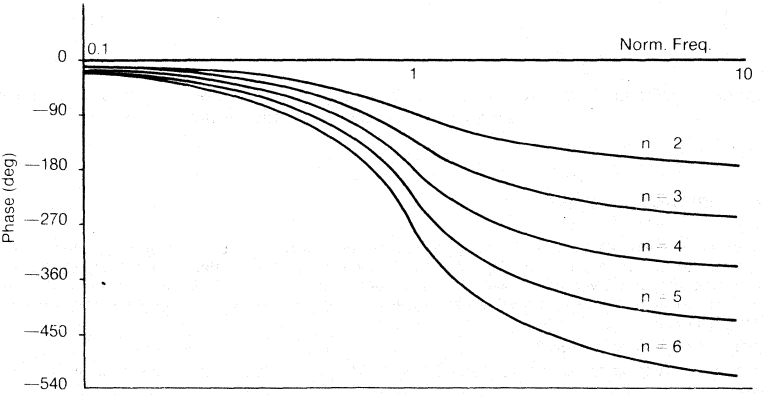


FIGURE 5: PHASE RESPONSE CURVES OF THE BUTTERWORTH LOW PASS FILTERS

The group delays are relatively constant within the passband and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/2 (figure 6).

Note: The higher the order n of the filter, the closer the amplitude response curve will be to the ideal curve (rectangular template).

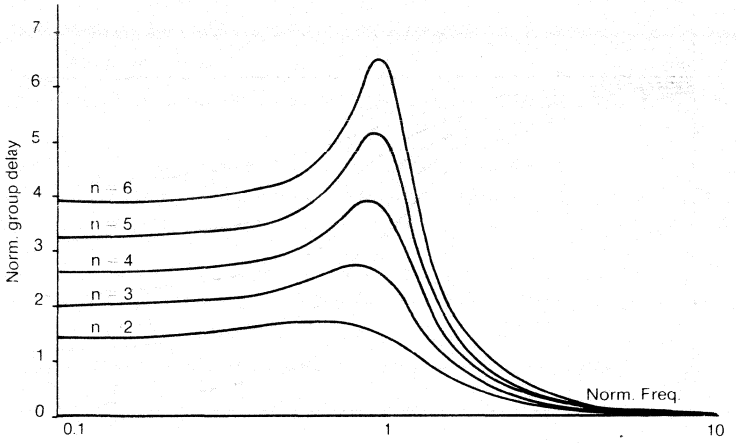


FIGURE 6: GROUP DELAY CURVES OF THE BUTTERWORTH LOW PASS FILTERS

— LEGENDRE filters:

They correspond to amplitude response curves having the following features (figure 7):

— cut-off as rapid as possible near the cut-off frequency

— regular attenuation within the stopband

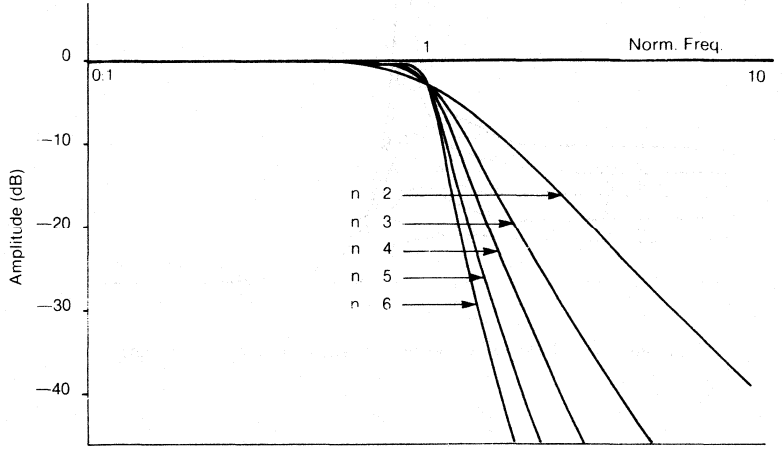


FIGURE 7: AMPLITUDE RESPONSE CURVES OF THE LEGENDRE LOW PASS FILTERS

The phase response curves are practically identical to those of a BUTTERWORTH filter (figure 8). Regarding the group delays for a given order, they are relatively constant within the passband, and their ratio with the group delays for the frequencies around the cut-off frequency is equal to 1/2 (figure 9). But since the slopes of these curves are very steep for this frequency, these time are in general higher than those of the BUTTERWORTH filters.

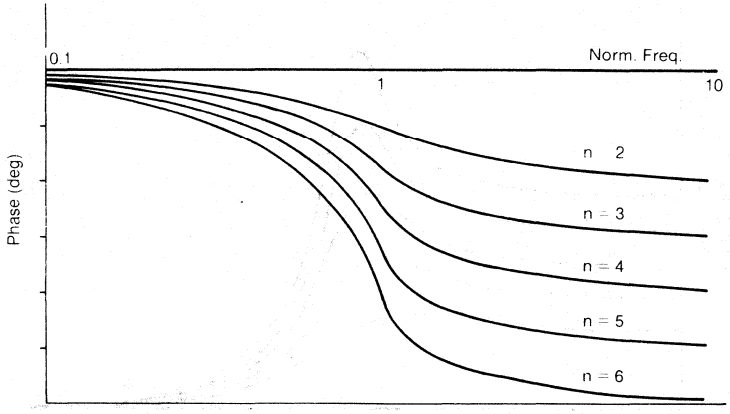


FIGURE 8: PHASE RESPONSE CURVES OF THE LEGENDRE LOW PASS FILTERS

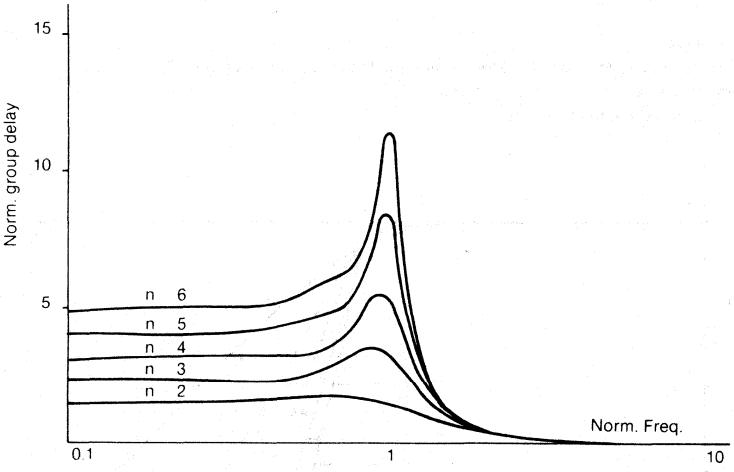


FIGURE 9: GROUP DELAY CURVES OF THE LEGENDRE LOW PASS FILTERS

— CHEBYCHEV filters:

They correspond to amplitude response curves presenting the following features (figure 10):

— ripples within the passband (up to 2dB)

— rapid cut-off near the cut-off frequency (at least in the first octave)

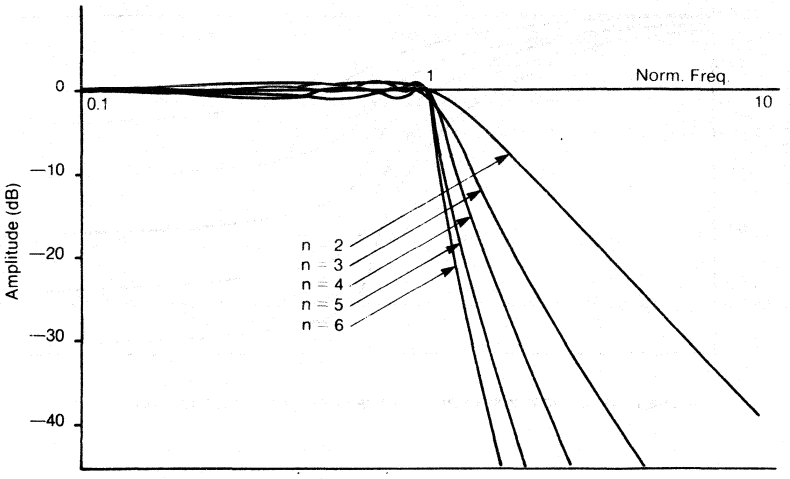


FIGURE 10: AMPLITUDE RESPONSE CURVES OF THE CHEBYCHEV LOW PASS FILTERS

The phase response curves present greater rotations than those of the BUTTERWORTH filters (figure 11). The group delays within the passband are not identical for a given order, and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/3 (figure 12).

Note: The order of a CHEBYCHEV filter is equal to the number of extrema of the amplitude response curves located within the passband.

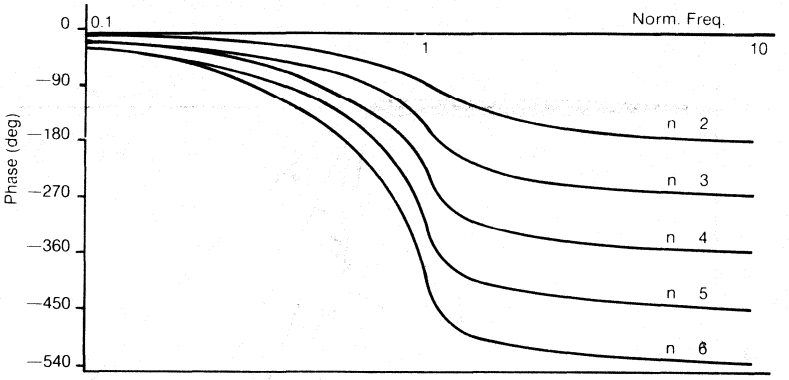


FIGURE 11: PHASE RESPONSE CURVES OF THE CHEBYCHEV LOW PASS FILTERS

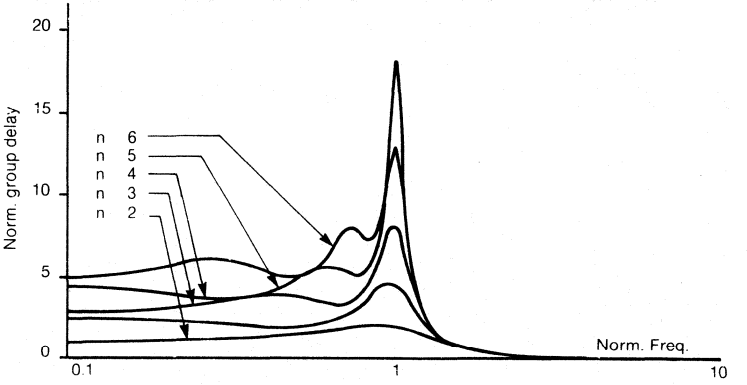


FIGURE 12: GROUP DELAY CURVES OF THE CHEBYCHEV LOW PASS FILTERS

– BESSEL filters:

They correspond to amplitude response curves presenting the following features (figure 13):

– very slow cut-off near the cut-off frequency

– small attenuation within the stopband

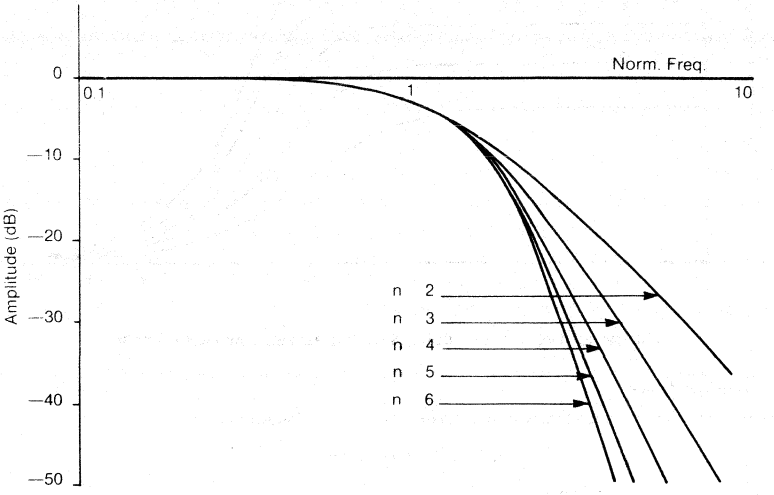


FIGURE 13: AMPLITUDE RESPONSES CURVES OF THE BESSEL LOW PASS FILTERS

The phase response curves are practically identical to those of the BUTTERWORTH filters (figure 14). These filters are mainly interesting because of their group delays, strictly constant within the passband until beyond the cut-off frequency (figure 15). They therefore have a very close to a pure delay characteristic, and they must be used in all applications for which the non-distortion of the signal is an essential factor.

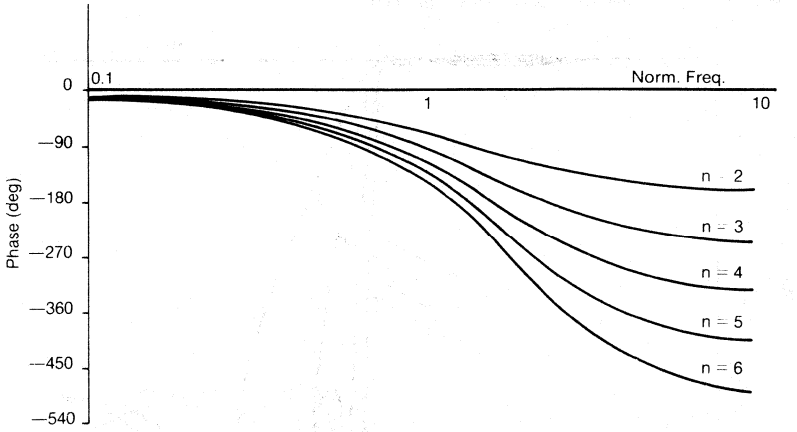


FIGURE 14: PHASE RESPONSE CURVES OF THE BESSEL LOW PASS FILTERS

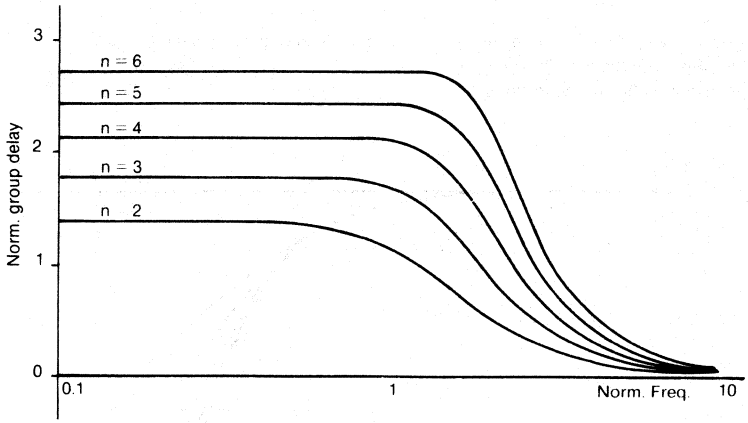


FIGURE 15: GROUP DELAY CURVES OF THE BESSEL LOW PASS FILTERS

● **Low-pass elliptic filters:**

Their transfer functions are such that N(p) may be expressed in the following way:

$$N(p) = (p^2 + \omega_1^2) \ldots\ldots (p^2 + \omega_k^2) \text{ with } \begin{cases} k = \frac{n}{2} \text{ if n is even} \\ k = \frac{n-1}{2} \text{ if n is odd} \end{cases}$$

and ω_1, ..., ω_k: transmission zeros.

— CAUER filters:

They correspond to amplitude response curves presenting the following features (figure 16):

— ripples within the passband
— very rapid cut-off near the cut-off frequency
— presence of one or several transmission zeros (N(p) roots)

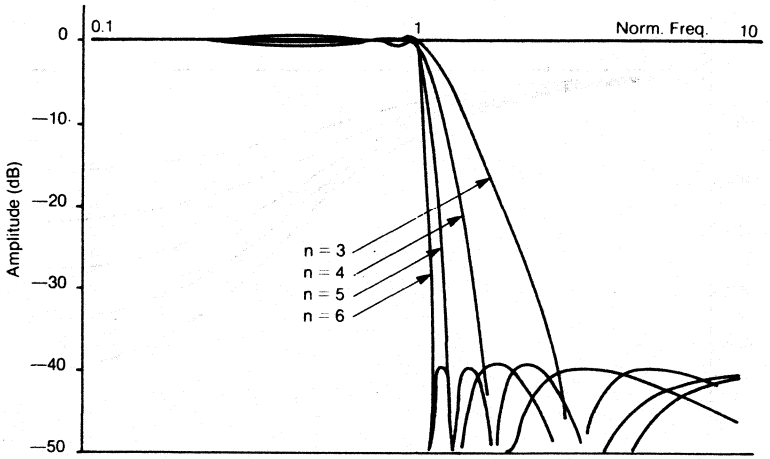


FIGURE 16: AMPLITUDE RESPONSE CURVES OF THE CAUER LOW PASS FILTERS

The phase response curves have greater rotations than the CHEBYCHEV filter ones (figure 17).

The group delays are very different for a given order, from one area of the passband to another, and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/10 (figure 18).

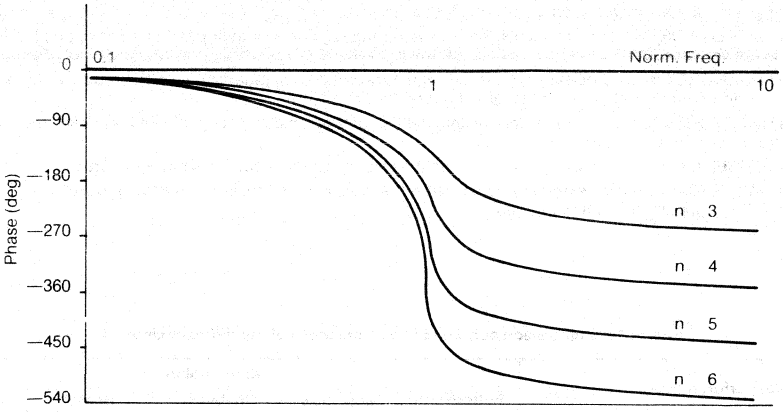


FIGURE17: PHASE RESPONSE CURVES OF THE CAUER LOW PASS FILTERS

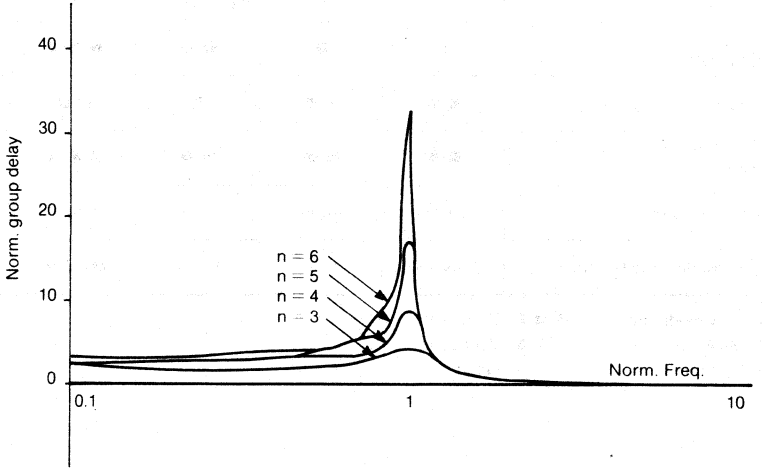


FIGURE 18: GROUP DELAY CURVES OF THE CAUER LOW PASS FILTERS

● **Conclusion:**

A number of nomographs, tables and curves provide, for each type of function and according to its order, the amplitude response curves, the phase response curves, the group delay curves, and also the pulse and step responses. All these characteristics, and a few others, are summarized in the table on figure 19.

Regarding our subject, we will keep in mind the following:

— The BUTTERWORTH filters are interesting because of the regularity of their passband (no ripple) but their cut-off is not very abrupt

— The LEGENDRE filters associate a convenient regularity of the amplitude response curve with a cut-off abruptness and a transient behaviour that are of good quality

— The CHEBYCHEV filters present, at least within the first octave, an abrupt cut-off, but their transient behaviour is not very performing

— The BESSEL filters present a very good transient behaviour, but their cut-off is not very abrupt

— The CAUER filters allow an extremely abrupt cut-off be obtained, but their group delay regularity is mediocre. They present transmission zeros.

Figure 19: Comparison between the performances of the different kinds of filters

Kind of performance	Kind of filter				
	Butterworth	**Legendre**	**Chebychev**	**Bessel**	**Cauer**
Cut-off abruptness for a given order	● ●	●	■ ■	● ● ●	■ ■ ■
Regularity of the amplitude response curve	■ ■ ■	■ ■	Ripple within the passband/ regular within the notch	■ ■	Ripple within the passband and the notch
Regularity of the group delay	■	●	● ●	■ ■ ■	● ● ●
Sensitivity	■ ■	■ ■	●	■ ■	● ●
Transient condition distortions	■ ■	■ ■	● ●	■ ■ ■	● ● ●
Transmission zeros	None	None	None	None	Yes
Required overvoltage factors	Very low	Low	Medium	Medium	High

● ● ● : Very mediocre
● ● : Mediocre
● : Medium

■ ■ ■ : Excellent
■ ■ : Very good
■ : Good

Some ideas concerning filters design

We will assume for the following that the future designer has a comprehensive knowledge of the system specifications of the filter required for his application. We will show briefly how, starting from these system specifications, he may design the filter required. Since this study is beyond the scope of this application specification, this approach will necessarily be very brief.

The design of a filter is performed in four steps:

— determining the characteristic parameters of the filter
— selecting the type of filter
— calculating the filter transfer function
— filter synthesis.

A) DETERMINING THE CHARACTERISTIC PARAMETERS OF THE FILTER:

From the amplitude template related back to the prototype filter template (standardized low-pass), the following parameters are assumed to be known:

— G_a: maximum gain within the passband
— G_b: maximum attenuation within the passband
— G_c: minimum attenuation within the stopband
— k: selectivity
— Δ relative band (only for the bandpass and the notch filters)

The knowledge of these parameters will allow the complete design of the filter to be performed.

B) SELECTING THE TYPE OF FILTER:

We have seen the different features of the BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL and CAUER filters. Let us keep in mind that the main criteria used for selecting a given type of filter are the following:

— the cut-off abruptness
— the passband regularity
— the group delay regularity
— the existence of transmission zeros
— the behaviour under transient conditions
— ...

C) CALCULATING THE FILTER TRANSFER FUNCTION:

Let us assume that the type of filter is known. We must now determine its transfer function. Three steps are required to this end:

a) determining the degree of this function:

The desired amplitude template is related back to the prototype filter template (standardized low-pass); by placing the different response curves of the above filters within this template, we obtain not only a type of filter but also its order, and thereby the degree of the corresponding transfer function.

b) determining the transfer function of the prototype filter:

Depending on the different values of the parameters of the prototype amplitude template desired, a number of nomographs and tables allow the calculation of the transfer function corresponding to this template to be carried out.

c) transposing the transfer function:

If the filter to be designed is not a low-pass (high-pass, bandpass, notch filter), the transfer function determined above may be transposed to the corresponding transfer function, using the transformations defined above.

D) FILTER SYNTHESIS:

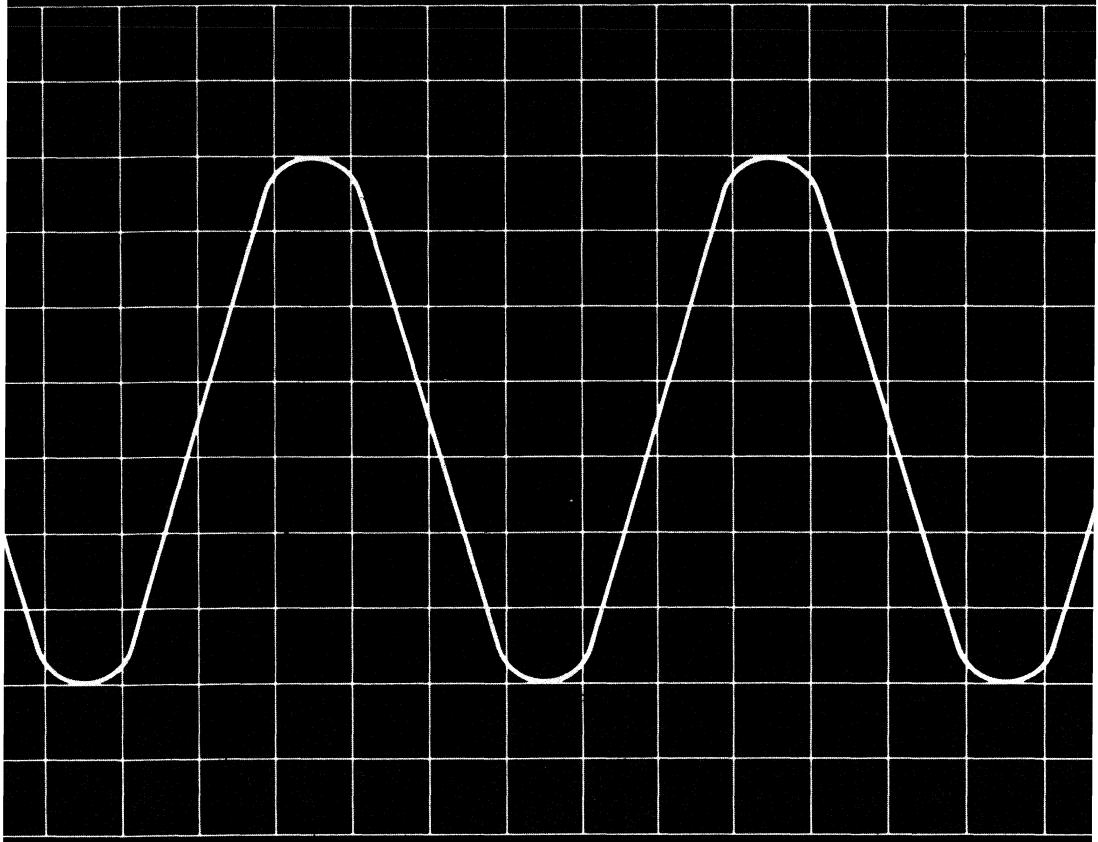
It mainly consists in factorising the final transfer function in the form of a product of 1st and 2nd degree factors. The desired filter may then be easily designed, by cascading the 1st and 2nd order elementary filters corresponding to each of these factors.

Conclusion:

In most — not to say all — electronic applications, the filtering portion has become one of the most important. We have found out that it also was the least well known. By defining all the parameters specified in the system specifications of a filter, and by providing a selection guide amongst the different existing types, we offer anybody who wishes to do so the possibility of making up for lost time, and seeing how this may be inserted into his general application.

MPLEMENTATION AND APPLICATIONS AROUND STANDARD MPF

APPLICATION NOTES AN-061



THOMSON
COMPONENTS
SEMICONDUCTEURS

O. LEENHARDT: Applications laboratory

INTRODUCTION

At a time when increased miniaturisation is the vogue, the problems posed by the filtering of electrical parameters are on an upward trend. The increase in filter order, progressively improved performances mean generally that in order to solve these problems, a considerable increase in components (also generally their size) has to be used. The adjustments in consequence become also more difficult to effect.
In this gloomy context, the advent of switched capacitor techniques has considerably widened the scope of classical filters. Not content to rest here, THOMSON SEMICONDUCTEURS goes even further and offers an even new concept in filtering: the M.P.F. (Mask Programmable Filter).
This application note has therefore several objectives: to explain the switched capacitor principle (application, advantages), to describe the M.P.F. general circuit (structure, block diagram, principal characteristics), to present the THOMSON SEMICONDUCTEURS approach (standard, custom) and to finish by a quick description of all the possible applications of the M.P.F. and more specially one amongst them: the frequency detection.

THE SWITCHED CAPACITOR

Principle:

Consider figure 1. When the switch is in position 1, the charge at the capacitor terminals is $Q1 = C \times V1$.
If the switch is now moved in position 2, the charge at the terminals of C becomes $Q2 = C \times V2$.
This switching allows a charge transfer $Q = Q2 - Q1 = C \times (V2 - V1) = C \times \Delta V$ between the points 1 and 2 of the circuit.
This charge transfer in equivalent to the flow of a current $I = \Delta Q/T = \Delta Q \times F = C \times \Delta V \times F$ where F is the commutating frequency of the switch. ($F = 1/T$)
If we compare now the previous expression with Ohm law applied to a resistance ($I = \Delta V/R$), then we can deduce an electrical equivalence between the resistor and the switched capacitor:

$$R = \frac{1}{C \times F}$$

The technique of switched capacitors enables us therefore to simulate resistors with capacitors. Additionnally, the values of these resistors vary with the sampling frequency employed. These two key points offer considerable advantages to this technique.
This relationship leads to an important comment. In effect, the equivalence "transfered charge = discrete quantity of current" is only valid for high switching speeds. This is certainly the case for switched capacitor filters where, in order to avoid aliasing and smoothing problems inherent in all sampling systems, relatively high sampling frequencies are used, sufficiently high, in any case, for the previous relationship to remain valid.

Example of the application with an integrator:

In order to understand the operation of a switched capacitor integrator, consider the case of a standard inverting integrator as shown in figure 2.
Remember that the time constant of this circuit ($\tau = R \times C'$) determines, in active filter circuits, parameters such as bandwith and cut-off frequency.
However, in this example, this time constant presents a major obstacle: the total lack of correlation between the values of R and C'. The eventual variations or drifts of these two values not necessarily moving in the same direction, leads to a relatively high and difficult to handle innacuracy when associated with the values mentioned above.
Consider now the switched capacitor integrator shown in figure 3. According to the equivalence previously mentioned, the time constant of this integrator is equal to:

$$\tau = \frac{C'}{C \times F}$$

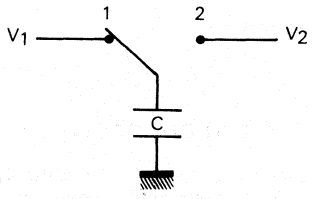


FIGURE 1 - PRINCIPLE OF THE SWITCHED CAPACITOR

1: C produces the charge $Q_1 = C \times V_1$

2: C produces the charge $Q_2 = C \times V_2$

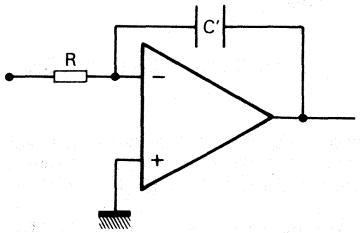
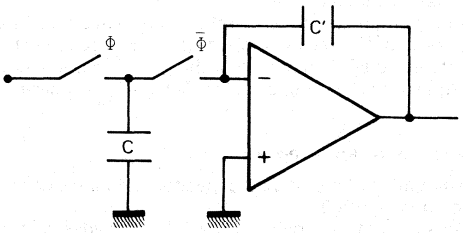


FIGURE 2 - STANDARD INVERTING INTEGRATOR ($\tau = R \times C'$)



where F is the switching frequency

($F = \frac{1}{T}$ with $T = \Phi + \bar{\Phi}$)

FIGURE 3 - SWITCHED CAPACITOR INVERTING INTEGRATOR ($\tau = \frac{C'}{C \times F}$)

Then, we show in a standard integrator, accuracy depends upon the absolute values of the components, when in a switched capacitor integrator, only the relative values are considered.

Advantages of the switched capacitor technique:

The preceeding result shows three major advantages.
The first concerns the relative ease with which an MOS technology can supply excellent precision of capacitor ratio (0.1%). Also, since it is not difficult to obtain good sampling frequency accuracy, the accuracy of the global time constant can attain, with the switched capacitor technique and no external adjustments, values better than 0.5%. It is this precision that we find over the complete frequency range of M.P.F.
The second advantage concerns the equivalence "resistance = switched capacitor" and the possibility offered by this relationship of being able to integrate, in MOS technology, high values of resistance on a small surface area.
Finally, the use of a clock offers considerable scope for modification of the time constant by simple sampling frequency adjustment. Since this time constant is proportional to the cutt-off frequency, we can deduce that a constant ratio exists between the sampling frequency and the cut-off frequency of the M.P.F. It is possible therefore, using this technique, to offset the cutt-off frequency of the M.P.F. by simply modifying the sampling frequency. This last point highlights the extreme flexibility of use of the M.P.F.
Other advantages of equal importance such as the almost total absence of external components, low power consumption, no adjustment and high temperature stability confer on the M.P.F. extreme flexibility of use and very high operating reliability.

THE TS85XX PRODUCT

The M.P.F. structure:

The problems encountered now in filtering (varied requirements, prohibitive costs, long lead times) lead THOMSON SEMICONDUCTEURS to choose a pre-diffused technique where the final characterization of the filter is defined by the interconnection mask (last level of masking).
This structure, shown in figure 4, consists of 8 elementary cells each formed by a switched capacitor integrator and two capacitor areas CE and CI. Each area contains a high number of incremental capacitors each of value 0.1 pF. Thus, according to the type and filter order of M.P.F. required, the integrators can be interconnected, and according to the "Gain-Frequency" response curve required, the various incremental capacitors are also interconnected. The number of incremental capacitors thus connected varies from one area to another and depends upon the different coefficients of the transfer function that the M.P.F. is required to execute.
N.B.: Generally, the number of integrators interconnected is equivalent to the filter order obtained.

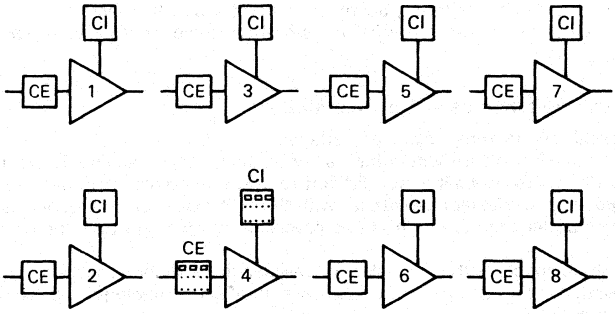


FIGURE 4 - A filtering unit consisting of 8 elementary cells each containing a switched capacitor integrator.
Each capacitance area (CI and CE) contains an optimum number of incremental capacitors of 0.1 pF.

Blockdiagram:

The block diagram of the M.P.F. structure utilised is shown in figure 5. The principal internal functions are:

- a filtering unit composed of 8 switched capacitor integrators interconnectable between each other at the final mask level (interconnection level),
- a clock generator producing the various phases required for the internal switching of the capacitors. These phases are imperatively non-overlapping. The internal clock is obtained via a divider, equally mask programmable, and which matches the external clock defined by the user to that of the M.P.F. As the clock input is TTL compatible, a TTL-MOS level interface is provided, within the circuit, in order to obtain the correct voltage swings,
- a sample and hold unit before the filtering unit,
- a sample and hold amplifier tied to the output of the filtering unit and which enables low impedance signals to be available at the output of the M.F.P.
- the adjustment of the DC ouput level of the M.P.F. by an external voltage source (for example a divider connected between the positive and the negative power supplies and whose mid-point is connected to the LVL pin of the M.P.F.),
- two general purpose and independant operational amplifiers available and destined to be used by the customer for other applications associated with the M.P.F. (anti-aliasing, smoothing, comparator, oscillator,...) in association with external components (R, C, crystal),
- the adjustment of the power consumption of the filter by means of the external resistance tied between the positive supply terminal V^+ (or ground) and the corresponding pin of the circuit (PWF). The power consumption can thus be choosen to match the particular application.
The stand-by mode is obtained by strapping pin PWF to the negative supply terminal V^-,
- the adjustment of the power consumption of the two operational amplifiers, obtainable exactly as for the previous case but via the pin PWA of the circuit.

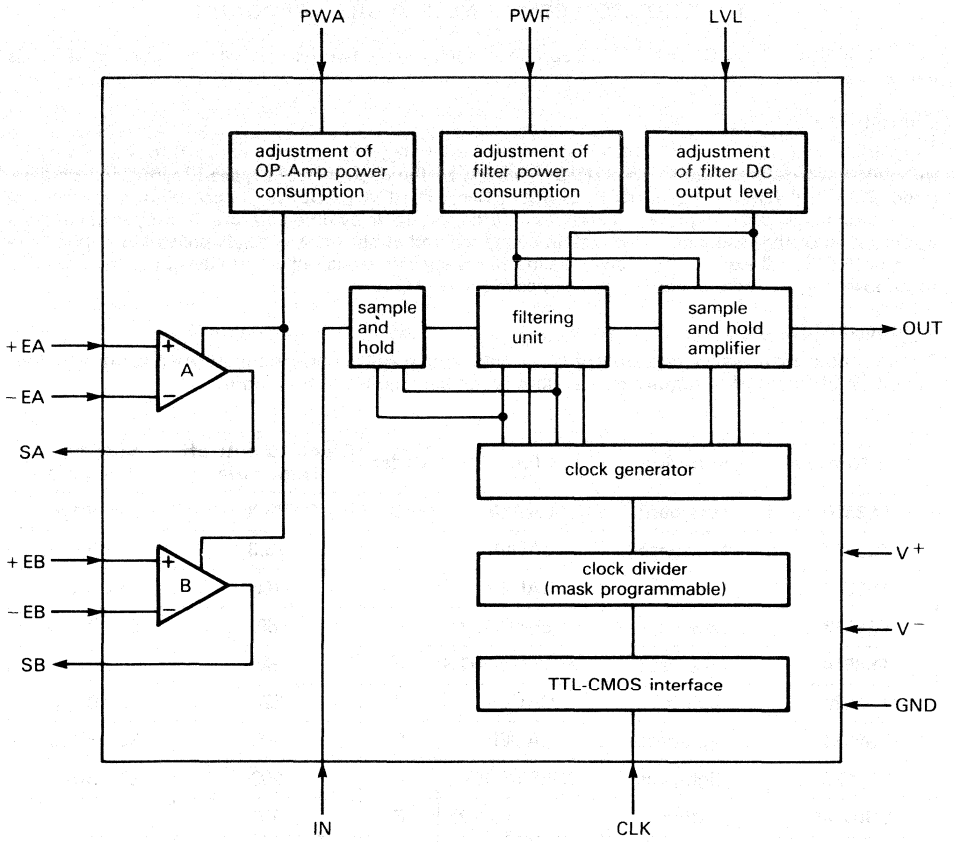


FIGURE 5 - BLOCK DIAGRAM OF THE CONSTRUCTION CHOSEN BY THOMSON-SEMICONDUCTEURS

Principal characteristics:

The principal characteristics of product TS85XX are as follows:

- technology: HCMOS1 (high density linear CMOS)
- available order: 2 to 8 (whatever the type of M.P.F.)
- input signal frequency: 0 to 30 kHz
- internal sampling frequency: 0.5 to 1000 kHz (depends upon the M.P.F. under consideration)
- ratio between internal sampling frequency and cut-off frequency: 10 to 200 (depends upon the M.P.F. under consideration)
- response curves (amplitude and phase) translatable by changing the sampling frequency
- signal to noise ratio: 70 to 85 dB (depends upon the internal construction of the M.P.F.)
- power supply: ±5 V or 0-10 V
- power consumption adjustable from 0.5 to 20 mW per order
- capacitor ratio tolerance: 0.1%
- cut-off frequency tolerance: 0.5% (max)

THE THOMSON SEMICONDUCTEURS APPROACH

The THOMSON SEMICONDUCTEURS approach is to produce two types of M.P.F.: custom M.P.F.'s and standard M.F.P.'s.

Custom M.P.F.'s:

THOMSON SEMICONDUCTEURS undertakes to deliver the first samples within 6 to 8 weeks maximum after the definition of the overall specification by the customer. All types of filters can be designed (BUTTERWORTH, LEGENDRE, BESSEL, CHEBYCHEV, CAUER,...) according to the general applications (low-pass, high-pass, band-pass, notch, group delay time correctors) or by simultaneous optimisation of the response curve both in amplitude and in phase. A special application note on the custom M.P.F. will explain later now to define all the specifications required to design a filter and how to choose among them according to the desired application.

Standard M.P.F.'s:

These constitute a family, currently of 11 circuits, which will expand in the future according to the evolution of the market requirements. Here is the description of this family:

Part Number	Function	Type	Order	Clock to cutt-off freq. ratio	Stopband attenuation
TS8510	Low-pass	CAUER	5	75.3	33 dB(typ)
TS8511	Low-pass	CAUER	7	75.3	55 dB(typ)
TS8512	Low-pass	CAUER	7	100	85 dB(typ)
TS8513	Low-pass	CHEBYCHEV	8	60	80 dB(typ)
TS8514	Low-pass	BUTTERWORTH	8	80	74 dB(typ)
TS8530	High-pass	CAUER	3	320	15 dB(typ)
TS8531	High-pass	CAUER	6	400	32 dB(typ)
TS8532	High-pass	CHEBYCHEV	6	500	60 dB(typ)
TS8540*	Notch	(Q = 7)	8	930	
TS8550*	Band-pass	CAUER (Q = 5)	8	60	
TS8551	Band-pass	Q = 35	8	187.2	70 dB(typ)

* Preliminary

N.B.: For other information, please consult the corresponding data sheets.

APPLICATIONS

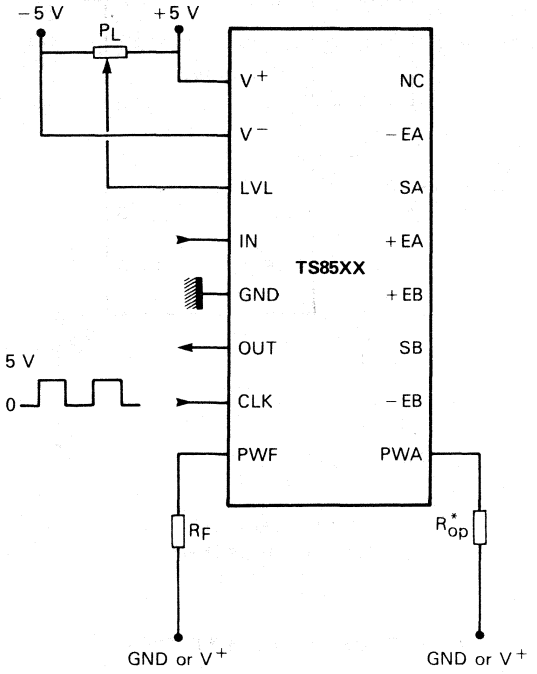
General applications around M.P.F.:

With this new concept of M.P.F., THOMSON SEMICONDUCTEURS is looking to cover all applications covering standard filters (passive, active) involved in the processing of analog signals. Amongst these, telecommunications (modem, PABX, telephone line, signaler, mobil telephone), data acquisition (before A/D conversion and after D/A conversion), speech (detection, analysis, storage), portable instrumentation (geophysics, biomedical) and specially industrial applications (process control, servomotor control, remote control). For all these applications, each filter function is reduced to one M.P.F. derived either from the standard range of M.P.F. or from custom design M.P.F.'s, according to the requirements of the equipment.

Hardware implementation around M.P.F.:

Typical use of the M.P.F. (figure 6):

The M.P.F. is fed in dual supply: ±5 V.
The adjustment of the DC output level of the M.P.F. is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F.). If no output DC adjustment is required, the LVL pin can be directly connected to GND.
The consumption of the filter can be also adjusted by means of an external resistance connected between V^+ (or GND) and the PWF pin of the circuit.
The consumption can thus be chosen to match the particular application.
The stand-by mode is obtained by strapping the PWF pin to V^- (or non connected).
The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V^- (or non connected).
The clock levels are TTL, but CMOS levels are accepted.
With these previous conditions, the output linear dynamic range of the M.P.F. is about 8 V, between −4.5 and 3.5 V.



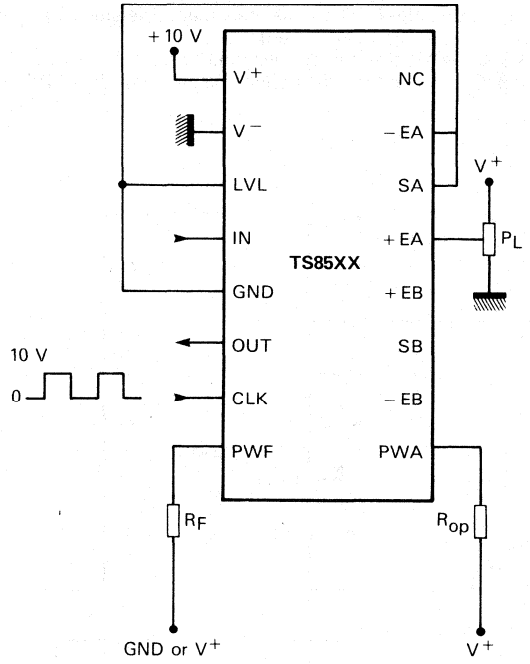
$P_L = 20\ k\Omega$ (multiturn)
$10\ k\Omega \leqslant R_F,\ R_{op} \leqslant 75\ k\Omega$

* If the OP. AMPS. are not used, R_{op} must not be connected between PWA and GND (or V^+).

FIGURE 6 - TYPICAL USE OF THE M.P.F. (±5 V)

Use of the M.P.F. with 0-10 V (figure 7):

The M.P.F. is fed in single supply: 0-10 V.
In this case, V^- is the reference ground of the circuit and GND must be adjusted to +5 V by means of the potentiometer P_L $((V^+ - V^-)/2)$.
The adjustments of the DC output level of the M.P.F., of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.
The high level of the clock must be at least 1.4 V upper the GND level.
With these previous conditions, the output linear dynamic range of the M.P.F. is about 8 V between 0.5 and 8.5 V.

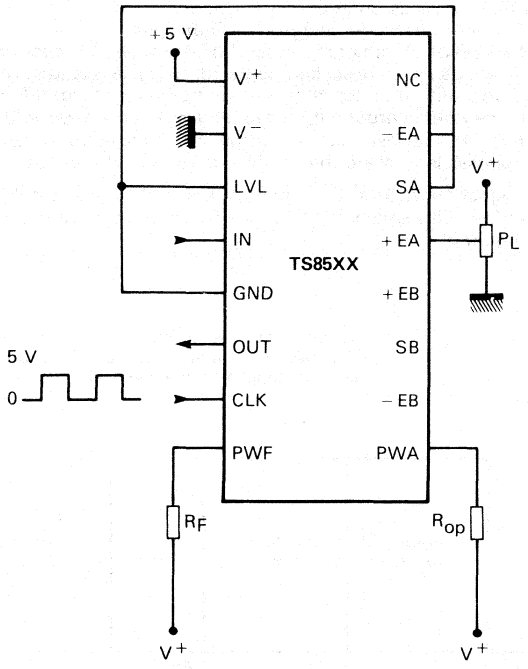


$P_L = 20$ kΩ (multiturn)
10 kΩ ≤ R_F, $R_{op} \leq 75$ kΩ

FIGURE 7 - USE OF THE M.P.F. WITH 0-10 V

Use of the M.P.F. with 0-5 V (figure 8):

The M.P.F. is fed on in single supply: 0-5 V.
In this case, V^- is the reference ground of the circuit and GND must be adjusted to +2.5 V by means of the potentiometer P_L $((V^+ - V^-)/2)$.
The other adjustments are achieved exactly like previously except for bias resistances of the filter and of the operational amplifiers (Rf and Rop), whose must be exclusively connected to V^+.
The clock levels must be TTL levels. With these previous conditions, the output linear dynamic range of the M.P.F. is about 2.2 V, between 1.2 and 3.4 V.



$P_L = 20\ k\Omega$ (multiturn)
$10\ k\Omega \leqslant R_F,\ R_{op} \leqslant 75\ k\Omega$

FIGURE 8 - USE OF THE M.P.F. WITH 0-5 V

Anti-aliasing and smoothing:

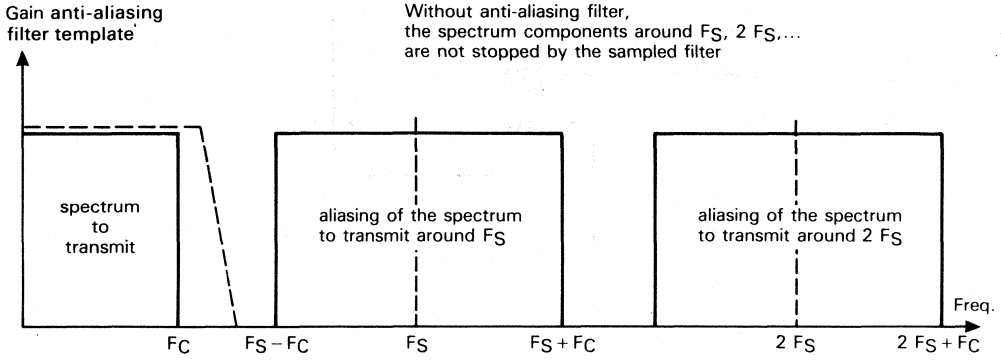
● Anti-aliasing: the switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (Fs) equal, at least, to the double of the upper frequency (Fc) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 9, where the entire spectrum to transmit appears around Fs, 2 Fs, 3 Fs,... and so on. Thus, all spectrum components of the signal contained around these frequencies are transmitted by the M.P.F., oppositively to the desired result.
To cancel the effects of this phenomenon, it is required, before all sampled system, to filter all the spectrum components of the input signal upper than Fs-Fc. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.
The selectivity of this filter depends upon the Fs/Fc ratio.

If Fs/Fc > 200, a RC filter (first order low-pass) is sufficient.

If Fs/Fc < 200, a SALLEN-KEY structure (second order low-pass) must be used.

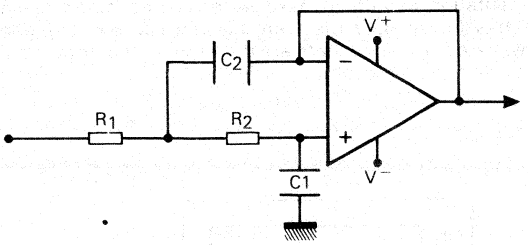
This structure and its relationship are described figure 10. In these relationship, Fc is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and without overvoltage around it, ξ must have a value around 0.7.
N.B. : If Fs/Fc < 2 (figure 11), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.

● Smoothing: as the signal obtained as the output of the M.P.F. is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (figure 9).



● Without anti-aliasing filter: spectrum to transmit ≠ transmited spectrum
● With anti-aliasing filter : spectrum to transmit = transmited spectrum

FIGURE 9 - PHENOMENON OF THE SPECTRUM ALIASING



$R_1 = R_2$ = arbitrary value
F_c = cut-off frequency desired
ξ = damping coefficient

$$C_1 = \frac{\xi}{2\pi R_1 \times F_c}$$

$$(C_1 = \xi^2 \times C_2)$$

$$C_2 = \frac{1}{2\pi\xi R_1 \times f_c}$$

FIGURE 10 - SALLEN-KEY (SECOND ORDER LOW-PASS FILTER) FOR ANTI-ALIASING AND SMOOTHING

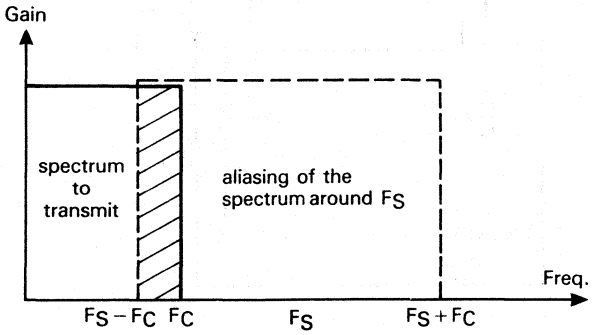
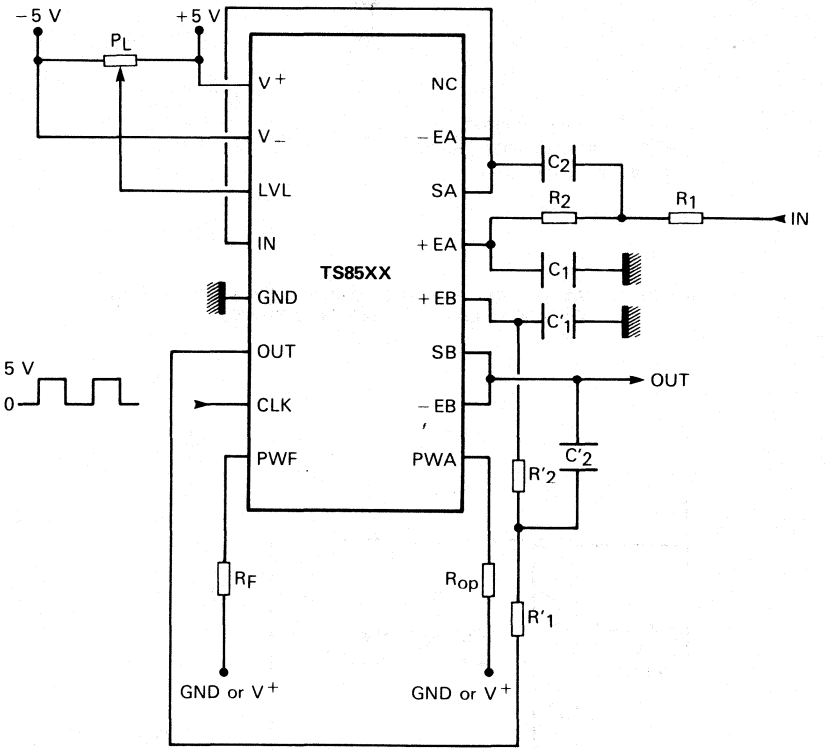


FIGURE 11 - WHEN Fs/Fc<2, THE SPECTRUM COMPONENTS INCLUDING BETWEEN Fs-Fc AND Fc AND WHICH ARE DUE TO SPECTRUM ALIASING ARE NOT STOPPED BY THE SAMPLED FILTER

● Hardware implementation: in order to make easier anti-aliasing and smoothing, THOMSON-SEMICONDUCTEURS has designed, on the even chip of the M.P.F., two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (figure 12).



$P_L = 20\ k\Omega$ (multiturn)
$10\ k\Omega \leqslant R_F,\ R_{op} \leqslant 75\ k\Omega$

R_1, R_2, C_1, C_2 } see anti-aliasing
R'_1, R'_2, C'_1, C'_2 } and smoothing considerations

FIGURE 12 - M.P.F. WITH ANTI-ALIASING AND SMOOTHING FILTERS

On the other hand, it the most M.P.F.'s, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around Fs.
Nonetheless, if the application allow it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator,...).
In this case, the circuit shown figure 13 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described figure 9 (second order low-pass), in the same way as the corresponding relationship.

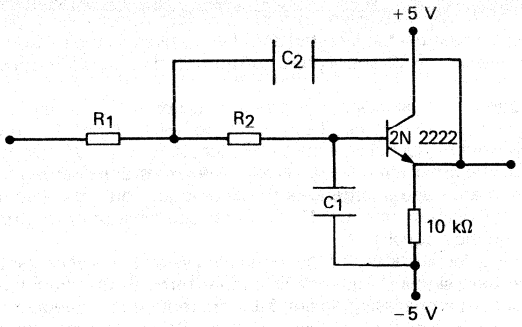


FIGURE 13 - SECOND ORDER LOW-PASS FILTER (SALLEN-KEY STRUCTURE) WITH A TRANSISTOR REPLACING THE OPERATIONAL AMPLIFIER

Implementation of the M.P.F. clock from external components (figure 14):

A mouting with a minimum of external components allows to achieve the clock required for the M.P.F.. The value of the frequency obtained with this mounting depends upon C value, as shown on the following board :

C (nF)	47	15	6.8	2.2	1	0.47	0.33	0.22
F_S min (kHz)	1.5	4.3	6.7	30	44	84	126	172
F_S max (kHz)	16	48	183	305	1020	1750	2430	3010

N.B.: The accuracy of these values is 20%, according to the usual resistor and capacitor accuracy.

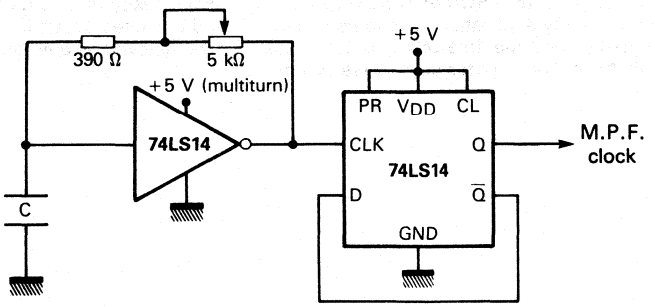


FIGURE 14 - M.P.F. CLOCK ACHIEVED FROM EXTERNAL COMPONENTS

Application example: frequency detection:

The principle of this type of application is as follows: a sinewave (amplitude x, frequency f) modulated by digital information is superposed to an other signal, that we shall call the main signal. To better understand and illustrate this example, we shall take the hypothesis of a main signal equally sinoidal (amplitude X, frequency F) and we shall assume that $X >> x$ and $F < f$ ($T > t$).Thus, the main signal is modulated by frequency f during high level (+ 5 V) and not modulated during low level (0 V) of the bit to be transmitted. These wave trains can, for example, correspond to commands that must be received and then understand by a microprocessor in a suitable format for their processing.
Therefore, these wave trains must be detected and then applied to the microprocessor in form of logic pulse, of which high levels (+ 5 V) correspond to the presence and low levels (0 V) to the absence of the waves.
In this type of application, two factors are of prime consideration, namely: selectivity and size. Both transmission channel and transferred data being prone to noise, the M.P.F. must be adequately selective to reject the unwanted frequencies close to the center frequency f. On the other hand, as far as the industrial aspect of the application is concerned, the size is considered to be of major importance since it is impractical to envisage a large area to accomodate only the filtering section.
Let's consider the general diagram of figure 15. By using a suitable sampling frequency (Fs), the M.P.F. can have a center frequency equal to f.
Since TS8551 is a highly selective filter and the modulated wave has a very stable frequency, the M.P.F. will only filter out the main signal (frequency F) and let through the modulated signal (frequency f). An attenuator stage and an anti-aliasing analog filter are required preceeding the M.P.F. The attenuator stage is used to match the amplitude of the main signal (X) to the input characteristics of the M.P.F., and the analog filter to prevent the M.P.F. from passing the frequency spectrum of the incident wave aliased around Fs. At the output of the M.P.F., the combination of a first order high pass CR filter and a negative voltage clipping diode will produce a sinewave of frequency f and amplitude v. Following this filter, an amplifier of gain $G > 1$ also delivers a sinewave signal of frequency f but of amplitude $V = G \times v$.
The following first order low pass RC filter detects the enveloppe of the amplified signal and then compares it with a reference voltage Vref.
If $V > Vref$, the output of the operational amplifier goes to the positive saturation state (+ Vsat) thereby indicating the presence of the wave, whereas if $V < Vref$, then the amplifier goes to the negative saturation state (− Vsat) to indicate the absence of the wave. A negative voltage clipping diode at the output of the comparator will provide a succession of high (+ 5 V) and low (0 V) states producing a pulse train. The period and the duration of this pulse train inform the microprocessor of the precise nature of control signal sent.

CONCLUSION

This unique example is sufficient to demonstrate the outstanding application possibilities offered by the M.P.F. Many other features were also discussed in various sections of the present article. Relying on these established facts, THOMSON SEMICONDUCTEURS is ready to provide an answer to every filtering problem in any application. Due to its remarkable and unlimited possibilities, the M.P.F. concept is estimated to become, in a very near future, as widely employed as gate-arrays and mask programmable ROM microcomputer devices are nowadays.

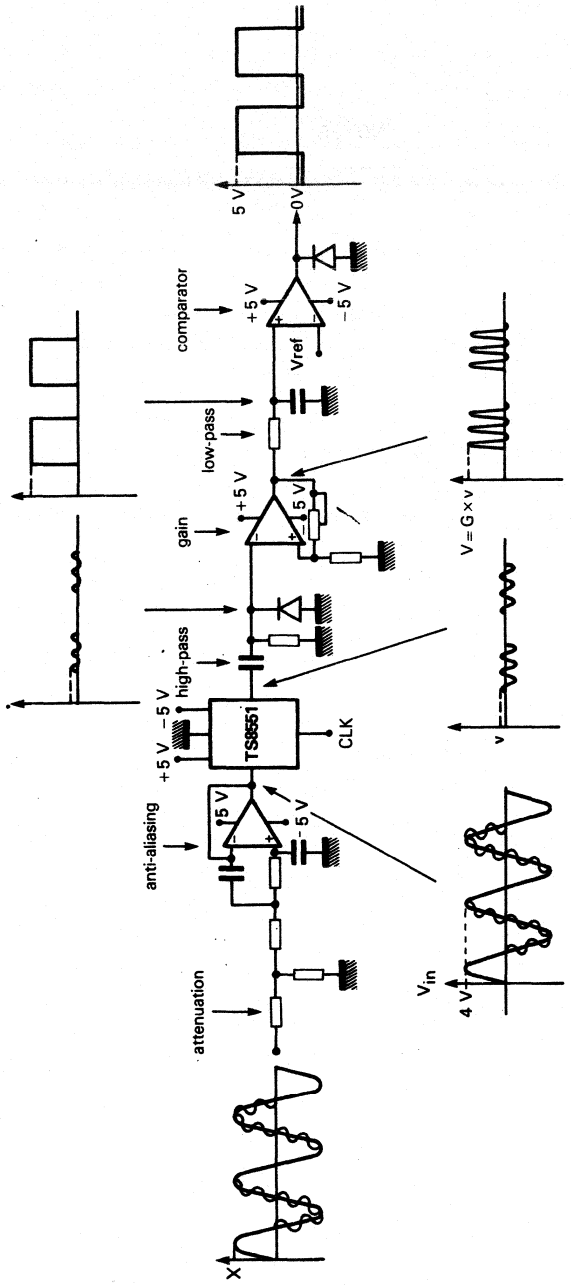


FIGURE 15 - EXAMPLE OF AN APPLICATION OF THE M.P.F. WITH A VERY SELECTIVE BAND-PASS FILTER: THE FREQUENCY TRACKING

These specifications are subject to change without notice
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NOTES

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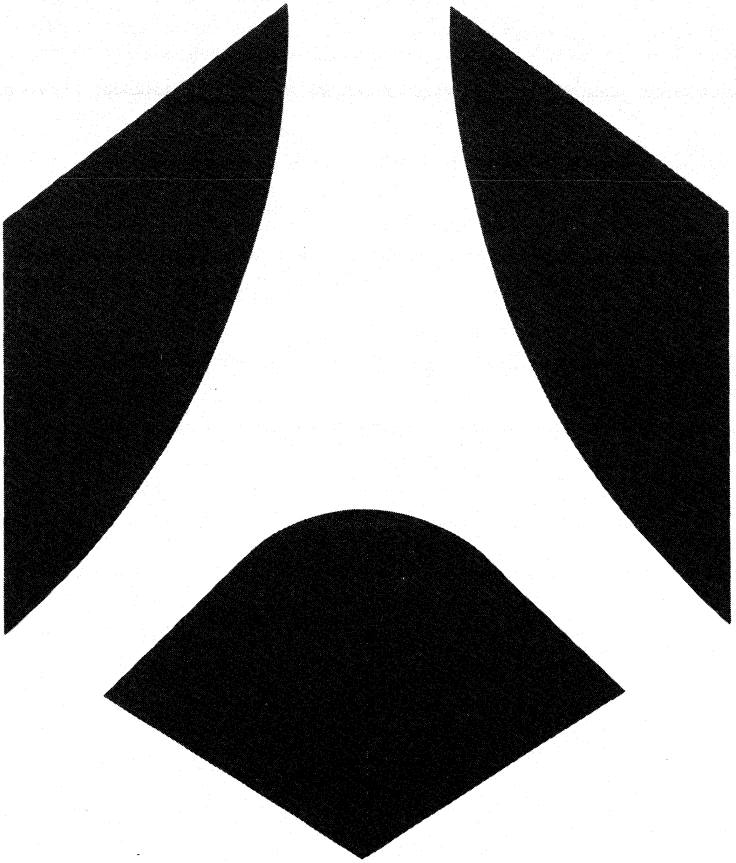
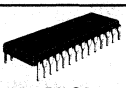
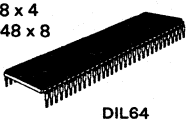


Microprocessors and microcomputers

4 BIT MICROCOMPUTERS

Function	Part number	Characteristic		Package	Page
LOW COST 4-BIT MCUs	ETC9410/9310 ETL9410/9310	With their efficient instruction set (1 byte instruction) and wide I/O option list, these MCUs are designed for home appliances and consumer applications. • One 4-bit SIO • Emulation and development on DEVICE	• RAM: 32 x 4 • ROM: 512 x 8 • 19 I/O lines	DIL24	6-5 6-21
	ETC9411/9311 ETL9411/9311		• RAM: 32 x 4 • ROM: 512 x 8 • 16 I/O lines	DIL20	6-5 6-21
	ETL9413 ETL9313		• RAM: 32 x 4 • ROM: 512 x 8 • 15 I/O lines	DIL20	6-41
	ET9420/9320 ETC9420/9320 ETL9420/9320		• RAM: 64 x 4 • ROM: 1024 x 8 • 23 I/O lines	 DIL28	6-45 6-69 6-91
	ET9421/9321 ETC9421/9321 ETL9421/9321		• RAM: 64 x 4 • ROM: 1024 x 8 • 19 I/O lines	DIL24	6-45 6-69 6-91
	ET9422/9322 ETC9422/9322 ETL9422/9322		• RAM: 64 x 4 • ROM: 1024 x 8 • 15 I/O lines	DIL20	6-45 6-69 6-91
	ETC9444/9344 ETL9444/9344		• RAM: 128 x 4 • ROM: 2048 x 8 • 23 I/O lines	DIL28	6-69 6-115
	ETC9445/9345 ETL9445/9345		• RAM: 128 x 4 • ROM: 2048 x 8 • 23 I/O lines	DIL24	6-69 6-115
MOTOR SPEED CONTROL LOW COST 4-BIT MUCs	TS94104	Well suited for speed measurement, direct triac drive in industrial environment (watchdog feature). Individual clock for MCU, speed measurement timer and triac drive timer. • One 4-bit SIO • Emulation and development on DEVICE	• RAM: 128 x 4 • ROM: 2048 x 8	 DIL64	6-139
	TS94120		• RAM: 64 x 4 • ROM: 1024 x 8 • 23 I/O lines	DIL28	6-153
	TS94144		• RAM: 128 x 4 • ROM: 2048 x 8 • 23 I/O lines	DIL28	6-153

8 BIT MICROCOMPUTERS

Application	Part number	Characteristic	Package	Page
N-MOS LOW COST Single chip microcomputer	EF6804P2	- 8 bits single chip microcomputer. N-MOS. - Pin compatible with EF6805-P2 and EF68HC04-P3. - 1024 bytes user ROM. - 32 bytes RAM. - 64 bytes look-up table ROM. - On chip clock generator. - 8 bit timer with 7 bit software programmable prescaler. - 5V single supply. 28 pins package. - 20 TTL/CMOS compatible bidirectional I/O.	 DIL28 PLCC28	6-237
	EF6804J2	- Similar to EF6804-P2 but with 12 TTL/CMOS compatible bidirectional I/O. - 20 pins package	 DIL20	6-185
C-MOS LOW COST Low power 8 bits	EF68HC04P3	8 bits HC-MOS microcomputer. - EF 6800 based instruction set. - 1644 bytes ROM user program. - 356 bytes self-check ROM program. - 72 bytes ROM data. - 124 bytes RAM/Standby mode. - Power saving stop and wait modes. - 20 TTL/CMOS compatible bidirectional I/O. - 8 bits timer with 7 bits programmable prescaler. - 28 pins package	 DIL28 PLCC28	6-291
	TS68HC04J3	- 8 bits HC-MOS microcomputer Similar to 68HC04P3 with reduced number of I/O. - 12 TTL/CMOS compatible bidirectional I/O. - 20 pins package.	 DIL20	6-289
8 bits N-MOS Microcomputer	EF6805XX	- 6800 based instruction set. - On chip CPU, ROM, RAM, I/O and timer. - Standard DIL plastic package and PLCC versions.		6-345

THOMSON COMPONENTS MICONDUCTEURS

ETC9410 • ETC9411 • ETC9310 • ETC9311

SINGLE SHIP MICROCONTROLLERS

The ETC 9410, C 9411, C 9310, and C 9311, fully Static, Single-Chip CMOS Microcontrollers are fully compatible with the COPS® family, fabricated using double-poly, silicon gate CMOS technology. These Controller Oriented Processors are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The ETC 9411 is identical to the ETC 9410 but with 16 I/O lines instead of 20. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end-product cost.

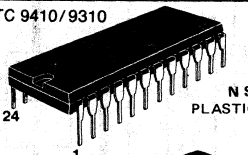
The ETC 9310/C9311 is the extended temperature range version of the ETC 9410/C9411.

- Lowest Power Dissipation (40μW typical)
- Low Cost
- Power saving HALT mode with Continue function
- Powerful Instruction Set
- 512 × 8 ROM, 32 × 4 RAM
- 20 I/O lines (ETC 9410)
- Two-level subroutine stack
- DC to 4 μs instruction time
- Single supply operation (2.4V to 5.5V)
- General purpose and TRI-STATE® outputs
- Internal binary/counter register with MICROWIRE® compatible serial I/O
- LSTTL/CMOS compatible in and out
- Software/hardware compatible with other members of the ET 9400 family
- Extended temperature (– 40°C to + 85°C).

CMOS

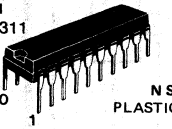
SINGLE CHIP MICROCONTROLLERS

ETC 9410/9310



N SUFFIX
PLASTIC PACKAGE

ETC 9411/9311



N SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT

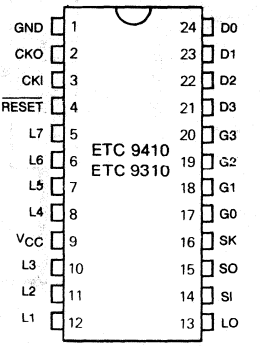


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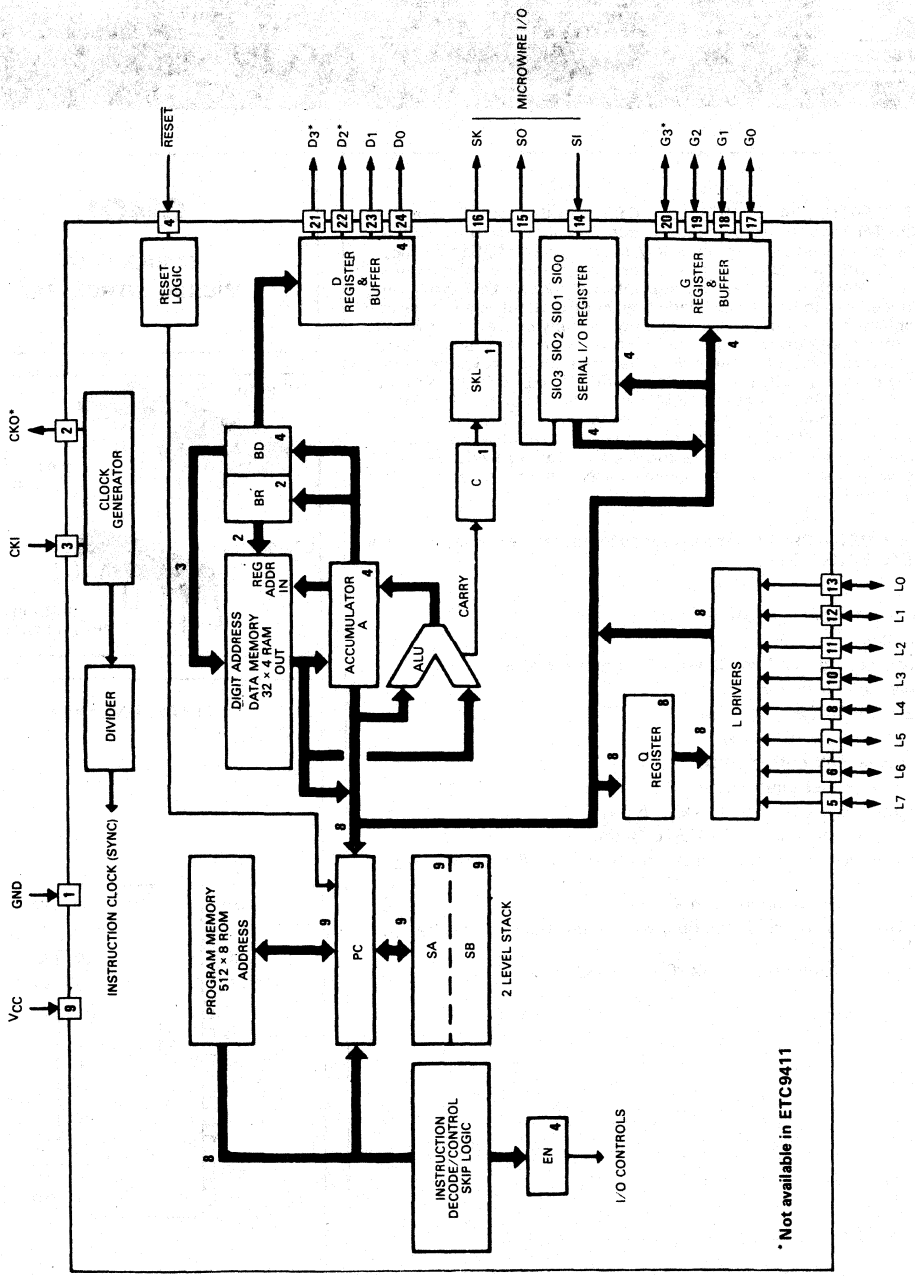
FIGURE 1 – BLOCK DIAGRAM (24-pin version)



ETC 9410 • ETC 9411

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	6V
Voltage at Any Pin Relative to GND	$-0.3V$ to $V_{CC} + 0.3$ V
Ambient Operating Temperature	0°C to + 70° C
Ambient Storage Temperature	− 65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	300° C
Total Source Current	25 mA
Total Sink Current	25 mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $0°C < T_A < +70°C$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Operating Voltage		2.4	5.5	V
Power Supply Ripple (Note 5)	Peak to peak	–	$0.1V_{CC}$	
Supply Current (Note 1)	V_{CC} = 2.4V tc = 125 µs	–	40	µA
	V_{CC} = 5.0V tc = 16 µs	–	500	µA
	V_{CC} = 5.0V tc = 4 µs	–	2000	µA
	(tc is the instruction cycle time)			
HALT Mode Current (Note 2)	V_{CC} = 5.0V Fin = 0kHz	–	15	µA
	V_{CC} = 2.4V Fin = 0kHz	–	6	µA
Input Voltage Levels RESET, CKI				
Logic High		$0.9V_{CC}$	–	V
Logic Low		–	$0.1V_{CC}$	V
All other inputs				
Logic High		$0.7V_{CC}$	–	V
Logic Low		–	$0.2V_{CC}$	V
Hi − Z input leakage		− 1	+ 1	µA
Input capacitance		–	+ 7	pF
Output Voltage Levels	Standard outputs			
LSTTL Operation	V_{CC} = 5.0V ± 5 %			
Logic High	I_{OH} = −25 µA	2.7	–	V
Logic Low	I_{OL} = 400 µA	–	0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 µA	V_{CC}-0.2	–	V
Logic Low	I_{OL} = 10µA	–	0.2	V
Output current levels	(except CKO)			
Sink (Note 6)	V_{CC} = 4.5V, Vout = V_{CC}	1.2	–	mA
	V_{CC} = 2.4V, Vout = V_{CC}	0.2	–	mA
Source (standard option)	V_{CC} = 4.5V, Vout = 0V	0.5	–	mA
	V_{CC} = 2.4V, Vout = 0V	0.1	–	mA
Source (low current option)	V_{CC} = 4.5V, Vout = 0V	30	330	µA
	V_{CC} = 2.4V, Vout = 0V	6	80	µA
CKO (as clock out) current levels				
Sink	V_{CC} = 4.5V, CKI = V_{CC}, Vout = V_{CC}			
divide by 4		0.3	–	mA
divide by 8		0.6	–	mA
divide by 16		1.2	–	mA
Source	V_{CC} = 4.5V, CKI = 0, Vout = 0			
divide by 4		0.3	–	mA
divide by 8		0.6	–	mA
divide by 16		1.2	–	mA

ETC 9410 • ETC 9411

DC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Conditions	Min.	Max.	Units
Allowable Loading on CKO (as HALT)		–	100	pF
Current needed to over-ride HALT	(note 3)			
To continue	V_{CC} = 4.5V, VIN = .2V_{CC}	–	.6	mA
To halt	V_{CC} = 4.5V, VIN = .7V_{CC}	–	1.6	mA
TRI-STATE® or open drain leakage current		–2	+2	µA

ETC 9410 • ETC 9411

AC ELECTRICAL CHARACTERISTICS ($0°C < T_A < +70°C$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Instruction Cycle Time = tc	$V_{CC} \geq 4.5V$	4	DC	µs
	$4.5V > V_{CC} \geq 2.4V$	16	DC	µs
Operating CKI Frequency	4 mode, $V_{CC} \geq 4.5V$	DC	1.0	MHz
	8 mode, $V_{CC} \geq 4.5V$	DC	2.0	MHz
	16 mode, $V_{CC} \geq 4.5V$	DC	4.0	MHz
	4 mode, $V_{CC} \geq 2.4V$	DC	250	kHz
	8 mode, $V_{CC} \geq 2.4V$	DC	500	kHz
	16 mode, $V_{CC} \geq 2.4V$	DC	1.0	MHz
Instruction Cycle Time - CKI (RC) (Note 4)	R = 30k ± 5 %, V_{CC} = 5V C = 82pF ± 5 % (÷ 4 Mode)	8	16	µs
INPUTS : (See Fig. 3)				
t_{SETUP}	G Imputs, $V_{CC} \geq 4.5V$	tc/4 = + 0.7	–	µs
	SI Input, $V_{CC} \geq 4.5V$	0.3	–	µs
	All Others, $V_{CC} \geq 4.5V$	1.7	–	µs
t_{HOLD}	$V_{CC} \geq 4.5V$	0.25	–	µs
	$V_{CC} \geq 2.4V$	1.0	–	µs
OUTPUT				
Propagation delay (see fig. 3)	Vout = 1.5V, C_L = 100pF, R_L = 5K			
t_{PD1}, t_{PD0}	$V_{CC} \geq 4.5V$	–	1.0	µs
t_{PD1}, t_{PD0}	$V_{CC} \geq 2.4V$	–	4.0	µs

Note 1 : Supply current is measured after running for 2000 cycle times with a square -wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20k resistors.

Note 2 : The HALT mode will stop CKI from oscillating in the RC and crystal configurations.

Note 3 : When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

Note 4 : This parameter is only sampled and not 100 % tested.

Note 5 : Voltage change must be less than 0.5 volt in a 1 ms period.

Note 6 : SO output sink current must be limited to keep V_{OL} below 0.2 V_{CC} when port is running in order to prevent entering test mode.

ETC 9310 • ETC 9311

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
Voltage at any pin $-0.3V$ to $V_{CC} + 0.3V$

Total allowable source current 25mA
Total allowable sink current 25mA

Operating temperature range $-40°C$ to $+85°C$
Storage temperature range $-65°C$ to $+150°C$
Lead temperature (soldering, 10 sec.) 300°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $-40°C \leq T_A \leq +85°C$ (Unless otherwise specified).

Parameter	Conditions	Min.	Max.	Units
Operating Voltage		3.0	5.3	V
Power Supply Ripple(Note 5)	Peak to Peak	–	$0.1V_{CC}$	V
Supply Current (Note 1)	$V_{CC} = 3.0V$, $t_c = 125\mu s$ $V_{CC} = 5.0V$, $t_c = 16\mu s$ $V_{CC} = 5.0V$, $t_c = 4\mu s$ (t_c is instruction cycle time)	– – –	60 600 2500	µA µA µA
HALT Mode Current (Note 2)	$V_{CC} = 5.0V$, $F_{IN} = 0kHz$ $V_{CC} = 3.0V$, $F_{IN} = 0kHz$	– –	25 13	µA µA
Input Voltage Levels RESET, CKI Logic High InpuLogic Low All Other Inputs Logic High Logic Low		 $0.9 V_{CC}$ – $0.7 V_{CC}$ –	 – $0.1 V_{CC}$ – $0.2 V_{CC}$	 V V V V
Hi-Z Input Leakage		–2	+2	µA
Input Capacitance		–	7	pF
Output Voltage Levels LSTTL Operation Logic High Logic Low CMOS Operation Logic High Logic Low	Standard Outputs $V_{CC} = 5.0V \pm 5\%$ $I_{OH} = 25\mu A$ $I_{OL} = 400\mu A$ $I_{OH} = -10\mu A$ $I_{OL} = 10\mu A$	 2.7 – $V_{CC} - 0.2$ –	 – 0.4 – 0.2	 V V V V
Output Current Levels Sink (Note 6) Source (Standard Option) Source (Low Current Option)	$V_{CC} = 4.5V$, $V_{OUT} = V_{CC}$ $V_{CC} = 3.0V$, $V_{OUT} = V_{CC}$ $V_{CC} = 4.5V$, $V_{OUT} = 0V$ $V_{CC} = 3.0V$, $V_{OUT} = 0V$ $V_{CC} = 4.5V$, $V_{OUT} = 0V$ $V_{CC} = 3.0V$, $V_{OUT} = 0V$	1.2 0.2 0.5 0.1 30 8	– – – – 440 200	mA mA mA mA µA µA

ETC 9310 • ETC 9311

DC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Conditions	Min.	Max.	Units
CKO Current Levels (As Clock Out)				
Sink ÷ 4	V_{CC} = 4.5V, CKI = V_{CC}, V_{OUT} = V_{CC}	0.3	–	mA
÷ 8		0.6	–	mA
÷16		1.2	–	mA
Source ÷ 4	V_{CC} = 4.5V, CKI = OV, V_{OUT} = OV	0.3	–	mA
÷ 8		0.6	–	mA
÷16		1.2	–	mA
Allowable Loading on CKO (as HALT I/O pin)		–	100	pF
Current Needed to Override HALT (Note 3)				
To Continue	V_{CC} = 4.5V, V_{IN} = 0.2 V_{CC}	–	0.8	mA
To Halt	V_{CC} = 4.5V, V_{IN} = 0.7 V_{CC}	–	2.0	mA
TRI-STATE or Open Drain Leakage Current		- 4	+ 4	µA

ETC 9310 • ETC 9311

AC ELECTRICAL CHARACTERISTICS $-40°C \leq T_A \leq +85°C$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Instruction Cycle Time (t_C)	$V_{CC} \leq 4.5V$	4	DC	µs
	$4.5V > V_{CC} \geq 3.0V$	16	DC	µs
Operating CKI ÷ 4 mode		DC	1.0	MHz
Frequency ÷ 8 mode	$V_{CC} \geq 4.5V$	DC	2.0	MHz
÷ 16 mode		DC	4.0	MHz
÷ 4 mode		DC	250	kHz
÷ 8 mode	$4.5V > V_{CC} \geq 3.0V$	DC	500	kHz
÷ 16 mode		DC	1.0	MHz
Instruction Cycle Time RC Oscillator (Note 4)	R = 30 k ± 5 %, V_{CC} = 5V C = 82pF ± 5 % (÷ 4 Mode)	8	16	µs
Inputs (See Figure 3)				
t_{SETUP} G Inputs		tc/4 + 0.7	–	µs
SI Input	$V_{CC} \geq 4.5V$	0.3	–	µs
All Others		1.7	–	µs
t_{HOLD} $V_{CC} \geq 4.5V$		0.25	–	µs
$V_{CC} \geq 3.0V$		1.0	–	µs
Output Propagation Delay	V_{OUT} = 1.5V, C_L = 100pF, R_L = 5k			
t_{PD1}, t_{PD0} $V_{CC} \geq 4.5V$		–	1.0	µs
t_{PD1}, t_{PD0} $V_{CC} \geq 3.0V$		–	4.0	µs

Note 1 : Supply current is measured after running for 2000 cycle times with a square-ware clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20 k resistors.

Note 2 : The HALT mode will stop CKI from oscillating in the RC and crystal configurations.

Note 3 : When forcing HALT, current is only needed for a short time (approximately 200 ns) to flip the HALT flip-flop.

Note 4 : This parameter is only sampled and not 100 % tested.

Note 5 : Voltage change must be less than 0.5 volt in a 1 ms period.

Note 6 : SO output sink current must be limited to keep V_{OL} below $0.2V_{CC}$ when port is running in order to prevent entering test mode.

FUNCTIONAL DESCRIPTION

To ease reading of this description, only ETC 9410 and/or ETC 9411 are referenced; however, all such references apply equally to ETC 9310 and/or ETC 9311,

A block diagram of the ETC 9410 is given in Figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is logic "1" when a bit is reset, it is a logic "0".

Program Memory

Program memory consists of a 512-byte ROM. As can be seen by an examination of the ETC 9410/C 9411 instruction set, these words may be program instructions, program data, or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID, and LQID instructions, ROM must often be thought of being organized into 8 pages of 64 words (bytes) each.

ROM addressing

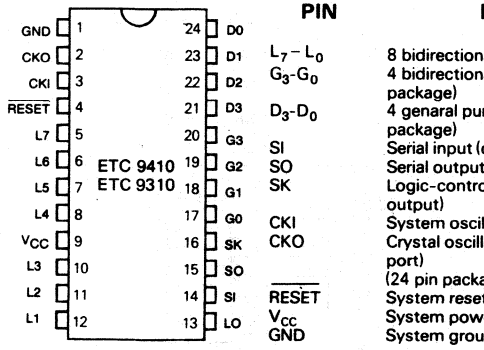
ROM addressing is accomplished by a 9-bit PC register. Its binary value selects one of the 512 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 9-bit binary count value. Two levels of subroutine nesting are implemented by two 9-bit subroutine save registers, SA and SB.

ROM instruction words are fetched, decoded, and executed by the Instruction Decode, Control and Skip Logic circuitry.

Data Memory

Data memory consists of a 128-bit RAM, organized as 4 data registers of 8 × 4-bit digits. RAM addressing is implemented by a 6-bit B register whose upper 2 bits (Br) select 1 of 4 data registers and lower 3 bits of the 4-bit Bd select 1 of eight 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with, the A register (accumulator), they may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the XAD 3,15 instruction. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

The most significant bit of Bd is not used to select a RAM digit. Hence, each physical digit of RAM may be selected by two different values of Bd a shown in Figure 4 below. The skip condition for XIS and XDS instructions will be true if Bd changes between 0 and 15, but NOT between 7 and 8 (see Table 3).



PIN	DESCRIPTION
$L_7 - L_0$	8 bidirectional I/O ports with TRI-STATE®
G_3-G_0	4 bidirectional I/O ports (G_2-G_0 for 20 pin package)
D_3-D_0	4 genaral purpose outputs (D_1-D_0 for 20 pin package)
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)
SK	Logic-controlled clock (or general purpose output)
CKI	System oscillator input
CKO	Crystal oscillator output (or HALT mode I/O port) (24 pin package only)
$\overline{RESET}$	System reset input
V_{CC}	System power supply
GND	System ground

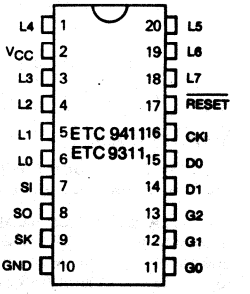


FIGURE 2 – CONNECTION DIAGRAMS

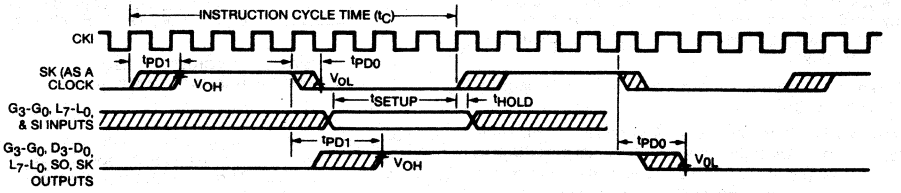


FIGURE 3 – INPUT/OUTPUT TIMING DIAGRAMS (DIVIDE-BY-8 MODE)

The D register provides 4 general purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The XAS instruction copies C into the SKL Latch. In the counter mode, SK is the output of SKL ; in the shift register mode, SK is a sync clock, inhibited when SKL is a logic "0"

The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN3-EN0).

1. The least significant bit of the enable register, EN0, selects the SIO register as either a 4-bit shift register or as a 4-bit binary counter. With EN0 set, SIO is an asynchronous binary counter, DECREMENTING its value by one upon each low going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least 2 (two) instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN3. With EN0 reset, SIO is a serial shift register, shifting left each instruction cycle time. The data present at SI is shifted into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each instruction cycle time. (See 4 below). The SK output becomes a logic controlled clock.
2. EN1 is not used, it has NO effect on the ETC 9410/C 9411.
3. With EN2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN2 disables the L drivers, placing the L I/O ports in a hight impedance input state.
4. EN3, in conjunction with EN0, affects the SO output. With EN0 set (binary counter option selected), SO will output the value loaded into EN3. With EN0 reset (serial shift register option selected), setting EN3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN3 with the serial shift register option selected, disables SO as the shift register output ; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0".

Enable Register Modes — Bits EN_3 and EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = Clock If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = Clock If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

Internal Logic

The internal logic of the ETC 9410/C 9411 is designed to insure fully static operation of the device.

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Bd portion of the register, to load 4 bits of the 8-bit Q latch data and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions of the ETC 9410/C 9411, storing its results in A. It also outputs the carry information to a 1-bit carry register, most often employed to indicate arithmetic overflow. The C registerin conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description below).

The G register contents are outputs to 4 general-purpose bidirectional I/O ports.

The Q register is an internal, latched, 8-bit register, used to hold data loaded from RAM and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction).

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and RAM.

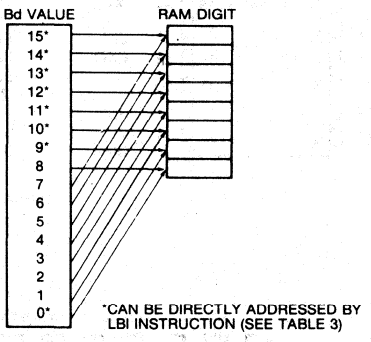


FIGURE 4 – RAM DIGIT ADDRESS TO PHYSICAL RAM DIGIT MAPPING

The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending upon the contents of the EN register. (See EN register description above). Its contents can be exchanged with A, allowing it to input or output continuous serial data stream. With SIO functioning as a serial-in/serial-out shift register and SK as a sync-clock, the ETC 9410/C 9411 is MICROWIRE® compatible.

Initialization

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 1 ms and if the operating frequency at CKI is greater than 32 kHz, otherwise the external RC network shown in Figure 5 must be connected to the RESET pin. The RESET pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the RESET input, providing it stays low for at least three instruction cycle times.

NOTE : If CKI clock is less than 32 kHz, the internal reset logic (option 25 = I) MUST be disabled and the external RC network must be present.

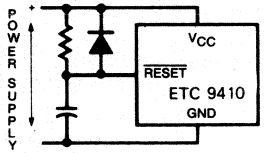


FIGURE 5 – POWER-UP CLEAR CIRCUIT

RC > 5 × Power Supply Rise Time
and RC > 100 × CKI period

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).

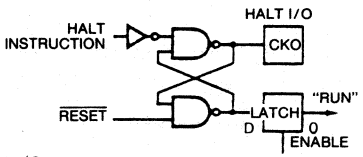
HALT Mode

The ETC 9410/C 9411 is a FULLY STATIC circuit ; therefore, the user may stop the system oscillator at any time to halt the chip. The chip may also be halted by the HALT instruction or by forcing CKO high when it is used as an HALT I/O port. Once in the HALT mode, the internal circuitry does not receive any clock signal, and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The HALT mode is the minimum power dissipation state.

The HALT mode has slight differences depending upon the type of oscillator used.

a) One-pin oscillator - (RC or External)
The HALT mode may be entered into by either program control (HALT instruction) or by forcing CKO to a logic "1" state.
The circuit may be awakened by one of two different methods :
1 - Continue function – by forcing CKO to a logic "0", the system clock is re-enabled and the circuit continues to operate from the point where it was stopped.
2 - Restart - forcing the RESET pin to a logic "0" will re-start the chip regardless of HALT or CKO (see Initialization).

b) Two-pin oscillator - (Crystal)
The HALT mode may be entered into by program control (HALT instruction) which forces CKO to a logic "1" state. The circuit can be awakened only by the RESET function.



HALT I/O port.

ETC 9411

If the ETC 9410 is bonded as a 20-pin package, it becomes the ETC 9411 illustrated in Figure 2, ETC 9410/C 9411 Connection Diagrams. Note that the ETC 9411 does not contain D2, D3, G3, or CKO. Use of this option of course precludes use of D2, D3, G3, and CKO options. All other options are available for the ETC 9411.

CKO Pin Options

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. CKO will be forced high during the execution of a HALT instruction, thus inhibiting the crystal network. If a one pin oscillator system is chosen (RC or external), CKO will be a selected as HALT and is an I/O flip-flop which is an indicator of the HALT status. An external signal can over ride this pin to start and stop the chip. By forcing a high level to CKO; the chip wil stop as soon as CKI is high and the CKO output will go high to keep the chip stopped. By forcing a low level to CKO, the chip will continue and CKO output will go low.

All features associated with the CKO I/O pin are available with the 24-pin package only.

Oscillator Options

There are three options available that define the use of CKI and CKO.

a) Crystal Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 16 (optionally by 8 or 4).

b) External Oscillator. CKI is configured as a LSTTL compatible input accepting an external clock signal. The external frequency is divided by 16 (optionally by 8 or 4) to give the instruction cycle time. CKO is the HALT I/O port.

c) RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is the HALT I/O port.

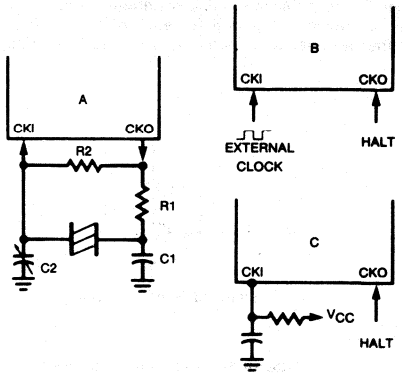


FIGURE 6 – ETC9410C OSCILLATOR

Crystal or resonator

Crystal value	Component Values R1	R2	C1 (pF)	C2 (pF)
32 kHz	220 k	20 M	30	5 36
455 kHz	5 k	10 M	80	40
2.096 MHz	2 k	1 M	30	5 36
4 MHz	1 k	1 M	30	5 36

R/C controlled Oscillator

R	C	Cycle time	V_{CC}
15 k	82 pF	4 to 9 µs	⩾4.5V
30 k	82 pF	8 to 16 µs	⩾4.5V
60 k	100 pF	16 to 32 µs	2.4 to 4.5V

Note : 15k ⩽ R ⩽ 150k ; 50pF ⩽ C ⩽ 150pF

This circuit and these values are for indication only. As the oscillator characteristics are not guaranteed, please consider and examine the circuit constants carefully on your application.

FIGURE 6 – ETC9410 OSCILLATOR

I/O Options

ETC 9410/C 9411 outputs have the following optional configurations, illustrated in Figure 7 :

a) Standard - A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL.

b) Low Current - This is the same configuration as a) above except that the sourcing current much less.

c) Open Drain - An N-channel device to ground only, allowing external pull-up as required by the user's application.

d) Standard TRI-STATE® L Output - A CMOS output buffer similar to a) which may be disabled by program control.

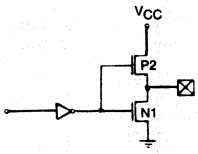
e) Low-Current TRI-STATE® L Output - This is the same as d) above except that the sourcing current is much less.

f) Open-Drain TRI-STATE® L Output - This has the N channel device to ground only.

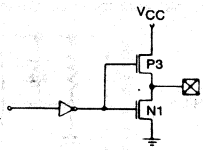
The SI and RESET inputs are Hi-Z inputs (Fig. 7 g)

When using either the G or L I/O ports as inputs, a pull-up device is necessary. This can be an external device or the following alternative is available : Select the low-current output option. Now, by setting the output registers to a logic "1" level, the P-channel devices will act as the pull-up load. Note that when using the L ports in this fashion the Q registers must be set to a logic "1" level and the L drivers MUST BE ENABLED by an LEI instruction.

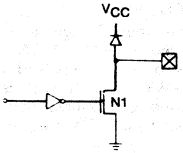
All output drivers use one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{out} V_{out} curves are given in Figure 8 for each of these devices to allow the designer to effectively use these I/O configurations.



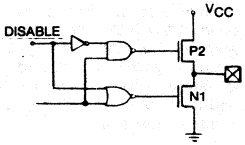
a) Standard Push Pull Output



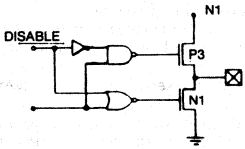
b) Low Current Push-Pull Output



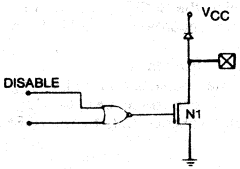
c) Open Drain Output



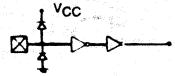
d) Standard TRI-STATE® "L" Output



e) Low Current TRI-STATE® "L" Output



f) Open Drain TRI-STATE® "L" Output



g) Hi-Z Input

FIGURE 7 – I/O CONFIGURATIONS

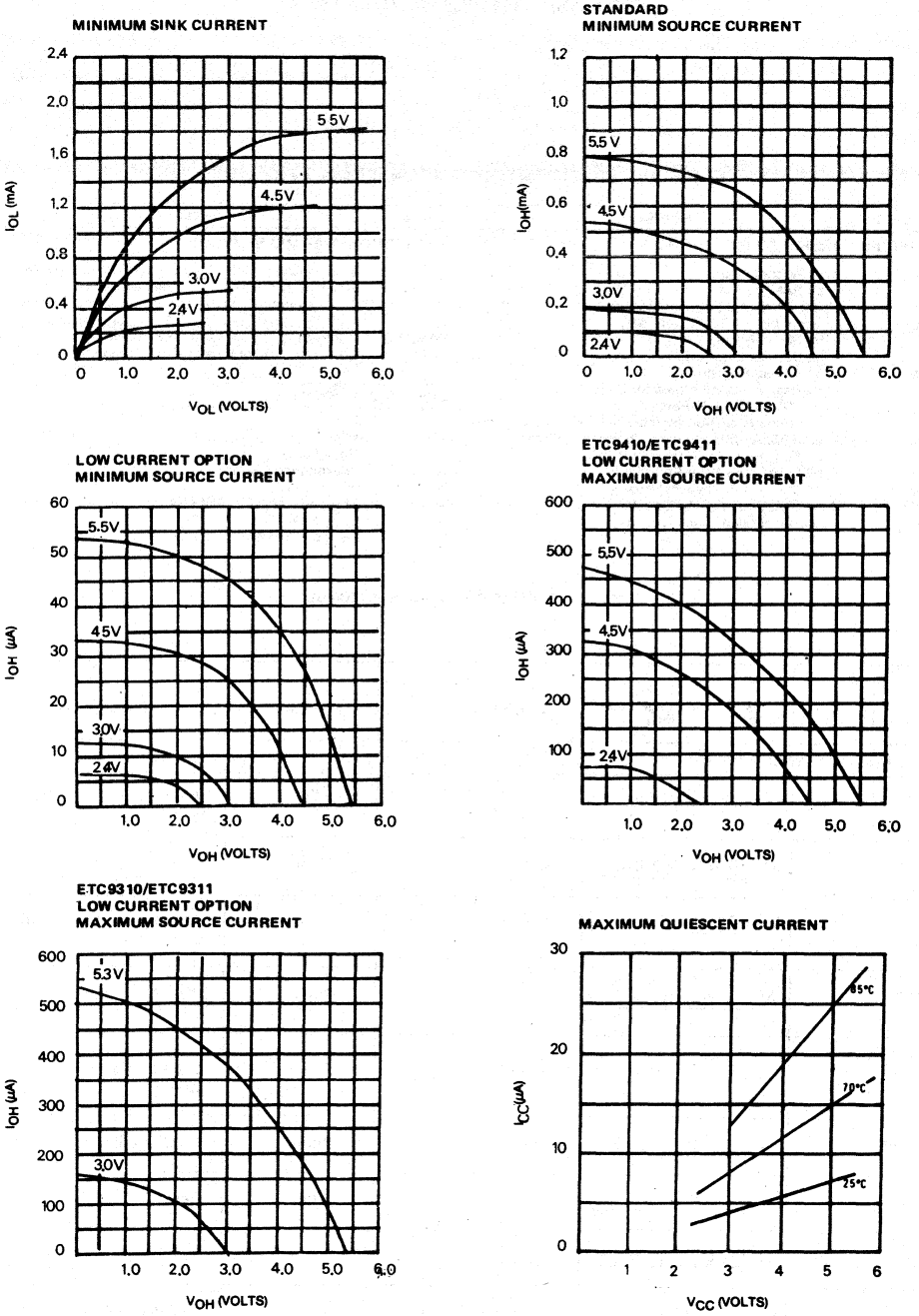


FIGURE 8 – INPUT/OUTPUT CHARACTERISTICS

ETC 9410/C 9411 INSTRUCTION SET

Table 2 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 3 provides the mnemonic, operand, machine, code, data flow, skip conditions and description associated with each instruction in the ETC 9410/C 9411 instruction set.

TABLE 2 – ETC9410/C 9411 INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
L	8-bit TRI-STATE I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
PC	9-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	9-bit Subroutine Save Register A
SB	9-bit Subroutine Save Register B
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0 - 15 binary (RAM Digit Select)
r	2-bit Operand Field, 0 - 3 binary (RAM Register Select)
a	9-bit Operand Field, 0 - 511 binary (ROM Address)
y	4-bit Operand Field 0 - 15 binary (Immediate Data)
RAM(s)	Contents of RAM location addressed by s
ROM(t)	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
—	Minus
→	Replaces
↔	Is exchanged with
=	Is equal to
$\overline{A}$	The one's complement of A
⊕	Exclusive-OR
:	Range of values

TABLE 3 – ETC9410/C 9411 INSTRUCTION SET

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0 0 1 1 | 0 0 0 0	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0 0 1 1 | 0 0 0 1	A + RAM(B) → A	None	Add RAM to A
AISC	y	5-	0 1 0 1 | Y	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CLRA		00	0 0 0 0 | 0 0 0 0	0 → A	None	Clear A
COMP		40	0 1 0 0 | 0 0 0 0	$\overline{A}$ → A	None	one's complement of A to A
NOP		44	0 1 0 0 | 0 1 0 0	None	None	No Operation
RC		32	0 0 1 1 | 0 0 1 0	"0" → C	None	Reset C
SC		22	0 0 1 0 | 0 0 1 0	"1" → C	None	Set C
XOR		02	0 0 0 0 | 0 0 1 0	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A

TABLE 3 – ETC9410/C 9411 INSTRUCTION SET (continued)

TRANSFER OF CONTROL INSTRUCTIONS

JID		FF 1 1 1 1 1 1 1 1	ROM(PC$_{8}$A,M)→PC$_{7:0}$	None	Jum Indirect
JMP	a	6- 0 1 1 0 0 0 0 a$_8$ -- a$_{7:0}$	a→ PC	None	Jump
JP	a	-- 1 a$_{6:0}$ (pages 2,3 only) or -- 1 1 a$_{5:0}$	a→ PC$_{6:0}$ a→ PC$_{5:0}$	None	Jump within Page (Note 1)
JSRP	a	-- 1 0 a$_{5:0}$	PC + 1→ SA→ SB 010→PC$_{8:6}$ a→ PC$_{5:0}$	None	Jump to Subroutine Page (Note 2)
JSR	a	6- 0 1 1 0 1 0 0 a a$_{7:0}$	PC + 1→ SA→ SB a→ PC	None	Jump to Subroutine
RET		48 0 1 0 0 1 0 0 0	SB→ SA→ PC	None	Return from Subroutine
RETSK		49 0 1 0 0 1 0 0 1	SB→ SA→ PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33 0 0 1 1 0 0 1 1 38 0 0 1 1 1 0 0 0		None	Halt processor

MEMORY REFERENCE INSTRUCTIONS

CAMQ		33 0 0 1 1 0 0 1 1 3C 0 0 1 1 1 1 0 0	A→ Q$_{7:4}$ RAM (B)→ Q$_{3:0}$	None	Copy A, RAM to Q
LD	r	-5 0 0 r 0 1 0 1	RAM (B)→ A Br ⊕ r → Br	None	Load RAM into A, Exclusive-OR Br with r
LQID		BF 1 0 1 1 1 1 1 1	ROM(PC$_{8}$A,M)→ Q SA→ SB	None	Load Q Indirect
RMB	0 1 2 3	4C 0 1 0 0 1 1 0 0 45 0 1 0 0 0 1 0 1 42 0 1 0 0 0 0 1 0 43 0 1 0 0 0 0 1 1	0→ RAM (B)$_0$ 0→ RAM (B)$_1$ 0→ RAM (B)$_2$ 0→ RAM (B)$_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 0 1 0 0 1 1 0 1 47 0 1 0 0 0 1 1 1 46 0 1 0 0 0 1 1 0 4B 0 1 0 0 1 0 1 1	1→ RAM (B)$_0$ 1→ RAM (B)$_1$ 1→ RAM (B)$_2$ 1→ RAM (B)$_3$	None	Set RAM Bit
STII	y	7- 0 1 1 1 y	y→ RAM (B) Bd + 1→ Bd	None	Store Memory Immediate and Increment Bd
X	r	-6 0 0 r 0 1 1 0	RAM (B)↔ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	3,15	23 0 0 1 0 0 0 1 1 BF 1 0 1 1 1 1 1 1	RAM (3,15)↔ A	None	Exchange A with RAM (3,15)
XDS	r	-7 0 0 r 0 1 1 1	RAM (B)↔A Bd − 1→Bd Br ⊕ r→Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	-4 0 0 r 0 1 0 0	RAM (B)↔A Bd + 1→Bd Br ⊕ r→Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive Or Br with r

TABLE 3 – ETC9410/C 9411 INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0 1 0 1 0 0 0 0	A → Bd	None	Copy A to Bd
CBA		4E	0 1 0 0 1 1 1 0	Bd → A	None	Copy Bd to A
LBI	r,d		0 0 r (d - 1) (d = 0..9 15)	r,d → B	Skip until not a LBI	Load B Immediate with r,d
LEI	y	33 6-	0 0 1 1 0 0 1 1 0 1 1 0 y	y → EN	None	Load EN Immediate
TEST INSTRUCTIONS						
SKC		20	0 0 1 0 0 0 0 0		C = "1"	Skip if C is True
SKE		21	0 0 1 0 0 0 0 1		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0 0 1 1 0 0 1 1 0 0 1 0 0 0 0 1		$G_{3\,0}$ = 0	Skip if G is Zero (all 4 bits)
SKGBZ		33	0 0 1 1 0 0 1 1	1st byte		Skip if G Bit is Zero
	0	01	0 0 0 0 0 0 0 1	2nd byte	G_0 = 0	
	1	11	0 0 0 1 0 0 0 1		G_1 = 0	
	2	03	0 0 0 0 0 0 1 1		G_2 = 0	
	3	13	0 0 0 1 0 0 1 1		G_3 = 0	
SKMBZ	0	01	0 0 0 0 0 0 0 1		$RAM(B)_0$ = 0	Skip if RAM Bit is Zero
	1	11	0 0 0 1 0 0 0 1		$RAM(B)_1$ = 0	
	2	03	0 0 0 0 0 0 1 1		$RAM(B)_2$ = 0	
	3	13	0 0 0 1 0 0 1 1		$RAM(B)_3$ = 0	
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	0 0 1 1 0 0 1 1 0 0 1 0 1 0 1 0	G → A	None	Input G Ports to A
INL		33 2E	0 0 1 1 0 0 1 1 0 0 1 0 1 1 1 0	$L_{7\,4}$ → RAM(B) $L_{3\,0}$ → A	None	Input L Ports to RAM, A
OBD		33 3E	0 0 1 1 0 0 1 1 0 0 1 1 1 1 1 0	Bd → D	None	Output Bd to D Outputs
OMG		33 3A	0 0 1 1 0 0 1 1 0 0 1 1 1 0 1 0	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0 1 0 0 1 1 1 1	A ⟷ SIO, C → SKL	None	Exchange A with SIO

Note 1 : The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.
Note 2 : A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

The following information is provided to assist the user in uderstanding the operation of several unique instructions and to provide notes useful to programmers in writing ETC 9410 C 9411.

XAS Instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register, above). If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM Addressed by the 9-bit word, PC_8, A, M. PC_8 is not affected by this instruction.

Note That JID requires 2 instruction cycles to execute.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 9-bit word PC_8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB) and replaces the least significant 8 bits of PC as follows : A → $PC_{7:4}$ RAM (B) → $PC_{3:0}$ leaving PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pusches SA → SB, the previous contents of SB are lost. Also, when LQID pops the stack, the previously pushed contents of SA are left in SB. The net result is that the contents of SA are placed in SB (SA → SB). Note that LQID takes two instruction cycle times to execute.

Instruction Set Notes

a) The first word of a ETC 9410/C 9411 program (ROM address 0) must be a CLRA (Clear A) instruction.

b) Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths except JID and LQID take the same number of cycle times whether instructions are skipped or executed. JID and LQID instructions take 2 cycles if executed and 1 cycle if skipped.

c) The ROM is organized into 8 pages of 64 words each. The Program Counter is a 9-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example : a JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3 or 7 will access data in the next group of 4 pages.

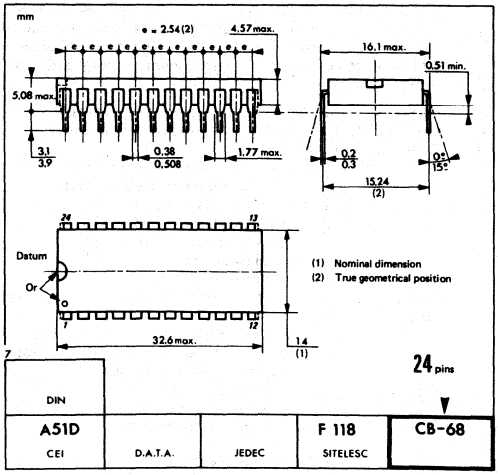
OPTION LIST

The ETC 9410/ETC 9411 mask-programmable options are assigned numbers which correspond with the ETC 9410 pins.

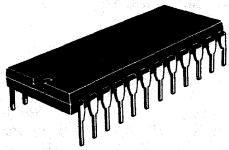
The following is a list of ETC9410 options. When specifying a ETC 9411chip, Options 20, 21, and 22 must be set to 0. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 : = 0 : Ground Pin. No options available.
Option 2 : CKO I/O Port. Determined by Option 3
Option 3 : CKI Input
= 0 : Crystal controlled oscillator input (÷ 4).
= 1 : Single-pin RC-controlled oscillator (÷ 4).
= 2 : External oscillator input (÷ 4).
= 3 : Crystal oscillator input (÷ 8).
= 4 : External oscillator input (÷ 8).
= 5 : Crystal oscillator input (÷ 16).
= 6 : External oscillator input (÷ 16).
Option 4 : RESET Input = 1 : Hi-Z input. No option available
Option 5 : L_7 Driver
= 0 : Standard TRI-STATE push-pull output
= 1 : Low-current TRI-STATE push-pull output
= 2 : Open-drain TRI-STATE output
Option 6 : L_6 Driver. (Same as Option 5.)
Option 7 : L_5 Driver. (Same as Option 5.)
Option 8 : L_4 Driver. (Same as Option 5.)
Option 9 : V_{CC} Pin.
Option 10 : L_3 Driver. (Same as Option 5.)
Option 11 : L_2 Driver. (Same as Option5.)
Option 12 : L_1 Driver. (Same as Option 5.)
Option 13 : L_0 Driver. (Same as Option 5.)
Option 14 : SI Input.
No option available.
= 1 : Hi-Z input
Option 15 : SO Output.
= 0 : Standard push-pull output.
= 1 : Low-current push-pull output.
= 2 : Open-drain output
Option 16 : SK Driver. (Same as Option 15.)
Option 17 : G_0 I/O Port. (Same as Option 15.)
Option 18 : G_1 I/O Port. (Same as Option 15.)
Option 19 : G_2 I/O Port. (Same as Option 15.)
Option 20 : G_3 Output. (Same as Option 15.)
Option 21 : D_3 Output. (Same as Option 15.)
Option 22 : D_2 Output. (Same as Option 15.)
Option 23 : D_1 Output. (Same as Option 15.)
Option 24 : D_0 Output. (Same as option 15.)
Option 25 : Internal Initialization logic.
= 0 : Normal operation.
= 1 : No internal initialization Logic
Option 26 : No option available.
Option 27 : Chip Bonding
= 0 : ETC 9410 (24-pin device).
= 1 : ETC 9411 (20-pin device).
= 2 : ETC 9410 and ETC 9411.

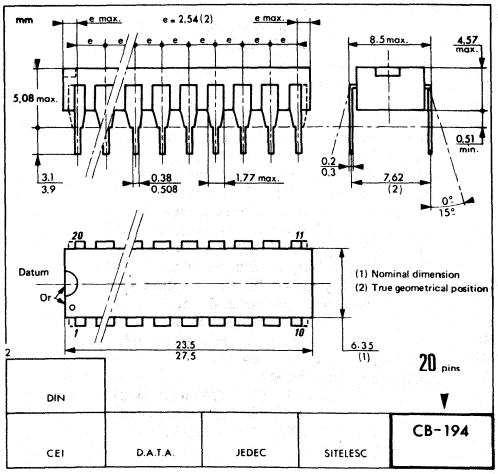
PHYSICAL DIMENSIONS



CB-68



N SUFFIX
PLASTIC PACKAGE



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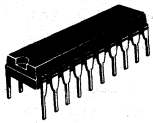

N SUFFIX
PLASTIC PACKAGE

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THOMSON COMPONENTS SEMICONDUCTEURS

ETL9410 • ETL9411 • ETL9310 • ETL9311

SINGLE SHIP MICROCONTROLLERS

The ETL9410 and ETL9411 Single-Chip N-Channel Microcontrollers are fully compatible with the COPS® family, fabricated using N-channel, silicon gate MOS technology. The Controller Oriented Processors are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The ETL9411 is identical to the ETL9410, but with 16 I/O lines instead of 19. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end-product cost.

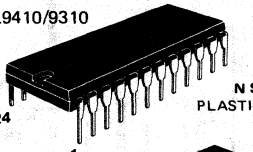
The ETL9310 and ETL9311 are exact functional equivalents but extended temperature versions of ETL9410 and ETL9411 respectively.

- Low cost
- Powerful instruction set
- 512 × 8 ROM, 32 × 4 RAM
- 19 I/O lines ETL9410 - COP
- Two-level subroutine stack
- 16μs instruction time
- Single supply operation (4.5 - 6.3V)
- Low current drain (6mA max.)
- Internal binary counter register with MICROWIRE® serial I/O capability
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS compatible in and out
- Direct drive of LED digit and segment lines
- Software/hardware compatible with other members of ET9400 family
- Extended temperature range device ETL9310 ETL9311 (-40° C to + 85° C)
- Wider supply range (4.5 - 9.5V) optionally available

NMOS

SINGLE CHIP MICROCONTROLLERS

ETL9410/9310



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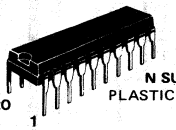
PLASTIC PACKAGE

ETL9411/9311



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PLASTIC PACKAGE

PIN ASSIGNMENT

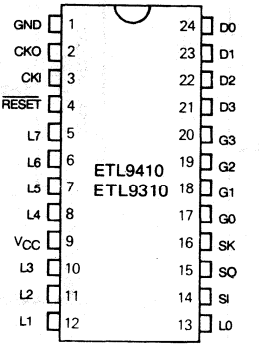

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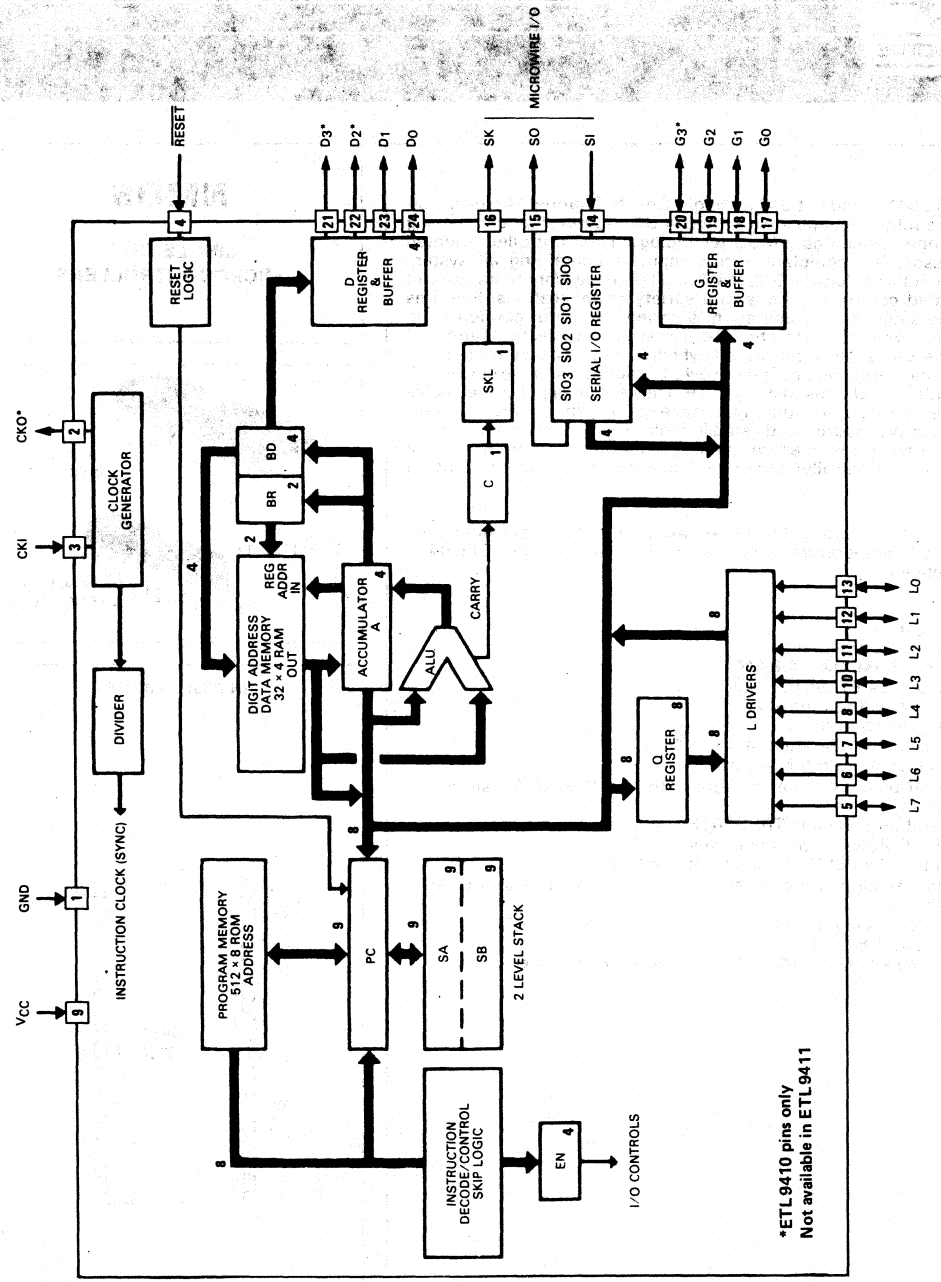
FIGURE 1 – BLOCK DIAGRAM (24-pin version)



ETL9410 • ETL9411

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	
ET L 9410	0.75 Watt at 25°C
	0.4 Watt at 70°C
ET L 9411	0.65 Watt at 25°C
	0.3 Watt at 70°C
Total Source Current	120mA
Total Sink Current	100mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 9.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Standard Operating Voltage (V_{CC})	Note 1	4.5	6.3	V
Optional Operating Voltage (V_{CC})		4.5	9.5	V
Power Supply Ripple	peak to peak	–	0.5	V
Operating Supply Current	all inputs and outputs open	–	6	mA
Input Voltage Levels				
CKI Input Levels				
Ceramic Resonator Input (÷8)				
Logic High (V_{IH})		2.0	–	V
Logic Low (V_{IL})		−0.3	0.4	V
Schmitt Trigger Input (÷4)				
Logic High (V_{IH})		0.7 V_{CC}	–	V
Logic Low (V_{IL})		−0.3	0.6	V
$\overline{\text{RESET}}$ Input Levels	(Schmitt Trigger Input)			
Logic High		0.7 V_{CC}	–	V
Logic Low		−0.3	0.6	V
SO Input Level (Test mode)	Note 2	2.0	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0	–	V
Logic High	with TTL trip level options	2.0	–	V
Logic Low	selected, $V_{CC} = 5V \pm 5\%$	−0.3	0.8	V
Logic High	with high trip level options	3.6	–	V
Logic Low	selected	−0.3	1.2	V
Input Capacitance		–	7	pF
Hi-Z Input Leakage		−1	+1	µA
Output Voltage Levels				
LSTTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High (V_{OH})	$I_{OH} = -25\mu A$	2.7	–	V
Logic Low (V_{OL})	$I_{OL} = 0.36mA$	–	0.4	V
CMOS Operation				
Logic High	$I_{OH} = -10\mu A$	$V_{CC} - 1$	–	V
Logic Low	$I_{OL} = +10\mu A$	–	0.2	V

Note 1 : V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.
Note 2 : SO output "0" level must be less than 0.8V for normal operation.

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DC ELECTRICAL CHARACTERISTICS (continued) $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 9.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	$V_{CC} = 9.5V$, $V_{OL} = 0.4V$	1.8	–	mA
	$V_{CC} = 6.3V$, $V_{OL} = 0.4V$	1.2	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.9	–	mA
L_0-L_7 Outputs, G_0-G_3 and LSTTL D_0-D_3 Outputs (I_{OL})	$V_{CC} = 9.5V$, $V_{OL} = 0.4V$	0.8	–	mA
	$V_{CC} = 6.3V$, $V_{OL} = 0.4V$	0.5	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.4	–	mA
D_0-D_3 Outputs with High Current Options (I_{OL})	$V_{CC} = 9.5V$, $V_{OL} = 1.0V$	15	–	mA
	$V_{CC} = 6.3V$, $V_{OL} = 1.0V$	11	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	7.5	–	mA
D_0-D_3 Outputs with Very High Current Options (I_{OL})	$V_{CC} = 9.5V$, $V_{OL} = 1.0V$	30	–	mA
	$V_{CC} = 6.3V$, $V_{OL} = 1.0V$	22	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	15	–	mA
CKI (Single-pin RC oscillator)	$V_{CC} = 4.5V$, $V_{IH} = 3.5V$	2	–	mA
Output Source Current				
Standard Configuration, All Outputs (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−140	−800	µA
	$V_{CC} = 6.3V$, $V_{OH} = 2.0V$	−75	−480	µA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	−30	−250	µA
Push-Pull Configuration SO and SK Outputs (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 4.75V$	−1.4	–	mA
	$V_{CC} = 6.3V$, $V_{OH} = 2.4V$	−1.4	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.0V$	−1.2	–	mA
LED Configuration, L_0-L_7 Outputs, Low Current Driver Option (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−1.5	−18	mA
	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−1.5	−13	mA
LED Configuration, L_0-L_7 Outputs, High Current Driver Option (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−3.0	−35	mA
	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−3.0	−25	mA
TRI-STATE® Configuration, L_0-L_7 Outputs, Low Current Driver Option (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 5.5V$	−0.75	–	mA
	$V_{CC} = 6.3V$, $V_{OH} = 3.2V$	−0.8	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−0.9	–	mA
TRI-STATE® Configuration, L_0-L_7 Outputs, High Current Driver Option (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 5.5V$	−1.5	–	mA
	$V_{CC} = 6.3V$, $V_{OH} = 3.2V$	−1.6	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−1.8	–	mA
Input Load Source Current	$V_{CC} = 5.0V$, $V_{IL} = 0V$	−10	−140	µA
CKO Output				
RAM Power Supply Option Power Requirement	$V_R = 3.3V$	–	1.5	mA
TRI-STATE® Output Leakage Current		−2.5	+2.5	µA
Total Sink Current Allowed				
All Outputs Combined		–	100	mA
D Port		–	100	mA
L_7-L_4, G Port		–	4	mA
L_3-L_0		–	4	mA
Any Other Pin		–	2.0	mA
Total Source Current Allowed				
All I/O Combined		–	120	mA
L_7-L_4		–	60	mA
L_3-L_0		–	60	mA
Each L Pin		–	25	mA
Any Other Pin		–	1.5	mA

ETL9310 • ETL9311

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	−40°C to +85°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	
ET L 9310	0.75 Watt at 25°C
	0.25 Watt at 85°C
ET L 9311	0.65 Watt at 25°C
	0.20 Watt at 85°C
Total Source Current	120mA
Total Sink Current	100mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS — $-40°C \leq T_A \leq +85°C$, $4.5V \leq V_{CC} \leq 7.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Standard Operating Voltage (V_{CC})	Note 1	4.5	5.5	V
Optional Operating Voltage (V_{CC})		4.5	7.5	V
Power Supply Ripple	peak to peak	–	0.5	V
Operating Supply Current	all inputs and outputs open	–	8	mA
Input Voltage Levels				
Ceramic Resonator Input(÷8) Crystal Input				
Logic High (V_{IH})		2.2	–	V
Logic Low (V_{IL})		−0.3	0.3	V
Schmitt Trigger Input (÷4)				
Logic High (V_{IH})		0.7 V_{CC}	–	V
Logic Low (V_{IL})		−0.3	0.4	V
$\overline{RESET}$ Input Levels	(Schmitt Trigger Input)			
Logic High		0.7 V_{CC}	–	V
Logic Low		−0.3	0.4	V
SO Input Level (Test mode)	Note 2	2.2	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0	–	V
Logic High	with TTL trip level options	2.2	–	V
Logic Low	selected, $V_{CC} = 5V \pm 5\%$	−0.3	0.6	V
Logic High	with high trip level options	3.6	–	V
Logic Low	selected	−0.3	1.2	V
Input Capacitance		–	7	pF
Hi-Z Input Leakage		−2	+2	µA
Output Voltage Levels				
LSTTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High (V_{OH})	$I_{OH} = -20\mu A$	2.7	–	V
Logic Low (V_{OL})	$I_{OL} = 0.36mA$	–	0.4	V
CMOS Operation				
Logic High	$I_{OH} = -10\mu A$	$V_{CC} - 1$	–	V
Logic Low	$I_{OL} = +10\mu A$	–	0.2	V

Note 1 : V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.
Note 2 : SO output "0" level must be less than 0.6V for normal operation.

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DC ELECTRICAL CHARACTERISTICS (continued) $-40°C \leq T_A \leq +85°C$, $4.5V \leq V_{CC} \leq 7.5V$ (Unless otherwise specified)

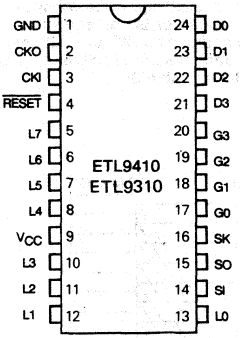
Parameter	Conditions	Min.	Max.	Units
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	$V_{CC} = 7.5V$, $V_{OL} = 0.4V$	1.4	–	mA
	$V_{CC} = 5.5V$, $V_{OL} = 0.4V$	1.0	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.8	–	mA
L_0-L_7 Outputs, G_0-G_3 and LSTTL, D_0-D_3 Outputs (I_{OL})	$V_{CC} = 7.5V$, $V_{OL} = 0.4V$	0.6	–	mA
	$V_{CC} = 5.5V$, $V_{OL} = 0.4V$	0.5	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.4	–	mA
D_0-D_3 Outputs with High Current Options (I_{OL})	$V_{CC} = 7.5V$, $V_{OL} = 1.0V$	12	–	mA
	$V_{CC} = 5.5V$, $V_{OL} = 1.0V$	9	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	7	–	mA
D_0-D_3 Outputs with Very High Current Options (I_{OL})	$V_{CC} = 7.5V$, $V_{OL} = 1.0V$	24	–	mA
	$V_{CC} = 5.5V$, $V_{OL} = 1.0V$	18	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	14	–	mA
CKI (Single-pin RC oscillator)	$V_{CC} = 4.5V$, $V_{IH} = 3.5V$	2	–	mA
Output Source Current				
Standard Configuration, All Outputs (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	−100	−900	µA
	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	−55	−600	µA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	−28	−350	µA
Push-Pull Configuration SO and SK Outputs (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 3.75V$	−0.85	–	mA
	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	−1.1	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.0V$	−1.2	–	mA
LED Configuration, L_0-L_7 Outputs, Low Current Driver Option (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	−1.4	−27	mA
LED Configuration, L_0-L_7 Outputs, High Current Driver Option (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	−2.7	−54	mA
TRI-STATE® Configuration, L_0-L_7 Outputs, Low Current Driver Option (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 4.0V$	−0.7	–	mA
	$V_{CC} = 5.5V$, $V_{OH} = 2.7V$	−0.6	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−0.9	–	mA
TRI-STATE® Configuration, L_0-L_7 Outputs, High Current Driver Option (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 4.0V$	−1.4	–	mA
	$V_{CC} = 5.5V$, $V_{OH} = 2.7V$	−1.2	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−1.8	–	mA
Input Load Source Current	$V_{CC} = 5.0V$, $V_{IL} = 0V$	−10	−200	µA
CKO Output				
RAM Power Supply Option Power Requirement	$V_R = 3.3V$	–	2.0	mA
TRI-STATE® Output Leakage Current		−5	+5	µA
Total Sink Current Allowed				
All Outputs Combined		–	100	mA
D Port		–	100	mA
L_7-L_4, G Port		–	4	mA
L_3-L_0		–	4	mA
Any Other Pin		–	2.0	mA
Total Source Current Allowed				
All I/O Combined		–	120	mA
L_7-L_4		–	60	mA
L_3-L_0		–	60	mA
Each L Pin		–	25	mA
Any Other Pin		–	1.5	mA

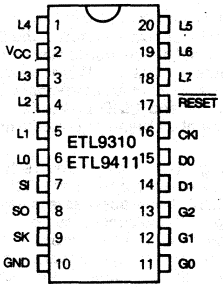
AC ELECTRICAL CHARACTERISTICS

ETL 9410/L 9411 : $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 9.5V$ (Unless otherwise specified)
ETL 9310/L 9311 : $-40°C \leq T_A \leq +85°C$, $4.5V \leq V_{CC} \leq 7.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Instruction Cycle Time — t_C		16	40	μs
CKI				
Input Frequency — f_I	÷8 mode	0.2	0.5	MHz
	÷4 mode	0.1	0.25	MHz
Duty Cycle		30	60	%
Rise Time	$f_I = 0.5$ MHz	–	500	ns
Fall Time		–	200	ns
CKI Using RC (÷4)	$R = 56k\Omega \pm 5\%$ $C = 100pF \pm 10\%$			
Instruction Cycle Time		16	28	μs
CKO as SYNC Input				
t_{SYNC}		400	–	ns
INPUTS:				
G_3-G_0, L_7-L_0				
t_{SETUP}		–	8.0	μs
t_{HOLD}		–	1.3	μs
SI				
t_{SETUP}		–	2.0	μs
t_{HOLD}		–	1.0	μs
OUTPUT PROPAGATION DELAY	Test condition: $C_L = 50pF$, $R_L = 20k\Omega$, $V_{OUT} = 1.5V$			
SO, SK Outputs				
t_{pd1}, t_{pd0}		–	4.0	μs
All Other Outputs				
t_{pd1}, t_{pd0}		–	5.6	μs

FIGURE 2 – CONNECTION DIAGRAMS





Pin	Description
L_7-L_0	8 bidirectional I/O ports with TRI-STATE®
G_3-G_0	4 bidirectional I/O ports (G_2-G_0 for COP411L)
D_3-D_0	4 general purpose outputs (D_1-D_0 for ETL 9411)
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)

Pin	Description
SK	Logic-controlled clock (or general purpose output)
CKI	System oscillator input
CKO	System oscillator output (or RAM power supply or SYNG input) (ETL 9410 only)
$\overline{RESET}$	System reset input
V_{CC}	Power supply
GND	Ground

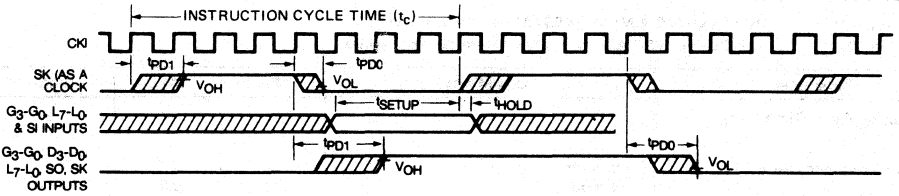


FIGURE 3 – INPUT/OUTPUT TIMING DIAGRAMS (CERAMIC RESONATOR DIVIDE-BY-8 MODE)

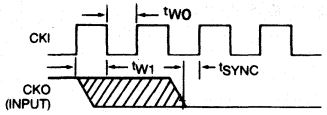


FIGURE 3a – SYNCHRONIZATION TIMING

FUNCTIONAL DESCRIPTION

A block diagram of the ET L 9410 is given in Figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2 volts). When a bit is reset, it is a logic "0" (less than 0.8 volts).

All functional references to the ET L 9410 / L 9411 - also apply to the ET L 9310 / L 9311.

Program Memory

Program Memory consists of a 512-byte ROM. As can be seen by an examination of the ET L 9410 / L 9411 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQID instructions, ROM must often be thought of as being organized into 8 pages of 64 words each.

ROM addressing is accomplished by a 9-bit PC register. Its binary value selects one of the 512 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 9-bit binary count value. Two levels of subroutine nesting are implemented by the 9-bit subroutine save registers, SA and SB, providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the instruction Decode, Control and Skip Logic circuitry.

Data Memory

Data memory consists of a 128-bit RAM, organized as 4 data registers of 8 4-bit digits. RAM addressing is implemented by a 6-bit B register whose upper 2 bits (Br) select 1 of 4 data registers and lower 3 bits of the 4-bit Bd select 1 of 8 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the XAD 3, 15 instruction. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

The most significant bit of Bd is not used to select a RAM digit. Hence each physical digit of RAM may be selected by two different values of Bd as shown in Figure 4 below. The skip condition for XIS and XDS instructions will be true if Bd changes between 0 and 15, but NOT between 7 and 8 (see Table 3).

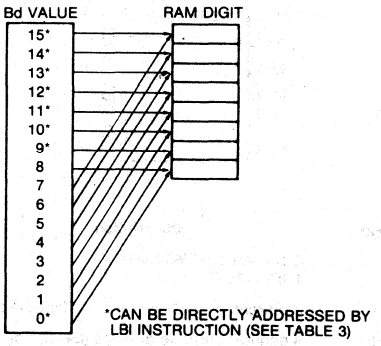


FIGURE 4 – RAM DIGIT ADDRESS TO PHYSICAL RAM DIGIT MAPPING

Internal Logic

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Bd portion of the B register, to load 4 bits of the 8-bit Q latch data, to input 4 bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions of the ET L 9410 / L 9411, storing its results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below).

The G register contents are outputs to 4 general-purpose bidirectional I/O ports.

The Q register is an internal, latched, 8-bit register, used to hold data loaded from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction.)

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa - Sg and decimal point segments of the display.

The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register. (See EN register description, below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/parallel-out shift registers.

The XAS instruction copies C into the SKL Latch. In the counter mode, SK is the output of SKL in the shift register mode, SK outputs SKL ANDed with internal instruction cycle clock.

The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

1. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. (See 4 below.) The SK output becomes a logic-controlled clock.
2. EN_1 is not used. It has no effect on ET L 9410 / L 9411-operation.
3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high-impedance input state.
4. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0." Table I provides a summary of the modes associated with EN_3 and EN_0.

Initialization

The Reset Logic will initialize (clear) the device upon power-up if the power supply rise time is less than 1 ms and greater than 1 µs. If the power supply rise time is greater than 1 ms, the user must provide an external RC

Enable Register Modes – Bits EN_3 and EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = Clock If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = Clock If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

network and diode to the $\overline{\text{RESET}}$ pin as shown below (Figure 5). The $\overline{\text{RESET}}$ pin is configured as a Schmitt trigger input. If not used it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{\text{RESET}}$ input, provided it stays low for at least three instruction cycle times.

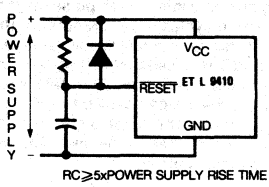
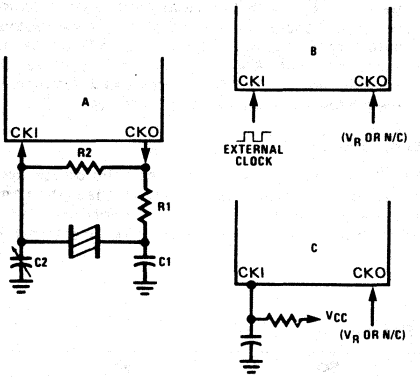


FIGURE 5 – POWER-UP CLEAR CIRCUIT

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. *Data Memory (RAM) is not cleared upon initialization.* The first instruction at address 0 must be a CLRA.



Ceramic Resonator Oscillator

Resonator Value	Component Values			
	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)
455 kHz	1k	1M	80	80

This circuit and these values are for indication only. As the oscillator characteristics are not guaranteed, please consider and examine the circuit constants carefully on your application.

Oscillator

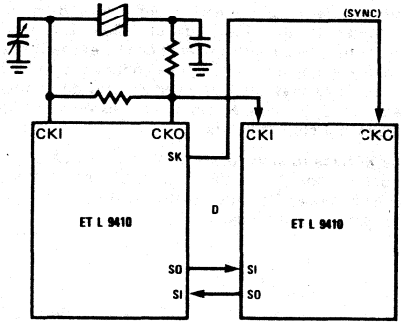
There are four basic clock oscillator configurations available as shown by Figure 6.

a. **Resonator Controlled Oscillator.** CKI and CKO are connected to an external ceramic resonator. The instruction cycle frequency equals the resonator frequency divided by 8. This is not available in the ET L 9411.

b. **External Oscillator.** CKI is an external clock input signal. The external frequency is divided by 8 to give the instruction frequency time. CKO is now available to be used as the RAM power supply (V_R), as a SYNC input, or no connection. (Note: No CKO on ET L 9411.

c. **RC Controlled Oscillator.** CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available as the RAM power supply (V_R) or no connection.

d. **Externally Synchronized Oscillator.** Intended for use in multi-COP systems, CKO is programmed to function as an input connected to the SK output of another chip operating at the same frequency (chip with L or C suffix) with CKI connected as shown. In this configuration, the SK output connected to CKO must provide a SYNC (instruction cycle) signal to CKO, thereby allowing synchronous data transfer between the chips using only the SI and SO serial I/O pins in conjunction with the XAS instruction. Note that on power-up SK is automatically enabled as a SYNC output. (See Functional Description, Initialization, above). This is not available in the ETL 9411.



RC Controlled Oscillator

R (kΩ)	C (pF)	Instruction Cycle Time in μs)
51	100	19 ± 15%
82	56	19 ± 13%

Note: 200kΩ ≥ R ≥ 25kΩ
360pF ≥ C ≥ 50pF

FIGURE 6 – ETL9410 / L 9411 - OSCILLATOR

CKO Pin Options

In a resonator controlled oscillator system, CKO is used as an output to the resonator network. As an option CKO can be a SYNC input as described above. As another option, CKO can be a RAM power supply pin (V_R), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using no connection option is appropriate in applications where the ET L 9410 system timing configuration does not require use of the CKO pin.

RAM Keep-Alive Option

Selecting CKO as the RAM power supply (V_R) allows the user to shut off the chip power supply (V_{CC}) and maintain data in the RAM. To insure that RAM data integrity is maintained, the following conditions must be met:

1. $\overline{\text{RESET}}$ must go low before V_{CC} goes below spec during power-off; V_{CC} must be within spec before $\overline{\text{RESET}}$ goes high on power-up.
2. During normal operation, V_R must be within the operating range of the chip with $(V_{CC} - 1) \leq V_R \leq V_{CC}$.
3. V_R must be $\geq$ 3.3V with V_{CC} off.

I/O Options

ET L 9410 / L 9411 inputs and outputs have the following optional configurations, illustrated in Figure 7.

a. **Standard** — an enhancement-mode device to ground in conjunction with a depletion-mode device to V_{CC}, compatible with LSTTL and CMOS input requirements. Available on SO, SK, and all D and G outputs.

b. **Open-Drain** — an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, and all D and G outputs.

c. **Push-Pull** — an enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.

d. **Standard L** — same as a., but may be disabled. Available on L outputs only.

e. **Open Drain L** — same as b., but may be disabled. Available on L outputs only.

f. **LED Direct Drive** — an enhancement mode device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (see Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display. Available on L outputs only.

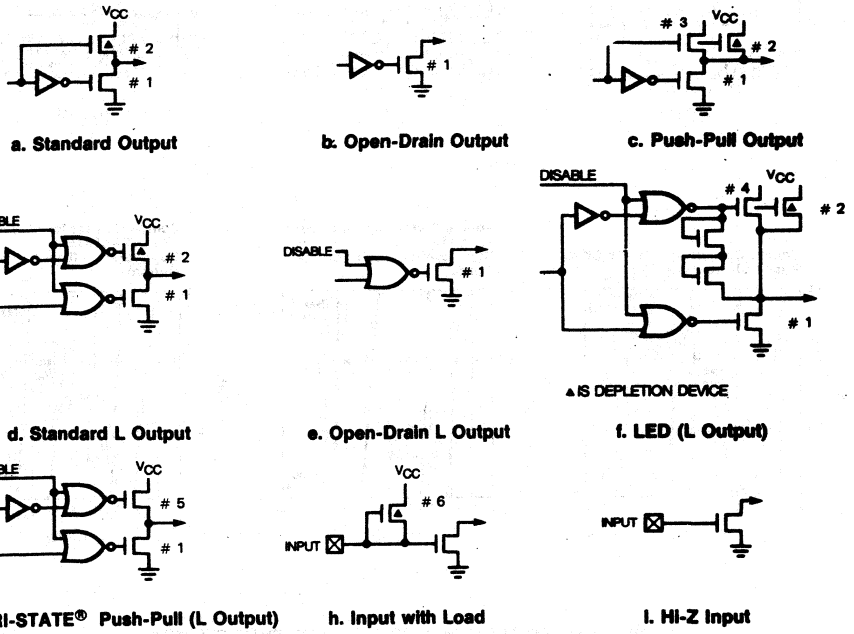


FIGURE 7 – INPUT AND OUTPUT CONFIGURATIONS

g. TRI-STATE® Push-Pull — an enhancement-mode device to ground and V_{CC}. These outputs are TRI-STATE® outputs, allowing for connection of these outputs to a data bus shared by other bus drivers. Available on L outputs only.

h. An on-chip depletion load device to V_{CC}.

i. A Hi-Z input which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in Figure 8 for each of these devices to allow the designer to effectively use these I/O configurations in designing a ETL 9410 / L 9411 system.

The SO, SK outputs can be configured as shown in **a.**, **b.**, or **c.** The D and G outputs can be configured as shown in **a.** or **b.** Note that when inputting data to the G ports, the G outputs should be set to "1." The L outputs can be configured as in **d.**, **e.**, **f.**, or **g.**

An important point to remember if using configuration **d.** or **f.** with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current. (See Figure 8, device 2.) However, when the L port is used as input, the disabled depletion device CANNOT be relied on to source sufficient current to pull an input to a logic "1"

ET L 9411

If the ET L 9410 is bonded as a 20-pin device, it becomes the ET L 9411, illustrated in Figure 2. ET L 9410 / ET L 9411 Connection Diagrams. Note that the ET L 9411 does not contain D2, D3, G3, or CKO. Use of this option of course precludes use of D2, D3, G3, and CKO options. All other options are available for the ET L 9411.

TYPICAL PERFORMANCE CURVES

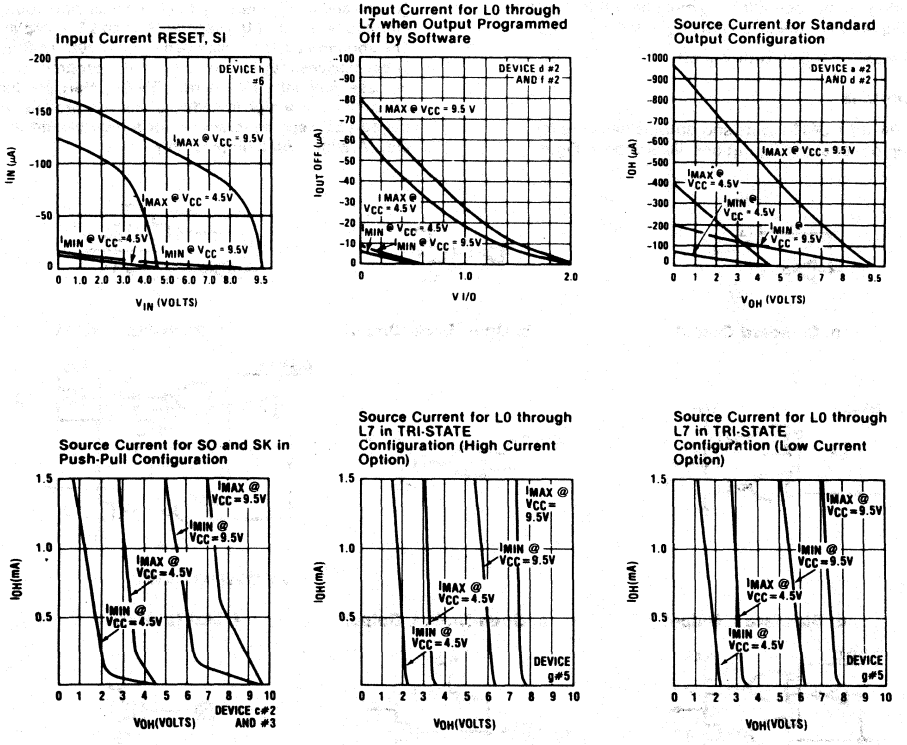
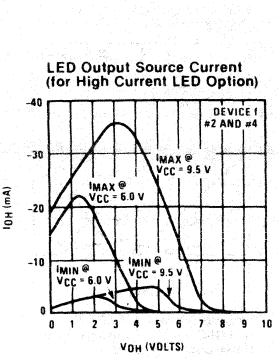
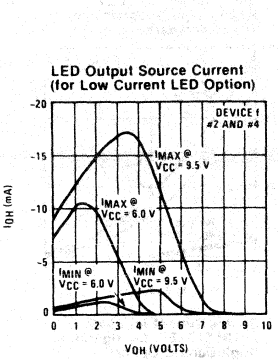
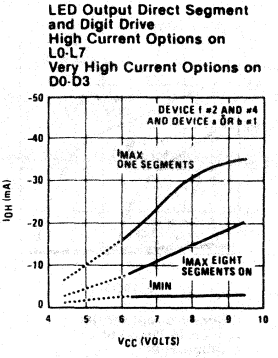
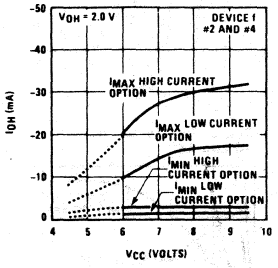


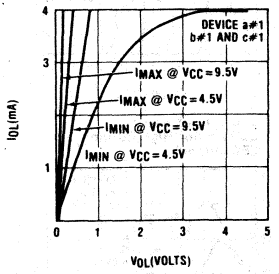
FIGURE 8a – ETL9410 / L 9411 - I/O DC CURRENT CHARACTERISTICS

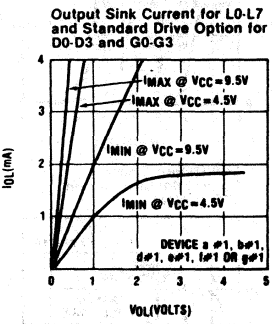


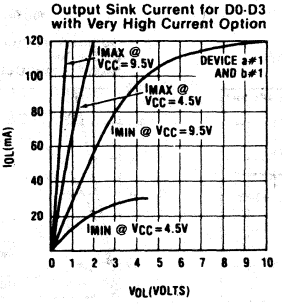












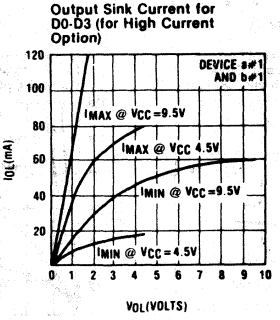
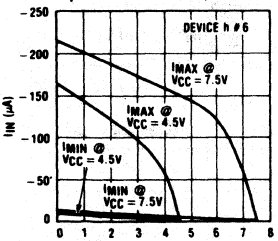
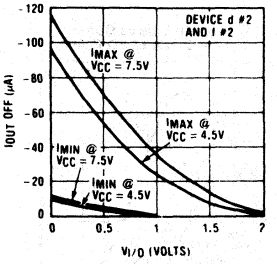


FIGURE 8a – ETL9410 / L 9411 - I/O DC CURRENT CHARACTERISTICS

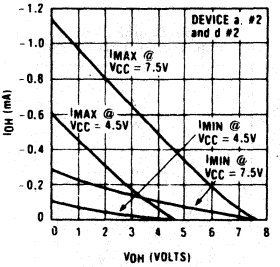
Input Current $\overline{RESET}$, SI



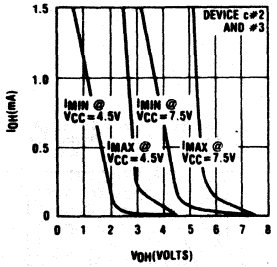
Input Current for L0-L7 when Output Programmed Off by Software



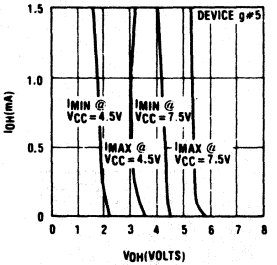
Source Current for Standard Output Configuration



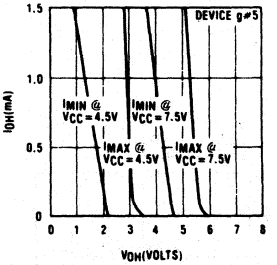
Source Current for SO and SK in Push-Pull Configuration



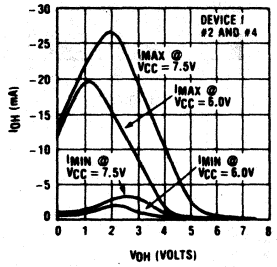
Source Current for L0-L7 in TRI-STATE Configuration (High Current Option)



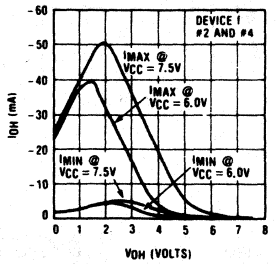
Source Current for L0-L7 in TRI-STATE Configuration (Low Current Option)



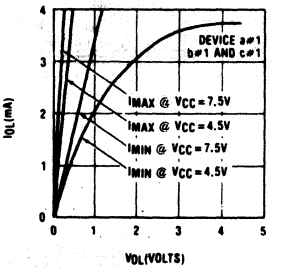
LED Output Source Current (for Low Current LED Option)



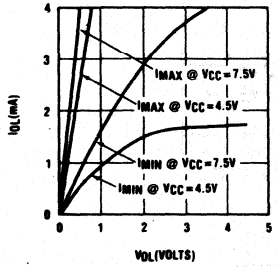
LED Output Source Current (for High Current LED Option)



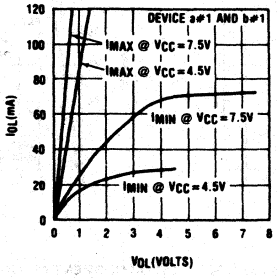
Output Sink Current for SO and SK



Output Sink Current for L0-L7 and Standard Drive Option for D0-D3 and G0-G3



Output Sink Current for D0-D3 with Very High Current Option



Output Sink Current for D0-D3 (for High Current Option)

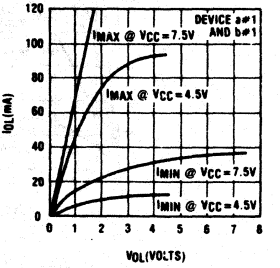


FIGURE 8b – ETL9310 / L9311 - INPUT/OUTPUT CHARACTERISTICS

ETL 9410/L 9411 - INSTRUCTION SET

Table 2 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 3 provides the mnemonic, operand, machine, code, data flow, skip conditions and description associated with each instruction in the ET L 9410 / L 9411- instruction set.

TABLE 2 – ETL9410 / L9411 - INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition
INTERNAL	ARCHITECTURE SYMBOLS
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
L	8-bit TRI-STATE I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
PC	9-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	9-bit Subroutine Save Register A
SB	9-bit Subroutine Save Register B
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0 - 15 binary (RAM Digit Select)
r	2-bit Operand Field, 0 - 3 binary (RAM Register Select)
a	9-bit Operand Field, 0 - 511 binary (ROM Address)
y	4-bit Operand Field 0 - 15 binary (Immediate Data)
$RAM_{(s)}$	Contents of RAM location addressed by s
$ROM_{(t)}$	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
–	Minus
→	Replaces
↔	Is exchanged with
=	Is equal to
$\bar{A}$	The one's complement of A
⊕	Exclusive-OR
:	Range of values

TABLE 3 – ETL9410 / L9411 - INSTRUCTION SET

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011|0000	A + C + RAM(B) → A Carry → C	Carry	Add with Carry. Skip on Carry
ADD		31	0011|0001	A + RAM(B) → A	None	Add RAM to A
AISC	y	5-	0101| y	A + y → A	Carry	Add Immediate. Skip on Carry (y ≠ 0)
CLRA		00	0000|0000	0 → A	None	Clear A
COMP		40	0100|0000	$\bar{A}$ → A	None	One's complement of A to A
NOP		44	0100|0100	None	None	No Operation
RC		32	0011|0010	"0" → C	None	Reset C
SC		22	0010|0010	"1" → C	None	Set C
XOR		02	0000|0010	A⊕RAM(B) → A	None	Exclusive-OR RAM with A

TABLE 3 – ETL9410 / L9411 - INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1111|1111	ROM (PC_8,A,M) → $PC_{7:0}$	None	Jump Indirect (Note 2)
JMP	a	6- --	0110|000|a_8 $a_{7:0}$	a → PC	None	Jump
JP	a	--	1| $a_{6:0}$ (pages 2,3 only) or	a → $PC_{6:0}$	None	Jump within Page (Note 3)
		--	11| $a_{5:0}$ (all other pages)	a → $PC_{5:0}$		
JSRP	a	--	10| $a_{5:0}$	PC + 1 → SA → SB 010 → $PC_{8:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 4)
JSR	a	6- --	0110|100|a_8 $a_{7:0}$	PC + 1 → SA → SB a → PC	None	Jump to Subroutine
RET		48	0100|1000	SB → SA → PC	None	Return from Subroutine
RETSK		49	0100|1001	SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33 3C	0011|0011 0011|1100	A → $Q_{7:4}$ RAM(B) → $Q_{3:0}$	None	Copy A, RAM to Q
LD	r	-5	00|r|0101	RAM(B) → A Br⊕r → Br	None	Load RAM into A, Exclusive-OR Br with r
LQID		BF	1011|1111	ROM(PC_8,A,M) → Q SA → SB	None	Load Q Indirect (Note 2)
RMB	0 1 2 3	4C 45 42 43	0100|1100 0100|0101 0100|0010 0100|0011	0 → $RAM(B)_0$ 0 → $RAM(B)_1$ 0 → $RAM(B)_2$ 0 → $RAM(B)_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	0100|1101 0100|0111 0100|0110 0100|1011	1 → $RAM(B)_0$ 1 → $RAM(B)_1$ 1 → $RAM(B)_2$ 1 → $RAM(B)_3$	None	Set RAM Bit
STII	y	7-	0111| y	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	-6	00|r|0110	RAM(B) ⟷ A Br⊕r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	3,15	23 BF	0010|0011 1011|1111	RAM(3,15) ⟷ A	None	Exchange A with RAM (3,15)
XDS	r	-7	00|r|0111	RAM(B) ⟷ A Bd − 1 → Bd Br⊕r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	-4	00|r|0100	RAM(B) ⟷ A Bd + 1 → Bd Br⊕r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r

TABLE 3 – ETL9410 / L9411 - INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0 1 0 1 | 0 0 0 0	A → Bd	None	Copy A to Bd
CBA		4E	0 1 0 0 | 1 1 1 0	Bd → A	None	Copy Bd to A
LBI	r,d	--	0 0 | r | (d - 1) | (d = 0, 9:15)	r,d → B	Skip until not a LBI	Load B Immediate with r,d (Note 5)
LEI	y	33 6-	0 0 1 1 | 0 0 1 1 0 1 1 0 | y	y → EN	None	Load EN Immediate (Note 6)
TEST INSTRUCTIONS						
SKC		20	0 0 1 0 | 0 0 0 0		C = "1"	Skip if C is True
SKE		21	0 0 1 0 | 0 0 0 1		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0 0 1 1 | 0 0 1 1 0 0 1 0 | 0 0 0 1		$G_{3:0} = 0$	Skip if G is Zero (all 4 bits)
SKGBZ		33	0 0 1 1 | 0 0 1 1	1st byte		Skip if G Bit is Zero
	0	01	0 0 0 0 | 0 0 0 1	2nd byte	$G_0 = 0$	
	1	11	0 0 0 1 | 0 0 0 1	2nd byte	$G_1 = 0$	
	2	03	0 0 0 0 | 0 0 1 1	2nd byte	$G_2 = 0$	
	3	13	0 0 0 1 | 0 0 1 1	2nd byte	$G_3 = 0$	
SKMBZ	0	01	0 0 0 0 | 0 0 0 1		$RAM(B)_0 = 0$	Skip if RAM Bit is Zero
	1	11	0 0 0 1 | 0 0 0 1		$RAM(B)_1 = 0$	
	2	03	0 0 0 0 | 0 0 1 1		$RAM(B)_2 = 0$	
	3	13	0 0 0 1 | 0 0 1 1		$RAM(B)_3 = 0$	
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	0 0 1 1 | 0 0 1 1 0 0 1 0 | 1 0 1 0	G → A	None	Input G Ports to A
INL		33 2E	0 0 1 1 | 0 0 1 1 0 0 1 0 | 1 1 1 0	$L_{7:4}$ → RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM, A
OBD		33 3E	0 0 1 1 | 0 0 1 1 0 0 1 1 | 1 1 1 0	Bd → D	None	Output Bd to D Outputs
OMG		33 3A	0 0 1 1 | 0 0 1 1 0 0 1 1 | 1 0 1 0	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0 1 0 0 | 1 1 1 1	A ⟷ SIO, C → SKL	None	Exchange A with SIO (Note 2)

Note 1 : All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2 : For additional information on the operation of the XAS, JID, and LQID instructions, see below.

Note 3 : The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 4 : A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 5 : The machine code for the lower 4 bits of the LBI instruction equals the binary value of the "d" data *minus 1*, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 6 : Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register).

The following information is provided to assist the user in uderstanding the operation of several unique instructions and to provide notes useful to programmers in writing ET L 9410 / L 9411.

XAS Instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register, above.) If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM addressed by the 9-bit word, PC_8, A, M. PC_8 is not affected by this instruction.

Note that JID requires 2 instruction cycles to execute.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 9-bit word PC_8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB) and replaces the least significant 8 bits of PC as follows: A → $PC_{7:4}$, RAM(B) → $PC_{3:0}$, leaving PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SA → SB, the previous contents of SB are lost. Also, when LQID pops the stack, the previously pushed contents of SA are left in SB. The net result is that the contents of SA are placed in SB (SA → SB). Note that LQID takes two instruction cycle times to execute.

Instruction Set Notes

a. The firs word of a ET L 9410 / ET L 9411 program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths except JID and LQID take the same number of cycle times whether instructions are skipped or executed. JID and LQID instructions take 2 cycles if executed and 1 cycle if skipped.

c. The ROM is organized into 8 pages of 64 words each. The Program Counter is a 9-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3 or 7 will access data in the next group of 4 pages.

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OPTION LIST

The ET L 9410 / ET L 9411 - mask programmable options are assigned numbers which correspond with the ET L 9410 pins.

The following is a list of ET L 9410 options. When specifying a ET L 9411 chip, Option 2 must be set to 3, Options 20, 21, and 22 to 0. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Output (no option available for ET L 9411)
- = 0: Clock output to ceramic resonator
- = 1: Pin is RAM power supply (V_R) input
- = 2: Multi-COP SYNC input
- = 3: No connection

Option 3: CKI Input
- = 0: Oscillator input divided by 8 (500 kHz max.)
- = 1: Single-pin RC controlled oscillator divided by 4
- = 2: External Schmitt trigger level clock divided by 4

Option 4: $\overline{\text{RESET}}$ Input
- = 0: Load device to V_{CC}
- = 1: Hi-Z input

Option 5: L_7 Driver
- = 0: Standard output
- = 1: Open-drain output
- = 2: High current LED direct segment drive output
- = 3: High current TRI-STATE® push-pull output
- = 4: Low-current LED direct segment drive output
- = 5: Low-current TRI-STATE® push-pull output

Option 6: L_6 Driver
same as Option 5

Option 7: L_5 Driver
same as Option 5

Option 8: L_4 Driver
same as Option 5

Option 9: V_{CC} Pin
- = 0: 4.5V to 6.3V operation
- = 1: 4.5V to 9.5V operation

Option 10: L_3 Driver
same as Option 5

Option 11: L_2 Driver
same as Option 5

Option 12: L_1 Driver
same as Option 5

Option 13: L_0 Driver
same as Option 5

Option 14: SI Input
- = 0: load device to V_{CC}
- = 1: HI-Z input

Option 15: SO Driver
- = 0: Standard Output
- = 1: Open-drain output
- = 2: Push-pull output

Option 16: SK Driver
same as Option 15

Option 17: G_0 I/O Port
- = 0: Standard output
- = 1: Open-drain output

Option 18: G_1 I/O Port
same as Option 17

Option 19: G_2 I/O Port
same as Option 17

Option 20: G_3 I/O Port (no option available for ET L 9411)
same as Option 17

Option 21: D_3 Output (no option available for ET L 9411)
- = 0: Very-high sink current standard output
- = 1: Very-high sink current open-drain output
- = 2: High sink current standard output
- = 3: High sink current open-drain output
- = 4: Standard LSTTL output (fanout = 1)
- = 5: Open-drain LSTTL output (fanout = 1)

Option 22: D_2 Output (no option available for ET L 9411)
same as Option 21

Option 23: D_1 Output
same as Option 21

Option 24: D_0 Output
same as Option 21

Option 25: L Input Levels
- = 0: Standard TTL input levels ("0" = 0.8V, "1" = 2.0V)
- = 1: Higher voltage input levels ("0" = 1.2V, "1" = 3.6V)

Option 26: G Input Levels
same as Option 25

Option 27: SI Input Levels
same as Option 25

Option 28 : Bonding
- = 0: ET L 9410 (24-pin device)
- = 1: ET L 9411 (20-pin device)
- = 2: Both 24- and 20-pin versions

Test Mode (Non-Standard Operation)

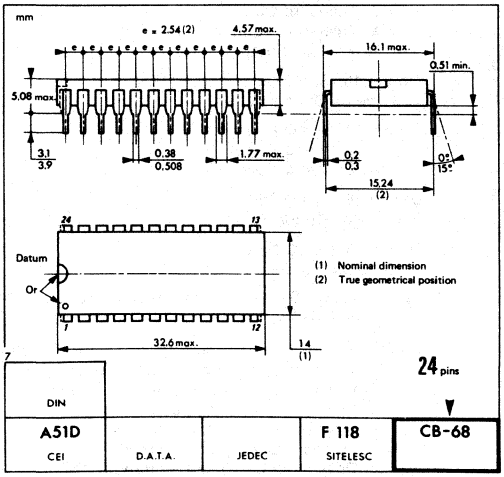
The SO output has been configured to provide for standard test procedures for the custom-programmed ET L 9410. With SO forced to logic "1", two test modes are provided, depending upon the value of SI:

a. RAM and Internal Logic Test Mode (SI = 1)

b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user; they are intended for manufacturing test only.

PHYSICAL DIMENSIONS



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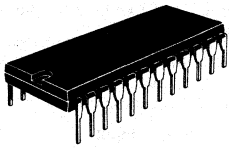
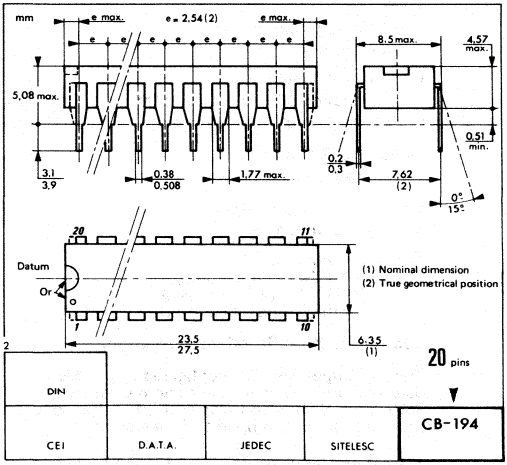


N SUFFIX
PLASTIC PACKAGE



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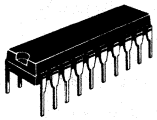

N SUFFIX
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ETL9413 • ETL9313

SINGLE CHIP MICROCONTROLLERS

The ETL9413 and ETL9313 Single-Chip N-Channel Microcontrollers are fully compatible with the COPS ® family, fabricated using N-channel, silicon gate MOS technology. The Controller Oriented Processors are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end-product cost.

The ETL9413 is identical to the ETL9410, but with 15 I/O lines instead of 19.

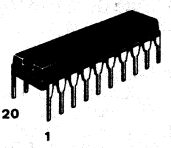
The ETL9313 is exact functional equivalent but extended temperature version of ETL9413.

- Low cost
- Powerful instruction set
- Ceramic or crystal oscillator input/output
- 512 × 8 ROM. 32 × 4 RAM
- Two-level subroutine stack
- 16μs instruction time
- Single supply operation (4.5 - 6.3V)
- Low current drain (6mA max.)
- Internal binary counter register with serial I/O capability
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS compatible in and out
- Direct drive of LED digit and segment lines
- Software/hardware compatible with other members of ETL9313 family
- Extended temperature range device ETL9310 ETL9311 (-40° C to + 85° C)
- Wider supply range (4.5 - 9.5V) optionally available

NMOS

SINGLE CHIP MICROCONTROLLERS

ETL9413 / ETL9313



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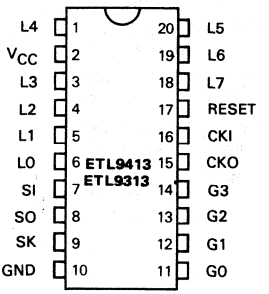
PIN ASSIGNMENT



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OPTION LIST

The ETL9413/ETL9313 - mask programmable options are assigned numbers which correspond with the ETL9410 pins.

The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Output
= 0: Clock output to ceramic resonator
= 1: Pin is RAM power supply (V_R) input
= 2: Multi-COP SYNC input
= 3: No connection

Option 3: CKI Input
= 0: Oscillator input divided by 8 (500 kHz max.)
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same as Option 5

Option 7: L_5 Driver
same as Option 5

Option 8: L_4 Driver
same as Option 5

Option 9: V_{CC} Pin
= 0: 4.5 V to 6.3 V operation
= 1: 4.5 V to 9.5 V operation

Option 10: L_3 Driver
same as Option 5

Option 11: L_2 Driver
same as Option 5

Option 12: L_1 Driver
same as Option 5

Option 13: L_0 Driver
same as Option 5

Option 14: SI Input
= 0: load device to V_{CC}
= 1: HI-Z input

Option 15: SO Driver
= 0: Standard Output
= 1: Open-drain output
= 2: Push-pull output

Option 16: SK Driver
same as Option 15

Option 17: G_0 I/O Port
= 0: Standard output
= 1: Open-drain output

Option 18: G_1 I/O Port
same as Option 17

Option 19: G_2 I/O Port
same as Option 17

Option 20: G_3 I/O Port
same as Option 17

Option 21: must be set to zero

Option 22: same as Option 21

Option 23: same as Option 21

Option 24: same as Option 21

Option 25: L Input Levels
= 0: Standard TTL input levels ("0" = 0.8 V, "1" = 2.0 V)
= 1: Higher voltage input levels ("0" = 1.2 V, "1" = 3.6 V)

Option 26: G Input Levels
same as Option 25

Option 27: SI Input Levels
same as Option 25

Option 28: Bonding, must be set to 3 for ETL9413/-9313

Test Mode (Non-standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed ETL9413. With SO forced to logic "1", two test modes are provided, depending upon the value of SI:

a. RAM and Internal Logic Test Mode (SI = 1)
b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user; they are intended for manufacturing test only.

The ETL9413 is the same chip as the ETL9410 but in a 20-pin package. The four D ports are not bonded.

Consequently, the electrical characteristics, the functional description and the instruction set are identical to the ETL9410 but without the D outputs. Please, refer to the ETL9410/9411 data sheet.

Note that the OBD instruction can be used but the D outputs are not available.

NOTES

Printed in France

ET9420/21/22 • ET9320/21/22

SINGLE SHIP MICROCONTROLLERS

The ET9420/9421/9422, ET9320/9321 and 9322 Single-Chip N-Channel Microcontrollers are fully compatible with the COPS ® family, fabricated using N-channel, silicon gate XMOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The ET9421 is identical to the ET9420, except with 19 I/O lines instead of 23 ; the ET9422 has 15 I/O lines. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end-product cost.

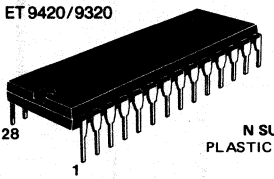
The ET9320 is the extended temperature range version of the ET9420 (likewise the ET9321 and ET9322 are the extended temperature range versions of the ET9421/ET9422). The ET9320/9321/9322 are exact functional equivalents of the ET9420/9421/9422.

- Low cost
- Powerful instruction set
- 1 K x 8 ROM, 64 x 4 RAM
- 23 I/O lines (ET9420, ET9320)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 4.0 μs instruction time
- Single supply operation
- Internal time-base counter for real-time processing
- Internal binary counter register with MICROWIRE® compatible serial I/O capability
- General purpose and TRI-STATE®outputs
- TTL/CMOS compatible in and out
- LED direct drive outputs
- MICROBUS ® compatible
- Software/hardware compatible with other members of ET9400
- Extended temperature range device ET9320/9321/9322 (-40° C to + 85° C)

NMOS

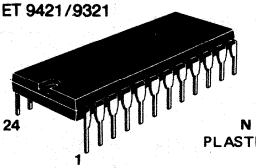
SINGLE-CHIP MICROCONTROLLERS

ET 9420/9320



N SUFFIX
PLASTIC PACKAGE

ET 9421/9321



N SUFFIX
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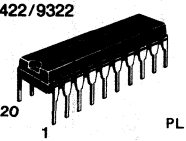
ET 9422/9322



N SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT

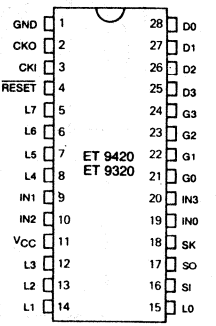


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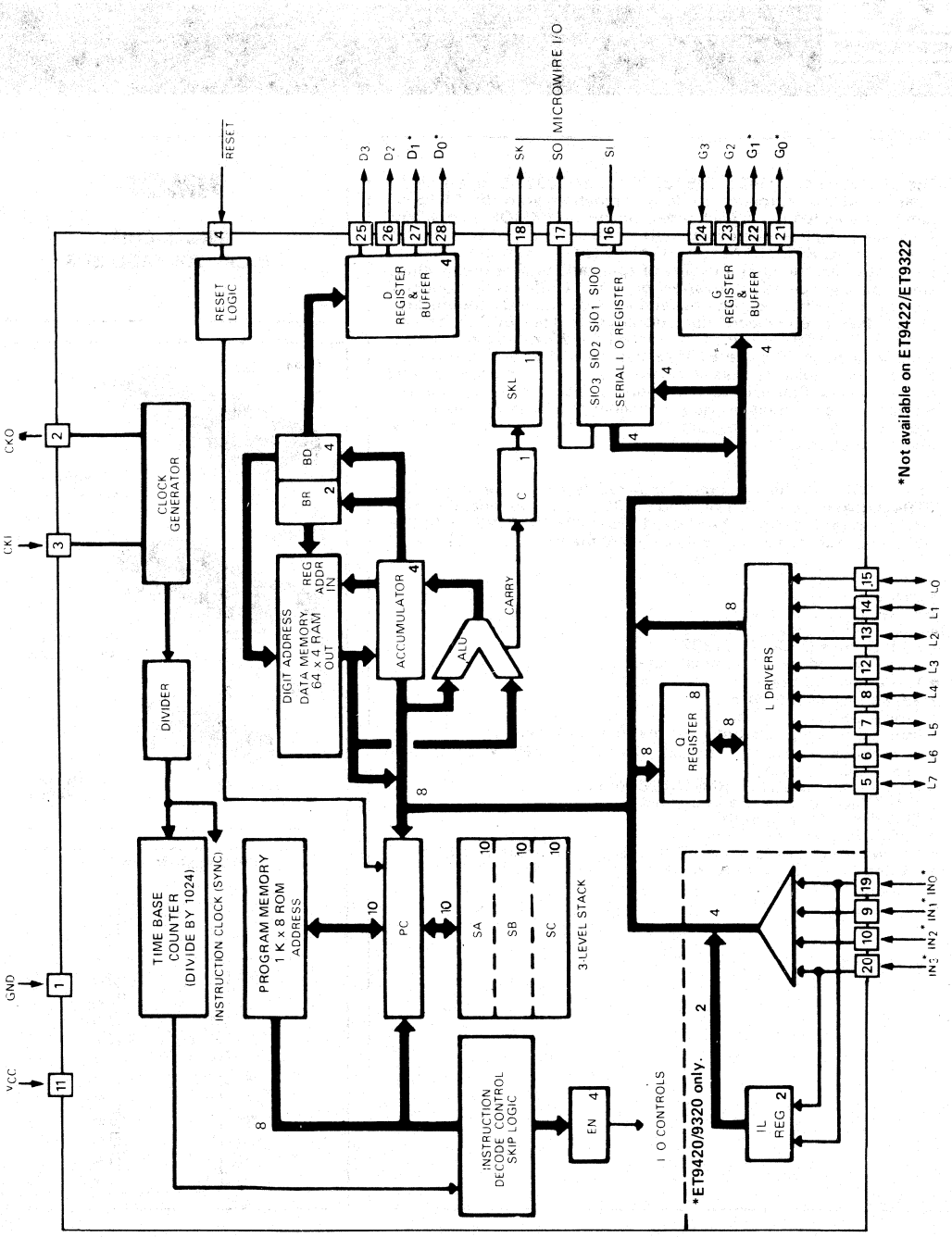
FIGURE 1 – BLOCK DIAGRAM (28-pin version)



ET9420/9421/9422 and ET9320/9321/9322

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin	−0.3V to +7V	Package Power Dissipation	750 mW at 25°C
Operating Temperature Range		24 and 28 pin	400 mW at 70°C
ET9420/9421/9422	0°C to 70°C		250 mW at 85°C
ET9320/9321/9322	−40°C to +85°C	Package Power Dissipation	650 mW at 25°C
Storage Temperature Range	−65°C to +150°C	20 pin	300 mW at 70°C
Total Sink Current	75 mA		200 mW at 85°C
Total Source Current	95 mA	Lead Temperature (soldering, 10 sec.)	300°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

ET9420/9421/9422

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C, 4.5C \leq V_{CC} \leq 6.3V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Operation Voltage		4.5	6.3	V
Power Supply Ripple	Peak to Peak (Note 3)	–	0.4	V
Supply Current	Outputs Open	–	38	mA
Supply Current	Outputs Open, $V_{CC} = 5V$, $T_A = 25°C$	–	30	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High	V_{CC} = Max.	3.0	–	
Logic High	$V_{CC} = 5V \pm 5\%$	2.0	–	V
Logic Low		−0.3	0.4	V
TTL Input	$V_{CC} = 5V \pm 5\%$			
Logic High		2.0	–	V
Logic Low		−0.3	0.8	V
Schmitt Trigger Inputs				
RESET, CKI (÷4)				
Logic High		0.7 V_{CC}	–	V
Logic Low		−0.3	0.6	V
SO Input Level (Test Mode)		2.0	3.0	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0	–	V
Logic High	$V_{CC} = 5V \pm 5\%$	2.0	–	V
Logic Low		−0.3	0.8	V
Input Levels High Trip Option				
Logic High		3.6	–	V
Logic Low		−0.3	1.2	V
Input Load Source Current	$V_{CC} = 5V$, $V_{IN} = 0V$			
CKO		−4	−800	µA
All Others		−100	−800	µA
Input Capacitance		–	7	pF
Hi-Z Input Leakage	$V_{CC} = 5V$	−1	+1	µA
Output Voltage levels				
Standard Outputs				
TTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High	$I_{OH} = -100\mu A$	2.4	–	V
Logic Low	$I_{OL} = 1.6mA$	−0.3	0.4	V
CMOS Operation				
Logic High	$I_{OH} = -10\mu A$	$V_{CC} - 1$	–	V

ET9420/9421/9422

DC ELECTRICAL CHARACTERISTICS (Cont'd) $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 6.3V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Output Current Levels				
LED Direct Drive Output Logic High	$V_{CC} = 6V$, $V_{OH} = 2.0V$	2.5	14	mA
CKI Sink Current (R/C Option)	$V_{IN} = 3.5V$	2	–	mA
CKO (RAM Supply Current)	$V_R = 3.3V$	–	3	mA
TRI-STATE®or Open Drain Leakage Current	$V_{CC} = 5V$	−2.5	+2.5	µA
Output Current Levels				
Output Sink Current (I_{OL})	$V_{CC} = 6.3V$, $V_{OL} = 0.4V$	−2.0	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	−1.0	–	mA
Output Source Current (I_{OH})				
Standard Configuration				
All Outputs	$V_{CC} = 6.3V$, $V_{OH} = 3.0V$	−200	−900	µA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	−100	−500	µA
Push-Pull Configuration				
SO, SK Outputs	$V_{CC} = 6.3V$, $V_{OH} = 3.0V$	−1.0	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	−0.4	–	mA
TRI-STATE Configuration				
L_0-L_7 Outputs	$V_{CC} = 6.3V$, $V_{OH} = 3.0V$	−2.0	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	−0.8	–	mA
LED Configuration				
L_0-L_7 Outputs	$V_{CC} = 6.3V$, $V_{OH} = 3.0V$	−1.0	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	−0.5	–	mA
Allowable Sink Current				
Per Pin (L, D, G)		–	10	mA
Per Pin (All Others)		–	2	mA
Per Port (L)		–	16	mA
Per Port (D, G)		–	10	mA
Allowable Source Current				
Per Pin (L)		–	−15	mA
Per Pin (All Others)		–	−1.5	mA

ET9320/9321/9322

DC ELECTRICAL CHARACTERISTICS – $40° \leq T_A \leq +85°C$, $4.5V \leq V_{CC} \leq 5.5V$ (Unless otherwise specified).

Parameter	Conditions	Min.	Max.	Units
Operation Voltage		4.5	5.5	V
Power Supply Ripple	Peak to Peak (Note 3)	–	0.4	V
Supply Current	$T_A = -40°C$, Outputs Open	–	40	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High		2.2	–	V
Logic Low		−0.3	0.3	V
TTL Input	$V_{CC} = 5V \pm 5\%$			
Logic High		2.2	–	V
Logic Low		−0.3	0.6	V
Schmitt Trigger Inputs				
RESET, CKI (÷4)				
Logic High		$0.7 V_{CC}$	–	V
Logic Low		−0.3	0.4	V
SO Input Level (Test Mode)		2.0	3.0	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0	–	V
Logic High	$V_{CC} = 5V \pm 5\%$	2.2	–	V
Logic Low		−0.3	0.6	V
Input Levels High Trip Option				
Logic High		3.6	–	V
Logic Low		−0.3	1.2	V
Input Load Source Current	$V_{CC} = 5V$, $V_{IN} = 0V$			
CKO		−4	−800	μA
All Others		−100	−800	μA
Input Capacitance		–	7	pF
Hi-Z Input Leakage	$V_{CC} = 5V$	−2	+2	μA
Output Voltage levels				
Standard Outputs				
TTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High	$I_{OH} = -75\mu A$	2.4	–	V
Logic Low	$I_{OL} = 1.6mA$	−0.3	0.4	V
CMOS Operation				
Logic High	$I_{OH} = -10\mu A$	$V_{CC} - 1$	–	V
Logic Low	$I_{OL} = 10\mu A$	−0.3	0.2	V
Output Current Levels				
LED Direct Drive Output	$V_{CC} = 5V$ (Note 4)			
Logic High	$V_{OH} = 2.0V$	1.0	12	mA
CKI Sink Current (R/C Option)	$V_{IN} = 3.5V$	2	–	mA
CKO (RAM Supply Current)	$V_R = 3.3V$	–	4	mA
TRI-STATE® or Open Drain Leakage Current	$V_{CC} = 5V$	−5	+5	μA
Allowable Sink Current				
Per Pin (L, D, G)		–	10	mA
Per Pin (All Others)		–	2	mA
Per Port (L)		–	16	mA
Per Port (D, G)		–	10	mA
Allowable Source Current				
Per Pin (L)		–	−15	mA
Per Pin (All Others)		–	−1.5	mA

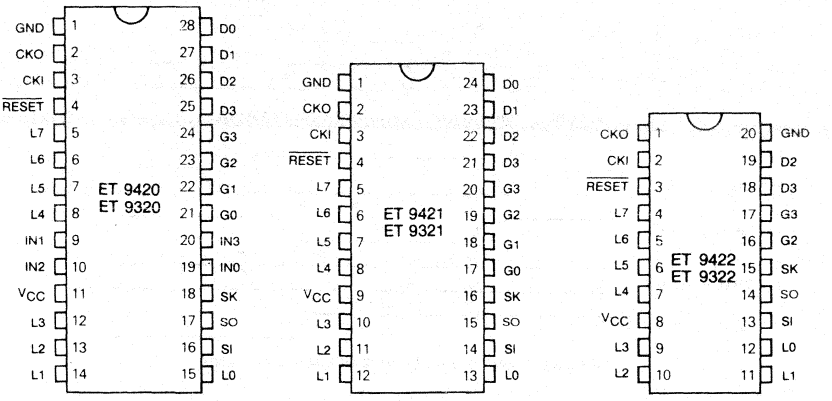
AC ELECTRICAL CHARACTERISTICS

ET9420/9421/9422 $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 6.3V$ (Unless otherwise specified)
ET9320/9321/9322 $-40°C \leq T_A \leq +85°C$, $4.5V \leq V_{CC} \leq 5.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Instruction Cycle Time		4	10	µs
Operating CKI Frequency	÷16 mode	1.6	4.0	MHz
	÷8 mode	0.8	2.0	MHz
CKI Duty Cycle (Note 1)		40	60	%
Rise Time	Freq. = 4 MHz	–	60	ns
Fall Time	Freq. = 4 MHz	–	40	ns
CKI Using RC (Figure 8c)	÷4 mode			
Frequency	R = 15 kΩ ± 5%, C = 100 pF ± 10%	0.5	1.0	MHz
Instruction Cycle Time		4	8	µs
CKO as SYNC input (Figure 8d)				
t_{SYNC}	Figure 3a	50	–	ns
Inputs:				
SI				
t_{SETUP}		0.3	–	µs
t_{HOLD}		250	–	ns
All Other Inputs				
t_{SETUP}		1.7	–	µs
t_{HOLD}		300		ns
Output Propagation Delay	Test Conditions: $R_L = 5 k\Omega$, $C_L = 50 pF$, $V_{OUT} = 1.5V$	300	–	ns
SO and SK				
t_{pd1}		–	1.0	µs
t_{pd0}		–	1.0	µs
CKO				
t_{pd1}		–	0.25	µs
t_{pd0}		–	0.25	µs
All Other Outputs				
t_{pd1}		–	1.4	µs
t_{pd0}		–	1.4	µs
MICROBUS ® Timing	$C_L = 100 pF$, $V_{CC} = 5V \pm 5\%$			
Read Operation (Figure 4)				
Chip Select Stable before $\overline{RD}$ — t_{CSR}		65	–	ns
Chip Select Hold Time for $\overline{RD}$ — t_{RCS}		20	–	ns
$\overline{RD}$ Pulse Width — t_{RR}		400	–	ns
Data Delay from $\overline{RD}$ — t_{RD}		–	375	ns
$\overline{RD}$ to Data Floating — t_{DF}		–	250	ns
Write Operation (Figure 5)				
Chip Select Stable before $\overline{WR}$ — t_{CSW}		65	–	ns
Chip Select Hold Time for $\overline{WR}$ — t_{WCS}		20	–	ns
$\overline{WR}$ Pulse Width — t_{WW}		400	–	ns
Data Set-Up Time for $\overline{WR}$ — t_{DW}		320	–	ns
Data Hold Time for $\overline{WR}$ — t_{WD}		100	–	ns
INTR Transition Time from $\overline{WR}$ — t_{WI}		–	700	ns

Note 1 : Duty cycle = t_{W1} ($t_{W1} + t_{W0}$).
Note 2 : See Figure 9 for additional I/O characteristics.
Note 3 : Voltage change must be less than 0.5 volt in a 1 ms period.
Note 4 : Exercise great care not to exceed maximum device power dissipation limits when direct driving LEDs (or sourcing similar loads) at high temperature.

FIGURE 2 – CONNECTION DIAGRAMS



Order number ET9420/N ET9320/N
Package N28A

Order number ET9421/N, ET9321/N
Package N24A

Order number ET9422/N ET9322/N
Package N20A

Pin	Description
L_7 - L_0	8 bidirectional I/O ports with TRI-STATE®
G_3 - G_0	4 bidirectional I/O ports
D_3 - D_0	4 general purpose outputs
IN_3 - IN_0	4 general purpose inputs (ET9420/9320 only)
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)

Pin	Description
SK	Logic-controlled clock (or general purpose output)
CKI	System oscillator input
CKO	System oscillator output (or general purpose input or RAM power supply)
$\overline{RESET}$	System reset input
V_{CC}	Power supply
GND	Ground

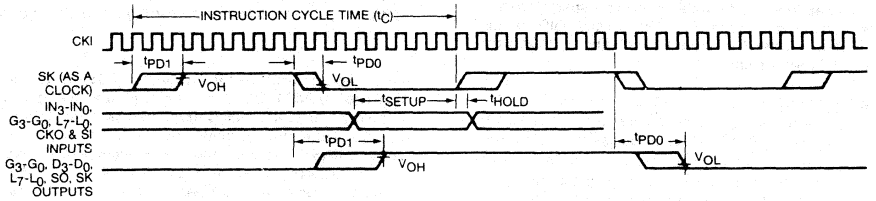


FIGURE 3 – INPUT/OUTPUT TIMING DIAGRAMS (CRYSTAL DIVIDE BY 16 MODE)

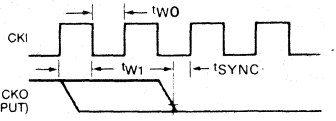


FIGURE 3a – SYNCHRONIZATION TIMING

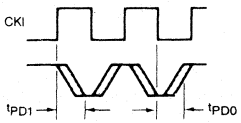


FIGURE 3b – CKO OUTPUT TIMING

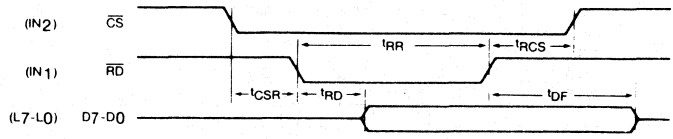


FIGURE 4 – MICROBUS® READ OPERATION TIMING

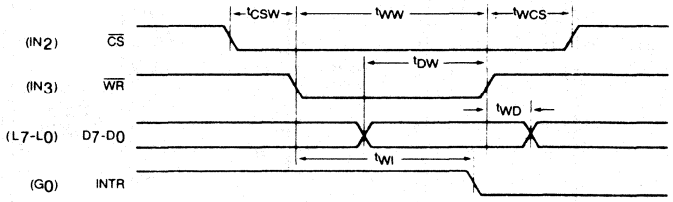


FIGURE 5 – MICROBUS® WRITE OPERATION TIMING

FUNCTIONAL DESCRIPTION

For ease of reading this description, only ET9420 and or ET9421 are referenced ; however, all such references apply equally to the ET9422, 9322, 9320 and or ET9321, respectively.

A block diagram of the ET9420 is given in figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2 volts). When a bit is reset, it is a logic "0" (less than 0.8 volts).

Program Memory

Programm Memory consists of a 1.024 byte ROM. As can be seen by an examination of the ET9420/9421/9422 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQID instructions, ROM must often be thought of as being organized into 16 pages of 64 words each.

ROM addressing is accomplished by a 10-bit PC register. Its binary value selects one of the 1,024 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 10-bit binary count value. Three levels of subroutine nesting are implemented by the 10-bit subroutine save registers, SA, SB and SC, providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

Data Memory

Data memory consists of a 256-bit RAM, organized as 4 data registers of 16 4-bit digits. RAM addressing is implemented by a 6-bit **B register** whose upper 2 bits (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the 6-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

Internal Logic

The 4-bit **A register** (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch data, to input 4 bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions of the ET9420/9421/9422, storing its results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below).

Four **general-purpose inputs,** IN_3-IN_0, are provided; IN_1, IN_2 **and** IN_3 may be selected, by a mask-programmable option, as Read Strobe, Chip Select and Write Strobe inputs, respectively, for use in MICROBUS® applications.

The **D register** provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The **G register** contents are outputs to 4 general-purpose bidirectional I/O ports. G_0 may be mask-programmed as an output for MICROBUS® applications.

The **Q register** is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction). With the MICROBUS™ option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurence of a write strobe from the host CPU.

The **8 L drivers**, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS™ option allows L I/O port data to be latched into the Q register. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa-Sg and decimal point segments of the display.

The **SIO register** functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register. (See EN register description, below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/parallel-out shift registers.

The XAS instruction copies C into the **SKL latch**. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

The **EN register** is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

1. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") ocurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. (See 4 below.) The SK output becomes a logic-controlled clock.
2. With EN_1 set the IN_1 input is enabled as an interrupt input. Immediately following an interrupt, EN_1 is reset to disable further interrupts.
3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high-impedance input state.
4. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0." The table below provides a summary of the modes associated with EN_3 and EN_0.

Enable Register Modes – Bits EN_3 and EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = CLOCK If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = CLOCK If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

Interrupt

The following features are associated with the IN_1 interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack, pushing in turn the contents of the other subroutine-save registers to the next lower level (PC + 1 → SA → SB → SC). Any previous contents of SC are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN_1 is reset.

b. An interrupt will be acknowledged only after the following conditions are met:
   1. EN_1 has been set.
   2. A low-going pulse ("1" to "0") at least two instruction cycles wide occurs on the IN_1 input.
   3. A currently executing instruction has been completed.
   4. All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the *end* of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. *At this time*, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines and LQID instructions should not be nested within the interrupt service routine, since their popping the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The first instruction of the interrupt routine at hex address 0FF must be a NOP.

e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

Microbus® Interface

The ET9420 has an option which allows it to be used as a peripheral microprocessor device, inputting and outputting data from and to a host microprocessor (μP). IN_1, IN_2 and IN_3 general purpose inputs become **MICROBUS® compatible** read-strobe, chip-select, and write-strobe lines, respectively. IN_1 becomes $\overline{RD}$ — a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the μP. IN_2 becomes $\overline{CS}$ — a logic "0" on this line selects the ET9420 as the μP peripheral device by enabling the operation of the $\overline{RD}$ and $\overline{WR}$ lines and allows for the selection of one of several peripheral components. IN_3 becomes $\overline{WR}$ — a logic "0" on this line will write bus data from the L ports to the Q latches for input to the ET9420. G_0 becomes INTR a "ready" output, reset by a write pulse from the μP on the $\overline{WR}$ line, providing the "handshaking capability necessary for asynchronous data transfer between the host CPU and the ET9420.

This option has been designed for compatibility with National's MICROBUS™ — a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS™ National Publication.) The functioning and timing relationships between the ET9420 signal lines affected by this option are as specified for the MICROBUS® interface, and are given in the AC electrical characteristics and shown in the timing diagrams (figures 4 and 5). Connection of the ET9420 to the MICROBUS® is shown in Figure 6.

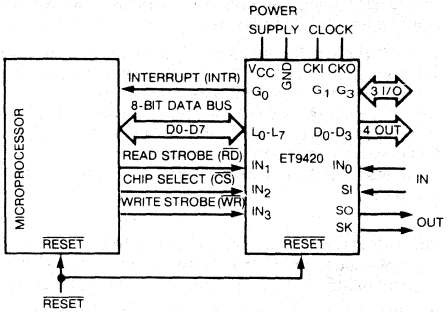


FIGURE 6 – MICROBUS® OPTION INTERCONNECT

Initialization

The Reset Logic, internal to the ET9420/9421/9422, will initialize (clear) the device upon power-up if the power supply rise time is less than 1ms and greater than 1μs. If the power supply rise time is greater than 1ms, the user must provide an external RC network and diode to the $\overline{RESET}$ pin as shown below. The $\overline{RESET}$ pin is configured as a Schmitt trigger input. If not used it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the RESET input, provided it stays low for at least three instruction cycle times.

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. *Data Memory (RAM) is not cleared upon initialization.* The first instruction at address 0 must be a CLRA.

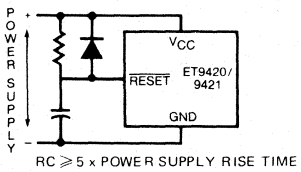


FIGURE 7 – POWER-UP CLEAR CIRCUIT

Oscillator

There are four basic clock oscillator configurations available as shown by figure 8.

a. **Crystal Controlled Oscillator.** CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 16 (optional by 8).

b. **External Oscillator.** CKI is an external clock input signal. The external frequency is divided by 16 (optional by 8) to give the instruction cycle time. CKO is now available to be used as the RAM power supply (V_R) or as a general purpose input.

c. **RC Controlled Oscillator.** CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available for non-timing functions.

d. **Externally Synchronized Oscillator.** Intended for use in multi-COP systems; CKO is programmed to function as an input connected to the SK output of another ET9420/-9421/9422 with CKI connected as shown. In this configuration, the SK output connected to CKO must provide a SYNC (instruction cycle) signal to CKO, thereby allowing synchronous data transfer between the COPs using only the SI and SO serial I/O pins in conjunction with the XAS instruction. Note that on power-up SK is automatically enabled as a SYNC output (See Functional Description, Initialization, above).

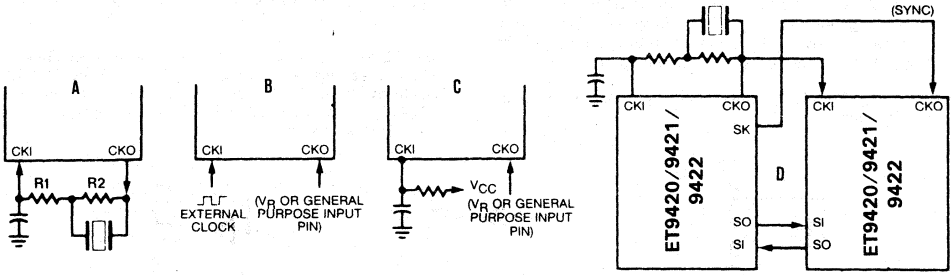
CKO Pin Options

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. As an option CKO can be a SYNC input as described above. As another option CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction. As another option, CKO can be a RAM power supply pin (V_R), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either option is appropriate in applications where the ET9420/-9421/9422 system timing configuration does not require use of the CKO pin.

RAM Keep-Alive Option (Not available on ET9422)

Selecting CKO as the RAM power supply (V_R) allows the user to shut off the chip power supply (V_{CC}) and maintain data in the RAM. To insure that RAM data integrity is maintained, the following conditions must be met:

1. $\overline{\text{RESET}}$ must go low before V_{CC} goes below spec during power off; V_{CC} must be within spec before $\overline{\text{RESET}}$ goes high on power up.
2. V_R must be within the operating range of the chip, and equal to $V_{CC} \pm 1V$ during normal operation.
3. V_R must be $\geq 3.3V$ with V_{CC} off.



Crystal Oscillator **External Oscillator** **RC Controlled Oscillator** **Externally Synchronized Oscillator**

Crystal Oscillator

Crystal Value	Component Values		
	R1 (Ω)	R2 (Ω)	C (pF)
4 MHz	1k	1M	27
3.58 MHz	1k	1M	27
2.09 MHz	1k	1M	56

RC Controlled Oscillator

R (kΩ)	C (pF)	Instruction Cycle Time (μs)
12	100	5 ± 20%
6.8	220	5.3 ± 23%
8.2	300	8 ± 29%
22	100	8.6 ± 16%

Note: $50k\Omega \geq R \geq 5k\Omega$
$360pF \geq C \geq 50pF$

FIGURE 8 — ET9420/9421/9422/ET9320/9321/9322 OSCILLATOR

I/O Options

ET9420/9421/9422 outputs have the following optional configurations, illustrated in Figure 9a :

a. Standard — an enhancement mode device to ground in conjunction with a depletion-mode device to V_{CC}, compatible with TTL and CMOS input requirements. Available on SO, SK, and all D and G outputs.

b. Open-Drain — an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, and all D and G outputs.

c. Push-Pull — An enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.

d. Standard L — same as **a.**, but may be disabled. Available on L outputs only.

e. Open Drain L — same as **b.**, but may be disabled. Available on L outputs only.

f. LED Direct Drive — an enhancement-mode device to ground and to V_{CC}, meeting the .typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (See Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display.

g. TRI-STATE® Push-Pull — an enhancement-mode device to ground and V_{CC}. These outputs are TRI-STATE outputs, allowing for connection of these outputs to a data bus shared by other bus drivers.

ET9420/9421/9422 inputs have the following optional configurations :

h. An on-chip depletion load device to V_{CC}.

i. A Hi-Z input which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in Figure 9b for each of these devices to allow the designer to effectively use these I/O configurations in designing a ET9420/9421/9422 system.

The SO, SK outputs can be configured as shown in **a.**, **b.**, or **c.** The D and G outputs can be configured as shown in **a.** or **b.** Note that when inputting data to the G ports, the G outputs should be set to "1." The L outputs can be configured as in **d.**, **e.**, **f.** or **g.**

An important point to remember if using configuration **d.** or **f.** with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current (see Figure 9b, device 2); however, when the L lines are used as inputs, the disabled depletion device can *not* be relied on to source sufficient current to pull an input to logic "1".

ET9421

If the ET9420 is bonded as a 24-pin device, it becomes the ET9421, illustrated in Figure 2, ET9420/9421 Connection Diagrams. Note that the ET9421 does not contain the four general purpose IN inputs (IN_3-IN_0). Use of this option precludes, of course, use of the IN options, interrupt feature, and the MICROBUS™ option which uses IN_1-IN_3. All other options are available for the ET9421.

ET9422

If the ET9420 is bonded as a 20-pin device, it becomes the ET9422, as illustrated in Figure 2. Note that the ETL9422 contains all the ET9421 pins except D0, D1, G0 and G1. ET9422 also does not allow RAM power supply input as a valid CKO pin option.

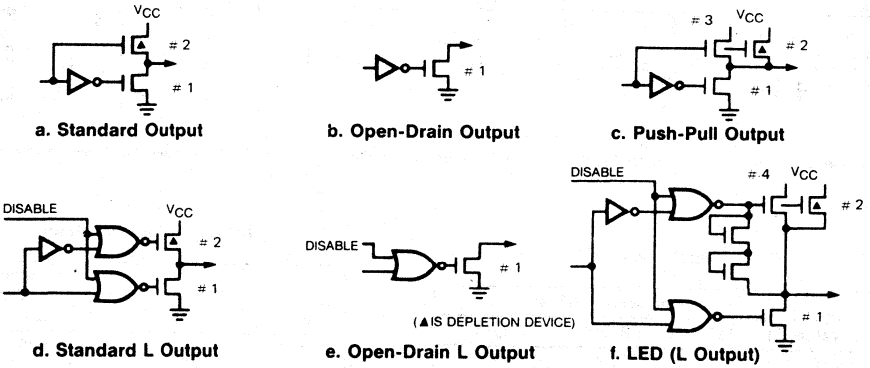
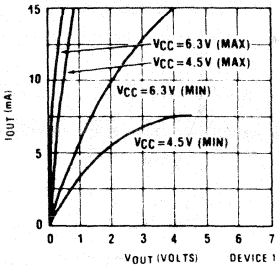
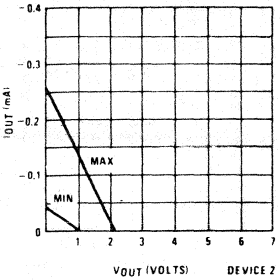


FIGURE 9a – INPUT/OUTPUT CONFIGURATIONS

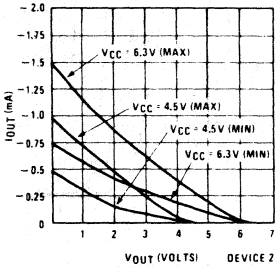
Output Sink Current



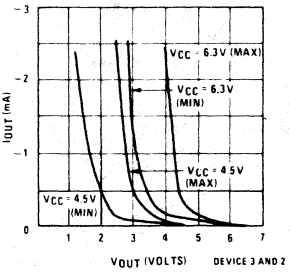
L Output Depletion Load OFF Source Current



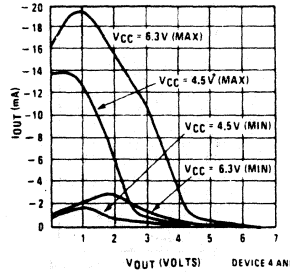
Standard Output Source Current



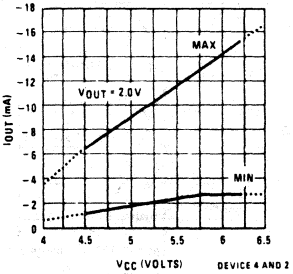
Push-Pull Source Current



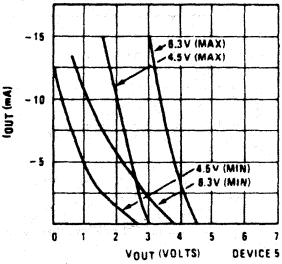
LED Output Source Current



LED Output Direct LED Drive



TRI-STATE ® Output Source Current



Input Load Source Current

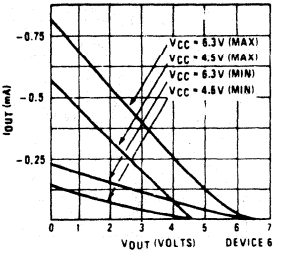


FIGURE 9b — ET9420/9421/9422 INPUT/OUTPUT CHARACTERISTICS

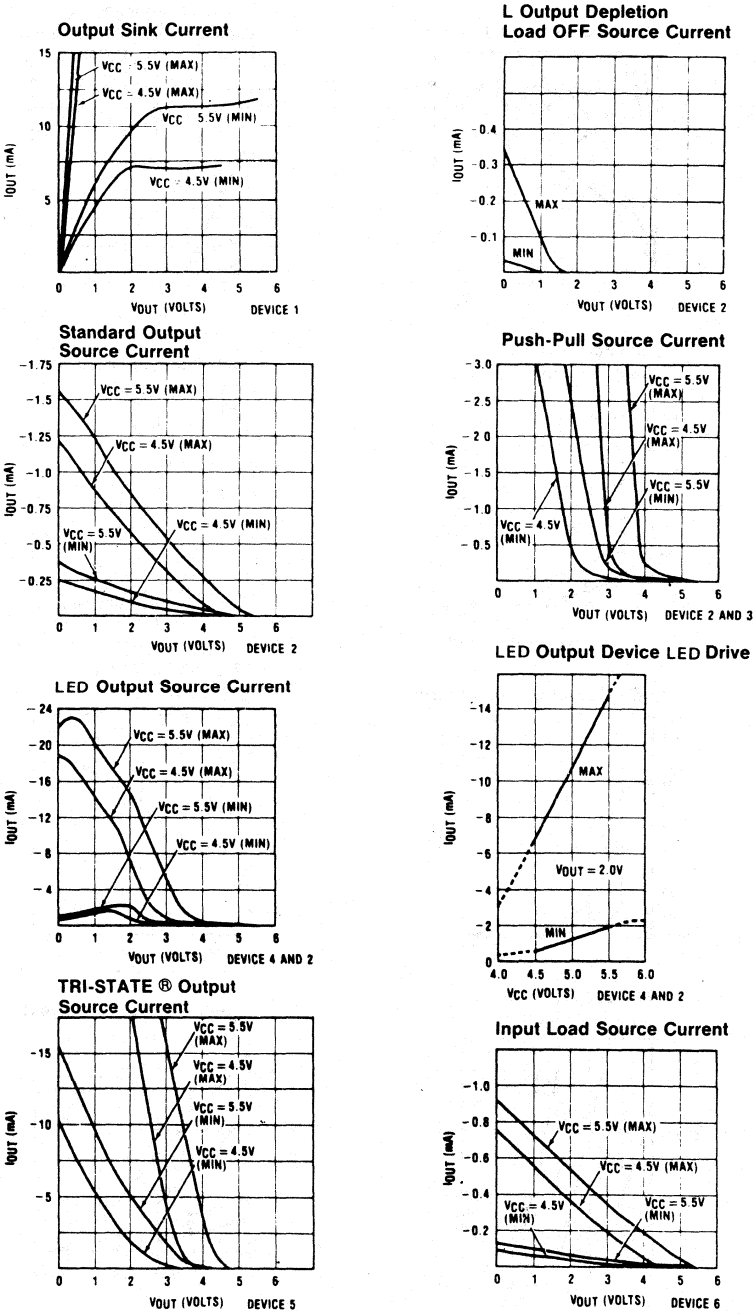


FIGURE 9c — ET9320/9321/9322 INPUT/OUTPUT CHARACTERISTICS

INSTRUCTION SET

Table 1 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 2 provides the mnemonic, operand, machine code, data flow, skip conditions, and description associated with each instruction in the ET9420/9421/9422 instruction set.

TABLE 2 – ET9420/9421/9422. ET9320/9321/9322 INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
IL	Two 1-bit latches associated with the IN_3 or IN_0 inputs
IN	4-bit Input Port
L	8-bit TRI-STATE® I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
PC	10-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	10-bit Subroutine Save Register A
SB	10-bit Subroutine Save Register B
SC	10 Subroutine Save Register A
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0-15 binary (RAM Digit Select)
r	2-bit Operand Field, 0-3 binary (RAM Register Select)
a	10-bit Operand Field, 0-1023 binary (ROM Address)
y	4-bit Operand Field, 0-15 binary (Immediate Data)
RAM(s)	Contents of RAM location addressed by s
ROM(t)	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
—	Minus
→	Replaces
↔	Is exchanged with
=	Is equal to
$\overline{A}$	The one's complement of A
⊕	Exclusive-OR
:	Range of values

TABLE 2 – ET9420/9421/9422. ET9320/9321/9322 INSTRUCTION SET

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011|0000	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0011|0001	A + RAM(B) → A	None	Add RAM to A
ADT		4A	0100|1010	A + 10_{10} → A	None	Add Ten to A
AISC	y	5-	0101| y	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CASC		10	0001|0000	$\overline{A}$ + RAM(B) + C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	0000|0000	0 → A	None	Clear A
COMP		40	0100|0000	$\overline{A}$ → A	None	One's complement of A to A
NOP		44	0100|0100	None	None	No Operation
RC		32	0011|0010	"0" → C	None	Reset C
SC		22	0010|0010	"1" → C	None	Set C
XOR		02	0000|0010	A⊕RAM(B) → A	None	Exclusive-OR RAM with A

TABLE 2 – ET9420/9421/9422. ET9320/9321/9322 INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1111|1111	ROM ($PC_{9:8}$, A,M) → $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6-	0110|00|$a_{9:8}$	a → PC	None	Jump
		--	$a_{7:0}$			
JP	a	--	1| $a_{6:0}$ (pages 2,3 only)	a → $PC_{6:0}$	None	Jump within Page (Note 4)
			or			
		--	11| $a_{5:0}$ (all other pages)	a → $PC_{5:0}$		
JSRP	a	--	10| $a_{5:0}$	PC + 1 → SA → SB → SC 0010 → $PC_{9:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6-	0110|10|$a_{9:8}$	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
		--	$a_{7:0}$			
RET		48	0100|1000	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0100|1001	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33	0011|0011	A → $Q_{7:4}$ RAM(B) → $Q_{3:0}$	None	Copy A, RAM to Q
		3C	0011|1100			
CQMA		33	0011|0011	$Q_{7:4}$ → RAM(B) $Q_{3:0}$ → A	None	Copy Q to RAM, A
		2C	0010|1100			
LD	r	-5	00| r |0101	RAM(B) → A Br⊕r → Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	23	0010|0011	RAM(r,d) → A	None	Load A with RAM pointed to directly by r,d
		--	00| r | d			
LQID		BF	1011|1111	ROM($PC_{9:8}$,A,M) → Q SB → SC	None	Load Q Indirect (Note 3)
RMB	0	4C	0100|1100	0 → $RAM(B)_0$	None	Reset RAM Bit
	1	45	0100|0101	0 → $RAM(B)_1$		
	2	42	0100|0010	0 → $RAM(B)_2$		
	3	43	0100|0011	0 → $RAM(B)_3$		
SMB	0	4D	0100|1101	1 → $RAM(B)_0$	None	Set RAM Bit
	1	47	0100|1101	1 → $RAM(B)_1$		
	2	46	0100|0110	1 → $RAM(B)_2$		
	3	4B	0100|1011	1 → $RAM(B)_3$		

TABLE 2 – ET9420/9421/9422. ET9320/9321/9322 INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS (continued)						
STII	y	7-	0111 y	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	-6	00 r 0110	RAM(B) ↔ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23 --	0010 0011 10 r d	RAM(r,d) ↔ A	None	Exchange A with RAM pointed to directly by r,d
XDS	r	-7	00 r 0111	RAM(B) ↔ A Bd – 1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	-4	00 r 0100	RAM(B) ↔ A Bd + 1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101 0000	A → Bd	None	Copy A to Bd
CBA		4E	0100 1110	Bd → A	None	Copy Bd to A
LBI	r,d	-- (d = 0, 9:15) or 33 -- (any d)	00 r (d – 1) 0011 0011 10 r d	r,d → B	Skip until not a LBI	Load B immediate with r,d (Note 6)
LEI	y	33 6-	0011 0011 0110 y	y → EN	None	Load EN Immediate (Note 7)
XABR		12	0001 0010	A ↔ Br (0,0 → A_3,A_2)	None	Exchange A with Br
TEST INSTRUCTIONS						
SKC		20	0010 0000		C = "1"	Skip if C is True
SKE		21	0010 0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0011 0011 0010 0001		$G_{3:0} = 0$	Skip if G is Zero (all 4 bits)
SKGBZ		33	0011 0011	1st byte		Skip if G Bit is Zero
	0	01	0000 0001	2nd byte	$G_0 = 0$	
	1	11	0001 0001		$G_1 = 0$	
	2	03	0000 0011		$G_2 = 0$	
	3	13	0001 0011		$G_3 = 0$	
SKMBZ	0	01	0000 0001		$RAM(B)_0 = 0$	Skip if RAM Bit is Zero
	1	11	0001 0001		$RAM(B)_1 = 0$	
	2	03	0000 0011		$RAM(B)_2 = 0$	
	3	13	0001 0011		$RAM(B)_3 = 0$	
SKT		41	0100 0001		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)

TABLE 2 – ET9420/9421/9422. ET9320/9321/9322 INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	0011 0011 0010 1010	G → A	None	Input G Ports to A
ININ		33 28	0011 0011 0010 1000	IN → A	None	Input IN Inputs to A (Note 2)
INIL		33 29	0011 0011 0010 1001	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (Note 3)
INL		33 2E	0011 0011 0010 1110	$L_{7:4}$ → RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM,A
OBD		33 3E	0011 0011 0011 1110	Bd → D	None	Output Bd to D Outputs
OGI	y	33 5-	0011 0011 0101 y	y → G	None	Output to G Ports Immediate
OMG		33 3A	0011 0011 0011 1010	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0100 1111	A ↔ SIO, C → SKL	None	Exchange A with SIO (Note 3)

Note 1 : All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2 : The ININ instruction is not available on the ET9421/ET9321 and ET9422/ET9322 since these devices do not contain the IN inputs.

Note 3 : For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4 : The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5 : A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6 : LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14 or 15. The machine code for the lower 4 bits equals the binary value of the "d" data *minus 1*, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equals 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 7 : Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register).

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing ET9420/9421/9422 programs.

XAS Instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register, above.) If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM addressed by the 10-bit word, $PC_{9:8}$, A, M. PC_9 and PC_8 are not affected by this instruction.

Note that JID requires 2 instruction cycles to execute.

INIL Instruction

INIL (Input IL Latches to A) inputs 2 latches, IL_3 and IL_0 (see figure 10) and CKO into A. The IL_3 and IL_0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN_3 and IN_0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs IL_3 and IL_0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN_3 and IN_0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A "0" is always placed in A1 upon the execution of an INIL. The general purpose inputs IN_3-IN_0 are input to A upon execution of an ININ instruction. (See table 2, ININ instruction.) INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction.

Note: IL latches are not cleared on reset.

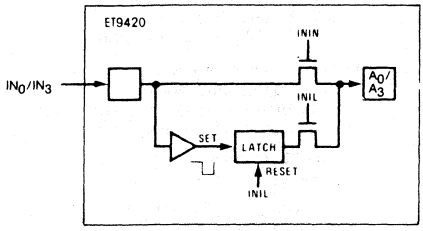


FIGURE 10.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 10-bit word PC_9, PC_8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB → SC) and replaces the least significant 8 bits of PC as follows: A → $PC_{7:4}$, RAM(B) → $PC_{3:0}$, leaving PC_9 and PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the contents of SB are placed in SC (SB → SC). Note that LQID takes two instruction cycle times to execute.

SKT Instruction

The SKT (Ship On Timer) instruction tests the state of an internal 10-bit time-base counter. This counter divides the instruction cycle clock frequency by 1024 and provides a latched indication of counter overflow. The SKT instruction tests this latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction, therefore, allow the ET9420/9421/9422 to generate its own time-base for real-time processing rather than relying on an external input signal.

For example, using a 2.097 MHz crystal as the time-base to the clock generator, the instruction cycle clock frequency will be 131 kHz (crystal frequency – 16) and the binary counter output pulse frequency will be 128 Hz. For time-of-day or similar real-time processing, the SKT instruction can call a routine which increments a "seconds" counter every 128 ticks.

Instruction Set Notes

a. **The first word of a ET9420/9421/9422 program (ROM address 0) must be a CLRA (Clear A) instruction.**

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths take the same number of cycle times whether instructions are skipped or executed except JID and LQID. LQID and JID take two cycle times if executed and one if skipped.

c. The ROM is organized into 16 pages of 64 words each. The Program Counter is an 10-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3, 7, 11 or 15 will access data in the next group of four pages.

OPTION LIST

The ET9420/9421/9422 mask programmable options are assigned numbers which correspond with the ET9420 pins.

The following is a list of ET9420 options. When specifying a ET9421 or ET9422 chip, Options 9, 10, 19, 20 and 29 must all be set to zero. When specifying a ET9422 chip, Options 21, 22, 27 and 28 must also be zero, and Option 2 must not be a 1. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Pin
- = 0: clock generator output to crystal (0 not available if option 3 = 4 or 5)
- = 1: pin is RAM power supply (V_R) input (Not available on ET9422, ET9322)
- = 2: general purpose input with load device
- = 3: multi-COP SYNC input
- = 4: general purpose Hi Z input

Option 3: CKI Input
- = 0: crystal input divided by 16
- = 1: crystal input divided by 8
- = 2: TTL external clock input divided by 16
- = 3: TTL external clock input divided by 8
- = 4: single-pin RC controlled oscillator (−4)
- = 5: Schmitt trigger clock input (−4)

Option 4: RESET Pin
- = 0: Load devices to V_{CC}
- = 1: Hi-Z input

Option 5: L_7 Driver
- = 0: Standard output (figure 9D)
- = 1: Open-Drain output (E)
- = 2: LED direct drive output (F)
- = 3: TRI-STATE®push-pull output (G)

Option 6: L_6 Driver
same as Option 5

Option 7: L_5 Driver
same as Option 5

Option 8: L_4 Driver
same as Option 5

Option 9: IN_1 Input
- = 0: load device to V_{CC} (H)
- = 1: Hi-Z input (I)

Option 10: IN_2 Input
same as Option 9

Option 11 = 0: V_{CC} Pin — no options available

Option 12: L_3 Driver
same as Option 5

Option 13: L_2 Driver
same as Option 5

Option 14: L_1 Driver
same as Option 5

Option 15: L_0 Driver
same as Option 5

Option 16 : SI Input
same as Option 9

Option 17: SO Driver
- = 0: standard output (A)
- = 1: open-drain output (B)
- = 2: push-pull output (C)

Option 18: SK Driver
same as Option 17

Option 19: IN_0 Input
same as Option 9

Option 20: IN_3 Input
same as Option 9

Option 21: G_0 I/O Port
- = 0: Standard output (A)
- = 1: Open-Drain output (B)

Option 22: G_1 I/O Port
same as Option 21

Option 23: G_2 I/O Port
same as Option 21

Option 24: G_3 I/O Port
same as Option 21

Option 25: D_3 Output
- = 0: Standard output (A)
- = 1: Open-Drain output (B)

Option 26: D_2 Output
same as Option 25

Option 27: D_1 Output
same as Option 25

Option 28: D_0 Output
same as Option 25

Option 29: Chip Function
- = 0: normal operation
- = 1: MICROBUS® option

Option 30: Chip Bonding
- = 0: ET9420 (28-pin device)
- = 1: ET9421 (24-pin device)
- = 2: 28 and 24-pin versions
- = 3: ET9422 (20-pin device)
- = 4: 28- and 20-pin versions
- = 5: 24- and 20-pin versions
- = 6: 28-, 24-, and 20-pin versio

Option 31: IN Input Levels
- = 0: normal input levels
- = 1: Higher voltage input leve ("0" = 1.2V, "1" = 3.6V)

Option 32: G Input Levels
same as Option 31

Option 33: L Input Levels
same as Option 31

Option 34: CKO Input Levels
same as Option 31

Option 35: SI Input Levels
same as Option 31

TEST MODE (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed ET9420. With SO forced to logic "1", two test modes are provided, depending upon the value of SI :

a. RAM and Internal Logic Test Mode (SI = 1)

b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user; they are intended for manufacturing test only.

APPLICATION EXAMPLE : ET9420 General Controller

Figure 9 shows an interconnect diagram for a ET9420 used as a general controller. Operation of the system is as follows :

1. The L_7-L_0 outputs are configured as LED Direct Drive outputs, allowing direct connection to the segments of the display.
2. The D_3-D_0 outputs drive the digits of the multiplexed display directly and scan the columns of the 4 x 4 keyboard matrix.
3. The IN_3-IN_0 inputs are used to input the 4 rows of the keyboard matrix. Reading the IN lines in conjunction with the current value of the D outputs allows detection, debouncing, and decoding of any one of the 16 keyswitches.
4. CKI is configured as a single-pin oscillator input allowing system timing to be controlled by a single-pin RC network. CKO is therefore available for use as a V_R RAM power supply pin. RAM data integrity is thereby assured when the main power supply is shut down (see RAM Keep-Alive Option description).
5. SI is selected as the input to a binary counter input. With SIO used as a binary counter, SO and SK can be used as general purpose outputs.
6. The 4 bidirectional G I/O ports (G_3-G_0) are available for use as required by the user's application.

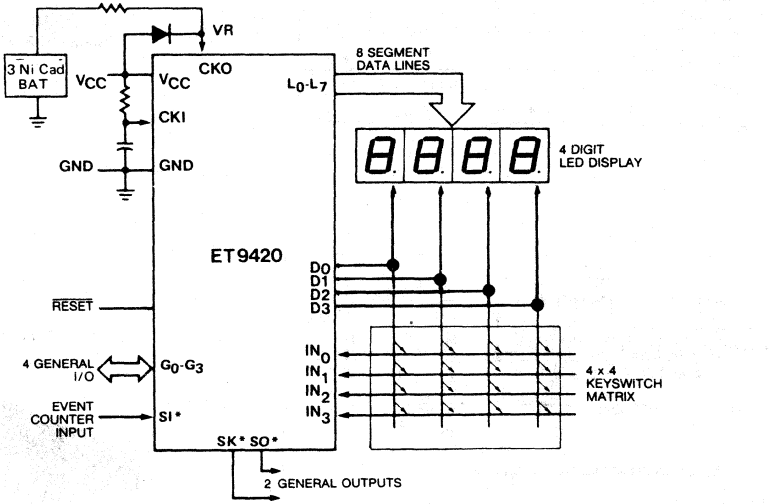


FIGURE 11 – ET9420 KEYBOARD/DISPLAY INTERFACE

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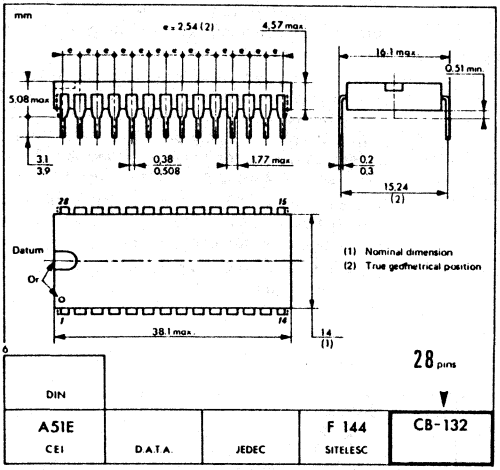
PHYSICAL DIMENSIONS



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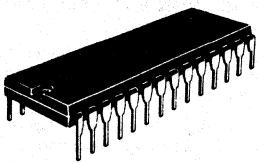

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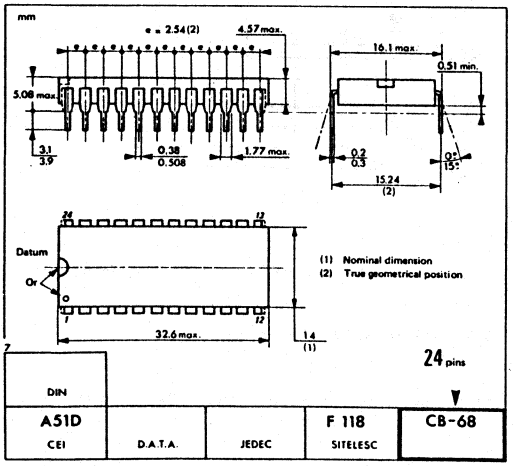

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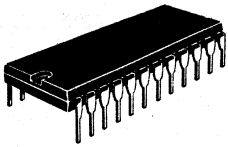

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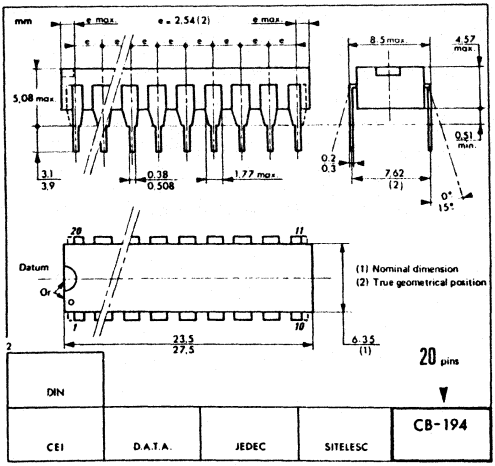
PHYSICAL DIMENSIONS



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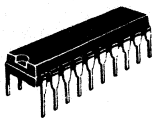

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NOTES

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HOMSON COMPONENTS
EMICONDUCTEURS

ETC9420/21/22 • ETC9320/21/22
ETC9444/45 • ETC9344/45
SINGLE SHIP MICROCONTROLLERS

The ETC 9420, C 9421, C 9422, C 9320, C 9321, C 9322, and ETC 9445, C 9344, C 9345 fully static single-chip CMOS microcontrollers are fully compatible with the COPS® family, fabricated using double-poly, silicon gate complementary MOS technology. These Controller Oriented Processors are complete microcontrollers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications.

Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The ETC 9420, C 9444 are 28-pin chips. The ETC 9421, C 9445 are 24-pin versions (4 inputs removed) and C 9422 is a 20-pin version with 15 I/O lines. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized microcontroller at a low end -product cost.

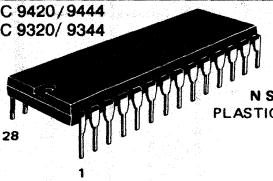
These microcontrollers are appropriate choices in many demanding control environments especially those with human interface.

- Lowest power dissipation (50 µW typical).
- Power saving IDLE state and HALT mode.
- Fully Static (can turn off the clock).
- 2 K x 8 ROM, 128 x 4 RAM (ETC 9444, C 9445).
- 1 K x 8 ROM, 64 x 4 RAM (ETC 9420, C 9421, C 9422).
- True vectored interrupt, plus restart.
- 3-level subroutine stack.
- 4 µsec intruction time, plus software selectable clocks.
- 23 I/Olines (ETC 9444, C 9420).
- Single supply operation (2.4 V to 5.5 V).
- Programmable read/write 8-bit timer/event counter.
- Internal binary counter register with MICROWIRE® serial I/O Capability.
- General purpose and tri-state® outputs.
- LSTTL/C MOS compatible.
- MICROBUS® compatible.
- Software/hardware compatible with other members of ET 9400 family.
- Extended temperature range devices ETC 9320/ETC 9321, ETC 9322 and ETC 9344/ETC 9345 (— 40° C to +85°C).
- Military devices (—55°C to +125°C) to be available.

CMOS

SINGLE CHIP MICROCONTROLLERS

ETC 9420/9444
ETC 9320/ 9344



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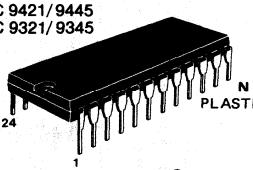
ETC 9421/9445
ETC 9321/9345



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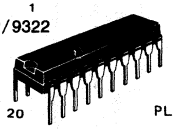
ETC 9422/9322



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PIN ASSIGNMENT

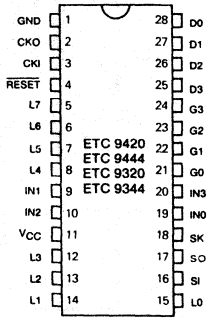

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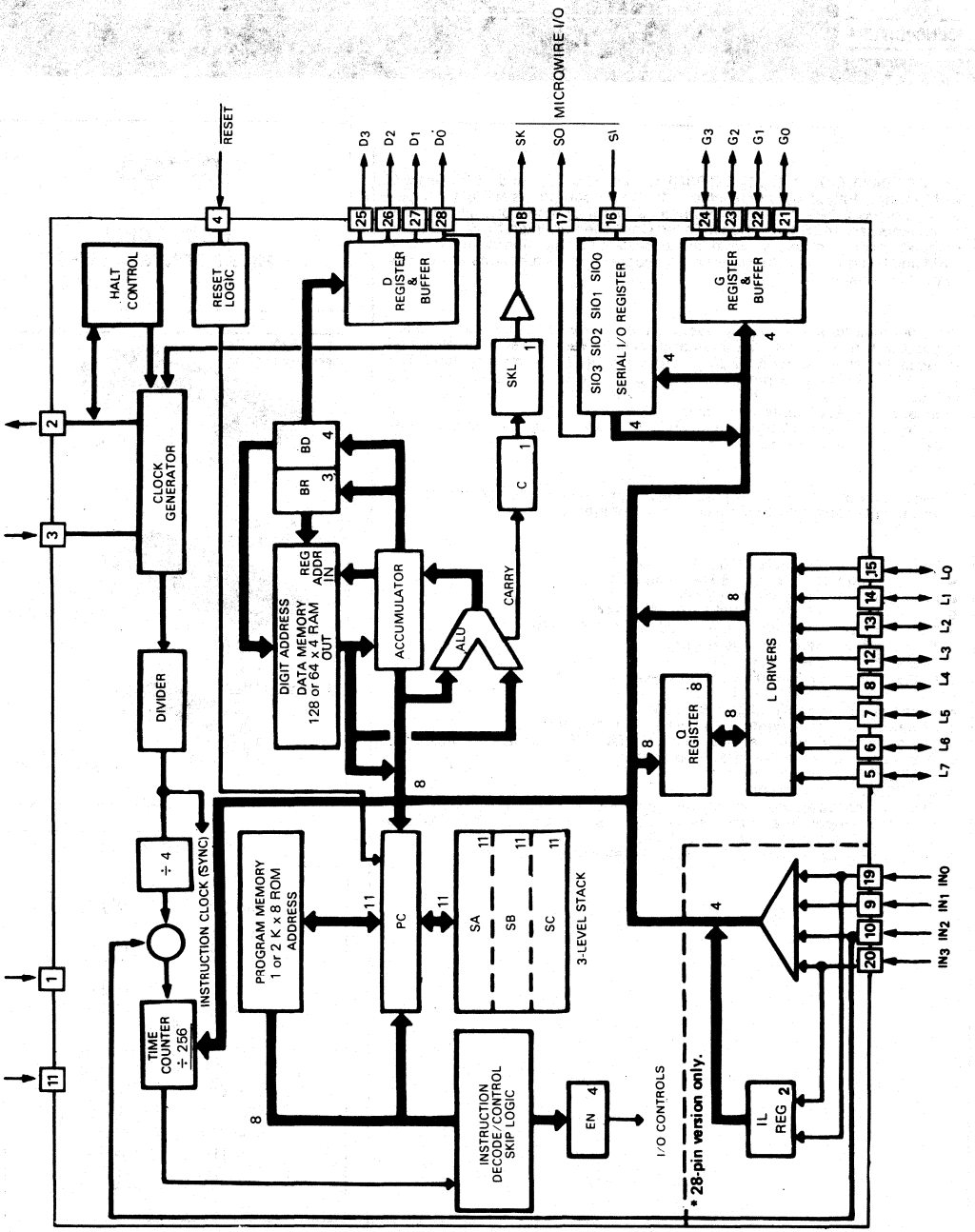
FIGURE 1 – BLOCK DIAGRAM (28-pin version)



ETC9420, ETC9421, ETC9422 • ETC9444, ETC9445

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Vcc)	6 V
Voltage at any pin	−0.3 V to V_{CC} + 0.3 V
Total Allowable Source current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	0° C to + 70° C
Storage Temperature Range	−65° C to + 150° C
Lead Temperature (soldering 10 seconds)	300° C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are note insured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$ (Unless otherwise specified)

Parameter	Conditions	Min	Max	Units
Operating Voltage		2.4	5.5	V
Power Supply Ripple (Note 5)	Peak to Peak	–	0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 2.4 V, tc = 64 µs	–	120	µA
	V_{CC} = 5.0 V, tc = 16 µs	–	700	µA
	V_{CC} = 5.0 V, tc = 4 µs (tc = instruction cycle time)	–	3000	µA
Halt Mode Current (Note 2)	V_{CC} = 5.0 V, Fin = 0 kHz	–	40	µA
	V_{CC} = 2.4 V, Fin = 0 kHz	–	12	µA
Input Voltage levels				
RESET CKI (RC or crystal opt.)				
Do (Clock input)				
Logic High		0.9 V_{CC}	–	V
Logic Low			0.1 V_{CC}	V
All other inputs				
Logic High		0.7 V_{CC}	–	
Logic Low		–	0.2 V_{CC}	V
Input Pull-up current	V_{CC} = 4.5 V, V_{IN} = 0	30	330	µA
HI-Z input leakage		−1	+1	µA
Input capacitance (Note 4)		–	7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0 V ± 5 %			
Logic High	I_{OH} = −100 µA	2.7	–	V
Logic Low	I_{OL} = 400 µA		0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 µA	V_{CC}−0.2	–	V
Logic Low	I_{OL} = 10 µA	–	0.2	V
Output current Level (except CKO)				
Sink (Note 6)	V_{CC} = 4.5 V, Vout = V_{CC}	1.2	–	mA
	V_{CC} = 2.4 V, Vout = V_{CC}	0.2	–	mA
Source (standard option)	V_{CC} = 4.5 V, Vout = 0V	0.5	–	mA
	V_{CC} = 2.4 V, Vout = 0V	0.1	–	mA
Source (Low current option)	V_{CC} = 4.5 V, Vout = 0V	30	330	µA
	V_{CC} = 2.4 V, Vout = 0V	6	80	µA
CKO Current level (As clock out)				
Sink ÷ 4	V_{CC} = 4.5 V, CKI = V_{CC} V_{OUT} = V_{CC}	0.3	–	mA
÷ 8		0.6	–	mA
÷ 16		1.2	–	mA
Source ÷ 4	V_{CC} = 4.5 V, CKI = 0V, V_{OUT} = 0V	0.3	–	mA
÷ 8		0.6	–	mA
÷ 16		1.2	–	mA
Allowable Sink Source current per pin (Note 6)		–	5	mA
Allowable loading on CKO (as HALT)		–	100	pF
Current needed to over-ride HALT (Note 3)				
To continue	V_{CC} = 4.5 V, Vin = 0.2 V_{CC}	–	0.7	mA
To halt	V_{CC} = 4.5 V, Vin = 0.7 V_{CC}	–	1.6	mA
TRI-STATE or open drain Leakage current		−2.5	+2.5	µA

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$ (Unless otherwise specified)

Parameter	Conditions	Min	Max	Units
Instruction cycle time (tc)	$V_{CC} \geq 4.5$ V	4	DC	µs
	$4.5 V > V_{CC} \geq 2.4$ V	16	DC	µs
Operating CKI Frequency				
÷ 4 mode	$V_{CC} \geq 4.5$ V	DC	1.0	MHz
÷ 8 mode		DC	2.0	MHz
÷ 16 mode		DC	4.0	MHz
÷ 4 mode	$4.5 V > V_{CC} \geq 2.4$ V	DC	250	kHZ
÷ 8 mode		DC	500	kHZ
÷ 16 mode		DC	1.0	MHz
Duty cycle (Note 4)	F1 = 4 MHz	40	60	%
Rise time (Note 4)	F1 = 4 MHz ext. dock	–	60	ns
Fall time (Note 4)	F1 = 4 MHz ext. dock	–	40	ns
Instruction cycle time (RC oscillator) (Note 4)	R = 30 K V_{CC} = 5 V, C = 82 pF, (÷ 4 Mode)	8	16	µs
INPUTS (fig. 3)				
t_{SETUP} G inputs	$V_{CC} \geq 4.5$ V	tc/4 +.7	–	µs
t_{SETUP} SI input		0.3	–	µs
t_{SETUP} All others		1.7	–	µs
t_{HOLD}	$V_{CC} \geq 4.5$ V	0.25	–	µs
	$4.5 V > V_{CC} \geq 2.4$ V	1.0	–	µs
OUTPUT PROPAGATION DELAY	Vout = 1.5 V, CL = 100 pF, R_L = 5 K			
t_{PD1}, t_{PDO}	$V_{CC} \geq 4.5$ V	–	1.0	µs
t_{PD1}, t_{PDO}	$4.5 V > V_{CC} \geq 2.4$ V	–	4.0	µs
MICROBUS® TIMING	C_L = 50 pF, V_{CC} = 5 V ± 5 %			µs
Read operation (fig. 4)				
Chip select stable before $\overline{RD}$ - t_{CSR}		65	–	ns
Chip select hold time for $\overline{RD}$ - t_{RCS}		20	–	ns
$\overline{RD}$ pulse width - t_{RR}		400	–	ns
Data delay from $\overline{RD}$ - t_{RD}		–	375	ns
$\overline{RD}$ to data floating - t_{DF} (note 4)		–	250	ns
Write operation (fig. 5)				
Chip select stable before $\overline{WR}$ - t_{CSW}		65	–	ns
Chip select hold time for $\overline{WR}$ - t_{WCS}		20	–	ns
$\overline{WR}$ pulse width - t_{WW}		400	–	ns
Data set-up time for $\overline{WR}$ - t_{DW}		320	–	ns
Data hold time for $\overline{WR}$ - t_{WD}		100	–	ns
INTR transition time for $\overline{WR}$ - t_{WI}		–	700	ns

Note 1 : Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20k resistors. See current drain equation on page 17.

Note 2 : The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions : all inputs tied to V_{CC}, L lines in TRI-STATE mode and tied to ground, all output low and tied to ground.

Note 3 : When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

Note 4 : This parameter is only sampled and not 100 % tested.

Note 5 : Voltage change must be less than 0.5 volt in a 1 ms period.

Note 6 : SO output sink current must be limited to keep V_{OL} below 0.2 V_{CC} when port is running in order to prevent entering test mode.

ETC9320, ETC9321, ETC9322 • ETC9344, ETC9345

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6 V
Voltage at any pin	−0.3 V to V_{CC} + 0.3 V
Total Allowable Source current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	−40° C to + 85° C
Storage Temperature Range	−65° C to + 150° C
Lead Temperature (soldering 10 seconds)	300° C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are note insured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS — 40° C ≤ T_A ≤ + 85° C (Unless otherwise specified)

Parameter	Conditions	Min	Max	Units
Operating Voltage		3.0	5.3	V
Power Supply Ripple (Note 5)	Peak to Peak	–	0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 3.0 V, t_C = 64 µs	–	180	µA
	V_{CC} = 5.0 V, tc = 16 µs	–	800	µA
	V_{CC} = 5.0 V, tc = 4 µs (tc = instruction cycle time)	–	3600	µA
Halt Mode Current (Note 2)	V_{CC} = 5.0 V, Fin = 0 kHz	–	60	µA
	V_{CC} = 3.0 V, Fin = 0 kHz	–	30	µA
Input Voltage levels				
RESET CKI (RC or crystal opt.)				
Do (Clock input)				
Logic High		0.9 V_{CC}	–	V
Logic Low		–	0.1 V_{CC}	V
All other inputs				
Logic High		0.7	–	
Logic Low		–	0.2 V_{CC}	V
Input Pull-up current	V_{CC} = 4.5 V, V_{IN} = 0	30	440	µA
HI-Z input leakage		−2	+2	µA
Input capacitance (Note 4)		–	7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0 V ± 5 %			
Logic High	I_{OH} = −100 µA	2.7	–	V
Logic Low	I_{OL} = 400 µA	–	0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 µA	V_{CC} −0.2	–	V
Logic Low	I_{OL} = 10 µA	–	0.2	V
Output current Level (except CKO)				
Sink (Note 6)	V_{CC} = 4.5 V, Vout = V_{CC}	1.2	–	mA
	V_{CC} = 3.0 V, Vout = V_{CC}	0.2	–	mA
Source (standard option)	V_{CC} = 4.5 V, Vout = 0V	0.5	–	mA
	V_{CC} = 3.0 V, Vout = 0V	0.1	–	mA
Source (Low current option)	V_{CC} = 4.5 V, Vout = 0V	30	440	µA
	V_{CC} = 3.0 V, Vout = 0V	8	200	µA
CKO Current level (As clock out)				
Sink ÷ 4	V_{CC} = 4.5 V, CKI = V_{CC}, Vout = V_{CC}	0.3	–	mA
÷ 8		0.6	–	mA
÷ 16		1.2	–	mA
Source ÷ 4	V_{CC} = 4.5 V, CKI = 0V, Vout = 0V	0.3	–	mA
÷ 8		0.6	–	mA
÷ 16		1.2	–	mA
Allowable Sink / Source current per pin (Note 6)		–	5	mA
Allowable loading on CKO (as HALT)		–	100	pF
Current needed to over-ride HALT (Note 3)				
To continue	V_{CC} = 4.5 V, Vin = 0.2 V_{CC}	–	0.9	mA
To halt	V_{CC} = 4.5 V, Vin = 0.7 V_{CC}	–	2.1	mA
TRI-STATE or open drain Leakage current		−5	+5	µA

AC ELECTRICAL CHARACTERISTICS – 40°C ≤ T_A ≤ + 85°C (Unless otherwise specified)

Parameter	Conditions	Min	Max	Units
Instruction cycle time (tc)	$V_{CC} \geq 4.5$ V	4	DC	µs
	4.5 V > $V_{CC} \geq 3.0$ V	16	DC	µs
Operating CKI Frequency				
÷ 4 mode	$V_{CC} \geq 4.5$ V	DC	1.0	MHz
÷ 8 mode		DC	2.0	MHz
÷ 16 mode		DC	4.0	MHz
÷ 4 mode	4.5 V > $V_{CC} \geq 3.0$ V	DC	250	kHZ
÷ 8 mode		DC	500	kHZ
÷ 16 mode		DC	1.0	MHz
Duty cycle (Note 4)	F1 = 4 MHz	40	60	%
Rise time (Note 4)	F1 = 4 MHz ext. clock	–	60	ns
Fall time (Note 4)	F1 = 4 MHz ext. clock	–	40	ns
Instruction cycle time (RC oscillator) (Note 4)	R = 30 K, V_{CC} = 5 V, C = 82 pF, (÷ 4 Mode)	8	16	µs
INPUTS (fig. 3)				
t_{SETUP} G inputs	$V_{CC} \geq 4.5$ V	(tc/4) + .7	–	µs
t_{SETUP} SI input		0.3	–	µs
t_{SETUP} All others		1.7	–	µs
t_{HOLD}	$V_{CC} \geq 4.5$ V	0.25	–	µs
	4.5 V > $V_{CC} \geq 3.0$ V	1.0	–	µs
OUTPUT				
PROPAGATION DELAY	Vout = 1.5 V, CL = 100 pF, RL = 5k			
t_{PD1}, t_{PDO}	$V_{CC} \geq 4.5$ V	–	1.0	µs
t_{PD1}, t_{PDO}	4.5 V > $V_{CC} \geq 3.0$ V	–	4.0	µs
MICROBUS® TIMING	C_L = 50 pF, V_{CC} = 5 V ± 5 %			
Read operation (fig. 4)				
Chip select stable before $\overline{RD}$ - t_{CSR}		65	–	ns
Chip select hold tome for $\overline{RD}$ - t_{RCS}		20	–	ns
$\overline{RD}$ pulse width - t_{RR}		400	–	ns
Data delay from $\overline{RD}$ - t_{RD}		–	375	ns
$\overline{RD}$ to data floating - t_{DF} (note 4)		–	250	ns
Write operation (fig. 5)				
Chip select stable before $\overline{WR}$ - t_{CSW}		65	–	ns
Chip select hold time for $\overline{WR}$ - t_{WCS}		20	–	ns
$\overline{WR}$ pulse width - t_{WW}		400	–	ns
Data set-up time for $\overline{WR}$ - t_{DW}		320	–	ns
Data hold time for $\overline{WR}$ - t_{WD}		100	–	ns
$\overline{INTR}$ transition time for $\overline{WR}$ - t_{WI}		–	700	ns

Note 1 : Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20k resistors. See current drain equation on page 17

Note 2 : The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions : all inputs tied to V_{CC}, L lines in TRI-STATE mode and tied to ground, all output low and tied to ground.

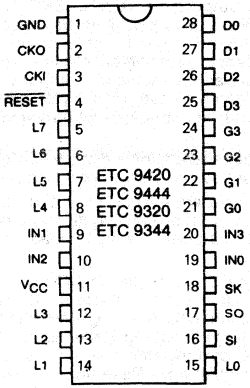
Note 3 : When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

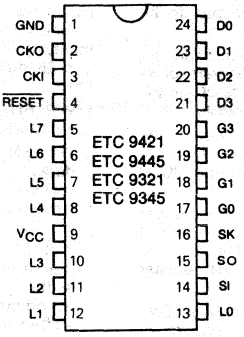
Note 4 : This parameter is only sampled and not 100 % tested.

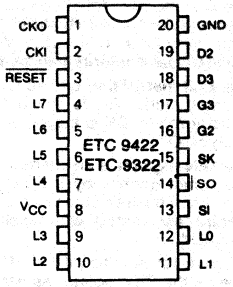
Note 5 : Voltage change must be less than 0.5 volt in a 1 ms period.

Note 6 : SO output sink current must be limited to keep V_{OL} below 0.2 V_{CC} when port is running in order to prevent entering test mode.

FIGURE 2 – CONNECTION DIAGRAMS







L_7-L_0	8 bit bidirectional I/O ports with TRI-STATE®
G_3-G_0	4 bit bidirectional I/O ports
D_3-D_1	3 bit general purpose outputs
D_0	General purpose output or oscillator input
IN_3-IN_0	4-bit input port (ETC 9420 or 9444 only)
SI	Serial input
SO	Serial output
SK	Logic-controlled clock or general purpose output
CKI	System oscillator input
CKO	System oscillator output (or general purpose Input or Halt I/O Port)
$\overline{RESET}$	System reset input
V_{CC}	Power supply
GND	Ground

FUNCTIONAL DESCRIPTION

For ease of reading only the ETC 9420/9421/9422/9444/9445 are referenced. However, all such references apply equally to ETC 9320/9321/9322/9344/9345.

The internal architecture is shown in Figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" when it is reset, it is a logic "0".

Program memory

Program Memory consists of ROM, 1024 bytes for the ETC 9420/C 9421/ C 9422 and 2048 bytes for the ETC 9444/C 9445. These bytes of ROM may be program instructions, constants or ROM addressing data.

ROM addressing is accomplished by a 11-bit PC register which selects one of the 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value.

Three levels of subroutine nesting are implemented by a three level deep stack. Each subroutine call or interrupt pushes the next PC address into the stack. Each return pops the stack back into the PC register.

Data memory

Data memory consists of a 512-bit RAM for the ETC 9444/C 9445 organized as 8 data registers of 16 × 4-bit digits. RAM addressing is implemented by a 7-bit B register whose upper 3 bits (Br) select 1 of 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register.

Data memory consists of a 256-bit RAM for the ETC 9420/C 9421/C 9422, organized as 4 data registers of 16 × 4 bits digits. The B register is 6 bits long. Upper 2 bis (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with the A register (accumulator), they may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the immediate operand field of these instructions.

The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

Internal Logic

The processor contains its own 4-bit A register (accumulator) which is the source and destination register for most I/O, arithmetic, logic, and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch, to input 4 bits of a ROM word, L I/O ports data, to input 4-bit G, or IN ports, and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing the results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register in conjunction with the XAS instruction and the EN register, also serves to control the SK output.

The 8-bit T counter is a binary up counter which can be loaded to and from M and A using CAMT and CTMA instructions. This counter may be operated in two modes depending on a mask-programmable option : as a timer or as an external event counter. When the T counter overflows, an overflow flag will be set (see SKT and IT instructions below). The T counter is cleared on reset. A functional block diagram of the timer/ counter is illustrated in *Figure 10.a.*

Four general-purpose inputs, IN3-IN0, are provided. IN1, IN2 and IN3 may be selected, by a mask-programmable option as Read Strobe, Chip Select, and Write Strobe inputs, respectively, for use in MICROBUS application.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. In the dual clock mode. D0 latch controls the clock selection (see dual oscillator below).

The G register contents are outputs to a 4-bit general-purpose bidirectional I/O port. G0 may be mask-programmed as an output for MICROBUS applications.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are outputted to the L I/O ports when the L drivers are enabled under program control (see LEI instruction). With the MICROBUS® option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurence of a write strobe from the host CPU.

The **8 L drivers,** when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS® option allows L I/O port data to be latched into the Q register.

The SIO register functions as a 4-bit serial-in/serial-out shift register for MICROWIRE I/O and peripherals, or as a binary counter (depending on the contents of the EN register). Its contents can be exchanged with A.

The XAS Instruction copies C into the SKL Latch. In the counter mode, SK is the output of SKL ; in the shift register mode, SK is a sync clock, inhibited when SKL is a logic "0".

The "EN register is an internal 4-bit register loaded under programm control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

0. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or as a 4-bit binary counter. With EN_0 set, SIO is as asynchronous binary counter, DECREMENTING its value by one upon each low going pulse ("1" to "0") occuring on the SI input. Each pulse must be at least 2 (two) instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register, shifting left each instruction cycle time. The data present at SI is shifted into the least significant bit of SIO, SO can be enabled to output the most significant bit of SIO each instruction cycle time. The SK output SKL ANDed with the instruction cycle clock.

1. With EN_1 set interrupt is enabled. Immediatly following an interrupt, EN_1 is reset to disable further interrupts.
2. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high impedance input state.
3. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set(binary counter option selected), SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected, disables SO as the shift register output ; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0".

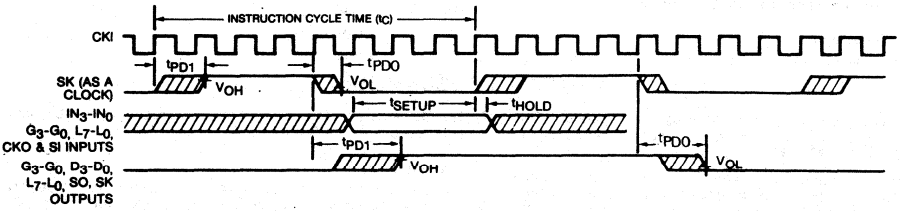


FIGURE 3 – INPUT/OUTPUT TIMING DIAGRAMS (Divide-by-8 Mode)

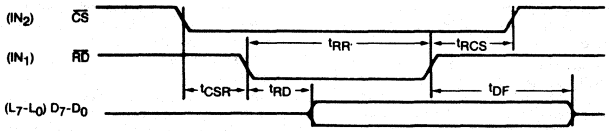


FIGURE 4 – MICROBUS READ OPERATION TIMING

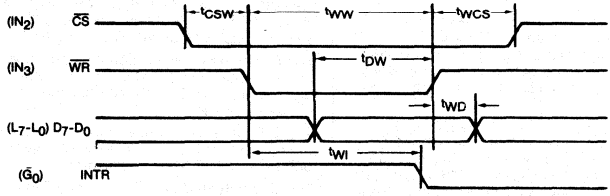


FIGURE 5 – MICROBUS WRITE OPERATION TIMING

FUNCTIONAL DESCRIPTION (continued)

TABLE 1 – ENABLE REGISTER MODES – BITS EN_0 AND EN_3

EN_0	EN_3	SIO	SI	SO	SK after XAS
0	0	Shift Register	Input to shift Register	0	If SKL = 1, SK = clock If SKL = 0, SK = 0
0	1	Shift Register	Input to Shift Register	Serial out	If SKL = 1, SK = clock If SKL = 0, SK = 0
1	0	Binary counter	Input to Counter	0	SK = SKL
1	1	Binary counter	Input to Counter	1	SK = SKL

Interrupt

The following features are associated with interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack. Any previous contents at the bottom of the stack are lost. The program counter is set to hex address OFF (the last word of page 3) and EN_1 is reset.

b. An interrupt will be acknowledged only after the following conditions are met :

1. EN_1 has been set.
2. A low-going pulse ("1" to "0") at least two instruction cycles wide occurs on the IN_1 input.
3. A currently executing instruction has been completed.
4. ALL successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon "popping" of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address OFF. At the end of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. **Subroutines should not be nested within the interrupt servicing routine** since their "popping" of the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The first instruction at hex address OFF must be a NOP.

e. A LEI instruction may be put immediately before the RET to re-enable interrupts.

MICROBUS interface

The ETC 9420/C 9444 has an option which allows it to be used as a peripheral microprocessor device, inputting and outputting data from to a host microprocessor (μP). IN_1, IN_2 and IN_3 general purposes input become **MICROBUS INTERFACE** read-strobe, chip-select, and write-strobe lines, respectively. IN_1 become $\overline{RD}$ — a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the μP. IN_2 becomes $\overline{CS}$ — a logic "0" on this line selects the ETC 9420/C 9444 as the uP peripheral device by enabling the operation of the $\overline{RD}$ and $\overline{WR}$ lines and allows for the selection of one of several peripheral components. IN_3 becomes $\overline{WR}$ — a logic "0" on this line will write bus data from the L ports to the Q latches for input to the ETC 9420/C 9444. G_0 becomes $\overline{INTR}$, a "ready" output, reset by a write pulse from the uP on the $\overline{WR}$ line, providing the "handshaking" capability necessary for asynchronous data transfer between the host CPU and the ETC 9420/C 9444.

This option has been designed for compatibility with MICROBUS a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS National Publication). The functioning and timing relationships between the signal lines affected by this option are as specified for the MICROBUS interface, and are given in the AC electrical characteristics and shown in the timing diagrams (figure 4 and 5). Connection of the ETC 9420/C 9444 to the MICROBUS is shown in figure 6.

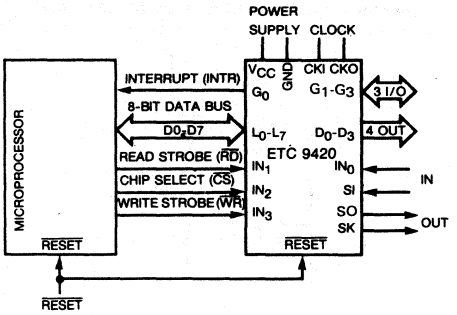
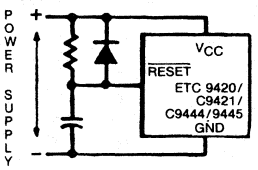


FIGURE 6 – MICROBUS® OPTION INTERCONNECT

Initialization

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 1 ms and if the operating frequency at CKI is greater than 32 kHz, otherwise the external RC network shown in Figure 7 must be connected to the $\overline{RESET}$ pin. The $\overline{RESET}$ pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{RESET}$ input, providing it stays low for at least three instruction cycle times.

NOTE : if CKI clock is less than 32 kHz, the internal reset logic (option = 29 = 1) must be disabled and the external RC circuit must be used.



RC ≥ 5 x Power Supply Rise Time and RC ≥ 100 x CKI period

FIGURE 7 – POWER-UP CIRCUIT

FUNCTIONAL DESCRIPTION (continued)

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, IL, T and G registers are cleared. The SKL Latch is set, this enabling SK as a clock output. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).

Timer

There are two modes selected by mask option :

a. Time-base counter. In this mode, the instruction cycle frequency generated from CKI passes through a 2-bit divide-by-4 prescaler. The output of this prescaler increments the 8-bit T counter thus providing a 10-bit timer. The prescaler is cleared during execution of a CAMT instruction and on reset.

   For example, using a 4 MHz crystal with a divide-by-16 option, the instruction cycle frequency of 250 kHz increments the 10-bit timer every 4 µs. By presetting the counter and detecting overflow, accurate timeouts between 16 µs (4 counts) and 4.096 ms (1024 counts) are possible. Longer timeouts can be achieved by accumulating, under software control, multiple overflows.

b. External event counter. In this mode, a low-going pulse ("1" to "0") at least 2 instruction cycles wide on the IN2 input will increment the 8-bit T counter.

Note : The IT instruction is not allowed in this mode.

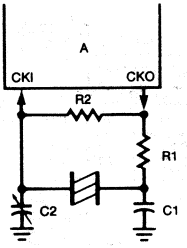
Halt mode

The ETC 9420/9421/C 9422/C 9444/C 9445 is a FULLY STATIC circuit ; therefore, the user may stop the system oscillator at any time to halt the chip. The chip may be also halted by the HALT instruction or by forcing CKO high when it is used as an HALT/I/O port. Once in the HALT mode, the internal circuitry does not receive any clocksignal, and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The chip may be awakened by one of the two different methods.

1. Continue function — by forcing CKO low, if it is mask-programmed as an HALT I/O port, the system clock is reenabled and the circuit continues to operate from the point where it was stopped.
2. Restart — by forcing the $\overline{\text{RESET}}$ pin low (see initialization).

The HALT mode is the mininum power dissipation state.

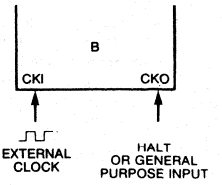
NOTE : If the user has selected dual clock with DO as external oscillator (option 30=2) AND the ETC 9444/C 9420 is running with the DO clock, the HALT mode — either hardware or software — will NOT be entered. Thus, the user should switch to the CKI clock to HALT. Alternatively, the user may stop the DO clock to minimize power.

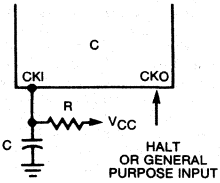


R/C controlled Oscillator

R	C	Cycle time	V_{CC}
15 k	82 pF	4 to 9 µs	≥ 4.5 V
30 k	82 pF	8 to 16 µs	≥ 4.5 V
60 k	100 pF	16 to 32 µs	2.4 to 4.5 V

Note : 15 k ≤ R ≤ 150 k ; 50 pF ≤ C ≤ 150 pF





Crystal or resonator

Crystal value	Component Values			
	R1	R2	C1 (pF)	C2 (pF)
32 kHz	220 k	20 M	30	6-36
455 kHz	5 k	10 M	80	40
2.086 MHz	2 k	1 M	30	6-36
4.0 MHz	1 k	1 M	30	6-36

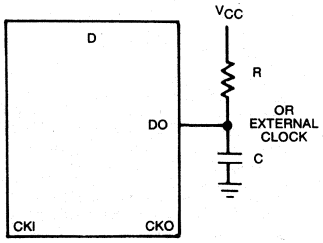


FIGURE 8 – OSCILLATOR COMPONENTS VALUES

This circuit and these values are for indication only. As the oscillator characteristics are not guaranteed, please consider and examine the circuit constants carefully on your application.

FUNCTIONAL DESCRIPTION (continued)

CKO Pin Options

a. Two-pin oscillator — (Crystal). See *Figure 9A*.

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. The HALT mode may be entered by program control (HALT instruction) which forces CKO high, thus inhibiting the crystal network. The circuit can be awakened only by forcing the RESET pin to a logic "0" (restart).

b. One-pin oscillator — (RC or external). See *Figure 9B*.

If a one-pin oscillator system is chosen, two options are available for CKO :

- CKO can be selected as the HALT I/O port. In that case, it is an I/O flip-flop which is an indicator of the HALT status. An external signal can over-ride this pin to start and stop the chip. By forcing a high level to CKO, the chip will stop as soon as CKI is high and CKO output will stay high to keep the chip stopped if the external driver returns to high impedance state.

  By forcing a low level to CKO, the chip will continue and CKO will stay low.

- As another option, CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction.

Oscillator options

There are four basic clock oscillator configuration available as shown by *Figure 8*.

a. Cyrstal Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency optionally divided by 4, 8 or 16.

b. External Oscillator. The external frequency is optionally divided by 4, 8 or 16 to give the instruction cycle time. CKO is the HALT I/O port or a general purpose input.

c. RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is the HALT I/O port or a general purpose input.

d. Dual oscillator. By selecting the dual clock option, pin D0 is now a single pin oscillator input. Two configurations are available : RC controlled Schmitt trigger oscillator or external oscillator.

The user may software select between the D0 oscillator (in that case, the instruction cycle time equals the D0 oscillation frequency divided by 4) by setting the D0 latch high or the CKI (CKO) oscillator by resetting D0 Latch low. Note that even in dual clock mode, the counter, if mask-programmed as a time-base counter, is always connected to the CKI oscillator.

For example, the user may connect up to a 1 MHz RC circuit to D0 for faster processing and a 32 kHz watch crystal to CKI and CKO for minimum current drain and time keeping.

Note : CTMA instructions is not allowed when chip is running from D0 clock.

Figures 10A and *10B* show the clock and timer diagrams with and without Dual clock.

ETC 9445/C 9421 24-Pin package option

If the ETC 9444/C 9420 is bonded in a 24-pin pckage, it becomes the ETC 9445/C 9421 illustrated in *Figure 2*, Connection diagrams. Note that the ETC 9445/C 9421 does not contain the four general purpose IN inputs (IN_3-IN_0). Use of this option precludes, ocourse, use of th IN optons, interrupt feature, external event counter feature, and the MICROBUS option which uses IN_1-IN_3. All other options are available for the ETC 9445/C 9421.

Note : If user selects 24-pin package, options 9, 10, 19 and 20 must be selected as a "0" (load to V_{CC} on the IN intputs). See option list.

BLOCK DIAGRAMS

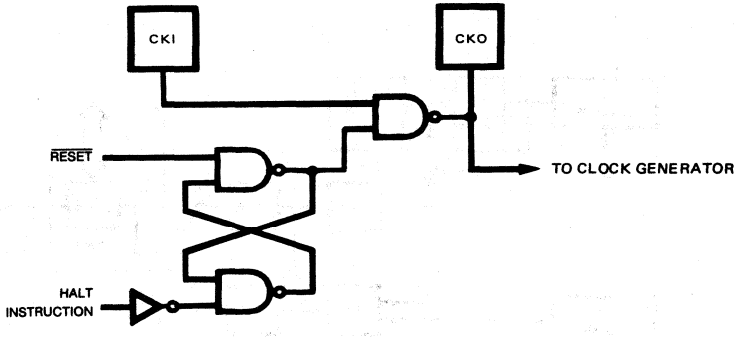


FIGURE 9 A – HALT MODE - TWO-PIN OSCILLATOR

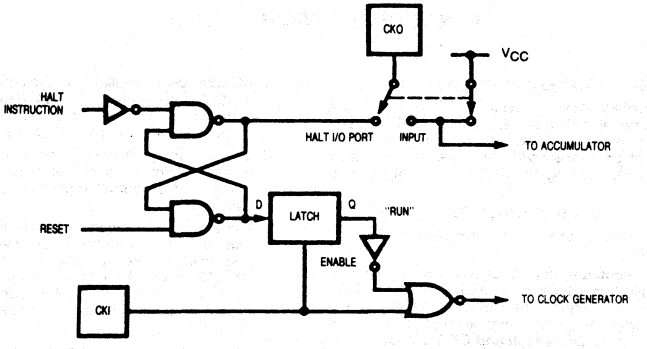


FIGURE 9 B – HALT MODE - ONE PIN OSCILLATOR

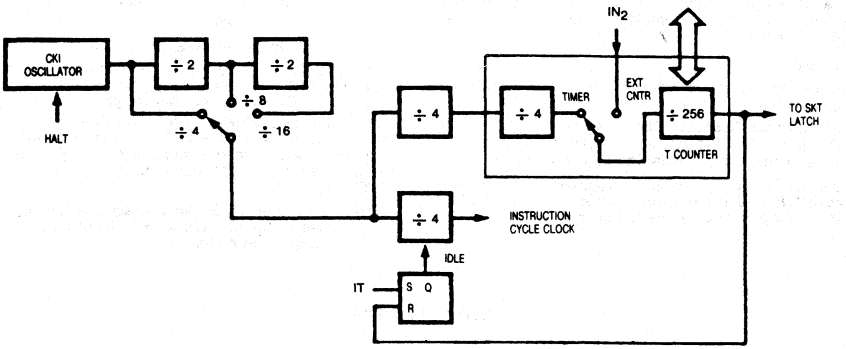


FIGURE 10 A – CLOCK AND TIMER BLOCK DIAGRAM WITHOUT DUAL-CLOCK

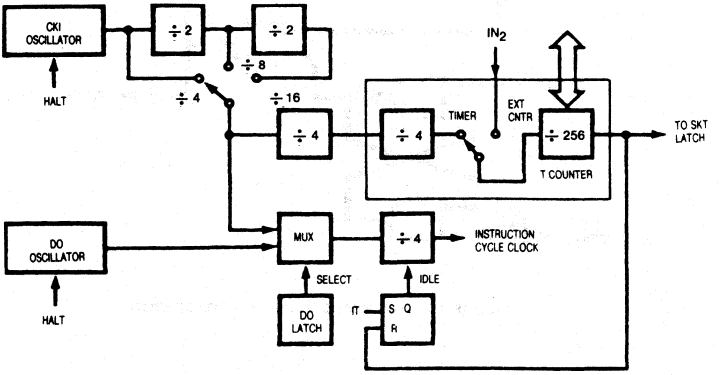


FIGURE 10 B – CLOCK AND TIMER BLOCK DIAGRAM WITH DUAL-CLOCK

INSTRUCTION SET

Table 2 is a symbol table providing internal architecture, instruction operand and operation symbols used in the instruction set table.

Table 3 provides the mnemonic, operand, machine code data flow, skip conditions and description of each instruction.

TABLE 2 – INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition
Internal Architecture Symbols	
A	4-bit Accumulator
B	7-bit RAM address register (6-bit for ETC 9420)
Br	Upper 3 bits of B (register address) (2-bit for ETC 9420)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry register
D	4-bit Data output port
EN	4-bit Enable register
G	4-bit General purpose I/O port
IL	Two 1-bit (IN_0 and IN_3) latches
IN	4-bit input port
L	8-bit TRI-STATE I/Oport
M	4-bit contents of RAM addressed by B
PC	11-bit ROM address program counter
Q	8-bit latch for L port
SA, SB, SC	11-bit 3-level subroutine stack
SIO	4 bit Shift register and counter
SK	Logic-controlled clock output
SKL	1-bit lach for SK output
T	8-bit timer

Instruction operand symbols	
d	4-bit operand field, 0-15 binary (RAM digit select)
r	3(2)-bit operand field, 0-7(3)binary (RAM register select)
a	11-bit operand field, 0-2047 (1023)
y	4-bit Operand field, 0-15 (immediate data)
RAM(x)	RAM addressed by variable x
ROM(x)	ROM addressed by variable x

Operational Symbols	
+	Plus
—	Minus
→	Replaces
↔	is exchanged with
=	is equal to
$\overline{A}$	one's complement of A
⊕	exclusive-or
:	range of values

TABLE 3 – ETC9444/C 9420 INSTRUCTION SET

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0 0 1 1 | 0 0 0 0	A + C + RAM(B) → A Carry → C	Carry	Add with CARRY. Skip on Carry
ADD		31	0 0 1 1 | 0 0 0 1	A + RAM(B) → A	None	Add RAM to A
ADT		4A	0 1 0 0 | 1 0 1 0	$A + 10_{10} \rightarrow A$	None	Add TEN TO A
AISC	y	5—	0 1 0 1 | y	A + y → A	Carry	Add Immediate Skip on Carry(y ≠ 0)
CASC		10	0 0 0 1 | 0 0 0 0	$\overline{A}$ + RAM(B) + C → A Carry → C	Carry	Complement and Add with Carry. Skip on Carry
CLRA		00	0 0 0 0 | 0 0 0 0	0 → A	None	Clear A
COMP		40	0 1 0 0 | 0 0 0 0	$\overline{A}$ → A	None	Ones complement of A to A
NOP		44	0 1 0 0 | 0 1 0 0	None	None	No Operation
RC		32	0 0 1 1 | 0 0 1 0	0 → C	none	Reset C
SC		22	0 0 1 0 | 0 0 1 0	1 → C	None	Set C
XOR		02	0 0 0 0 | 0 0 1 0	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A

INSTRUCTION SET (continued)

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1 1 1 1 | 1 1 1 1	ROM($PC_{10:8}$A,M) → $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6 -	0 1 1 0 | 0 | $a_{10:8}$	a → PC	None	Jump
		- -	$a_{7:0}$			
JP	a	- -	1 | $a_{6:0}$ (pages 2, 3, only)	a → $PC_{6:0}$	None	Jump within Page (Note 4)
			or			
		- -	1 1 | $a_{5:0}$ (all other pages)	a → $PC_{5:0}$		
JSRP	a	- -	1 0 | $a_{5:0}$	PC + 1 → SA → SB → SC	None	Jump to Subroutine Page
				00010 → $PC_{10:6}$		(Note 5)
				a → $PC_{5:0}$		
JSR	a	6 -	0 1 1 0 | 1 | $a_{10:8}$	PC + 1 → SA → SB → SC	None	Jump to Subroutine
			$a_{7:0}$	a → PC		
RET		48	0 1 0 0 | 1 0 0 0	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0 1 0 0 | 1 0 0 1	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33	0 0 1 1 | 0 0 1 1		None	HALT processor
		38	0 0 1 1 | 1 0 0 0			
IT		33	0 0 1 1 | 0 0 1 1			IDLE till timer
		39	0 0 1 1 | 1 0 0 1		None	Overflows then continues
MEMORY REFERENCE INSTRUCTIONS						
CAMT		33	0 0 1 1 | 0 0 1 1	A → $T_{7:4}$		
		3F	0 0 1 1 | 1 1 1 1	RAM(B) → $T_{3:0}$	None	Copy A, RAM to T
CTMA		33	0 0 1 1 | 0 0 1 1	$T_{7:4}$ → RAM(B)		
		2F	0 0 1 0 | 1 1 1 1	$T_{3:0}$ → A	None	Copy T to RAM, A (Note 9)
CAMQ		33	0 0 1 1 | 0 0 1 1	A → $Q_{7:4}$	None	Copy A, RAM to Q
		3C	0 0 1 1 | 1 1 0 0	RAM(B) → $Q_{3:0}$		
CQMA		33	0 0 1 1 | 0 0 1 1	$Q_{7:4}$ → RAM(B)	None	Copy Q to RAM, A
		2C	0 0 1 0 1 1 0 0	$Q_{3:0}$ → A		
LD	r	- 5	0 0 | r | 0 1 0 1	RAM(B) → A	None	Load RAM into A
			(r = 0 3)	Br ⊙ r → Br		Exclusive-OR Br with r
LDD	r d	23	0 0 1 0 | 0 0 1 1	RAM(r d) → A	None	Load A with RAM pointed
			0 | r | d			to directly by r d
LQID		BF	1 0 1 1 | 1 1 1 1	ROM($PC_{10:8}$ A M) → Q	None	Load Q Indirect (Note 3)
RMB	0	40	0 1 0 0 | 1 1 0 0	0 - $RAM(B)_0$	None	Reset RAM Bit
	1	45	0 1 0 0 | 0 1 0 1	0 - $RAM(B)_1$		
	2	42	0 1 0 0 | 0 0 1 0	0 - $RAM(B)_2$		
	3	43	0 1 0 0 | 0 0 1 1	0 - $RAM(B)_3$		

INSTRUCTION SET (continued)

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
SMB	0	4D	0 1 0 0 1 1 0 1	1 → RAM(B)$_0$	None	Set RAM Bit
	1	47	0 1 0 0 0 1 1 1	1 → RAM(B)$_1$		
	2	46	0 1 0 0 0 1 1 0	1 → RAM(B)$_2$		
	3	4B	0 1 0 0 1 0 1 1	1 → RAM(B)$_3$		
STII	y	7 -	0 1 1 1 y	y → RAM(B) Bd ⊕ 1 → Bd	None	Store Memory Immediate and increment Bd
X	r	- 6	0 0 r 0 1 1 0 (r = 0:3)	RAM(B) ↔ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23	0 0 1 0 0 0 1 1 -- 1 r d	RAM(r,d) ↔ A	None	Exchange A with RAM pointed to directly by r, d
XDS	r	- 7	0 0 r 0 1 1 1 (r = 0:3)	RAM(B) ↔ A Bd — 1 → Bd Br ⊕ → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd Exclusive-Or Br with r
XIS	r	- 4	0 0 r 0 1 0 0 (r = 0:3)	RAM(B) ↔ A Bd + 1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-Or Br with r

REGISTER REFERENCE INSTRUCTIONS

CAB		50	0 1 0 1 0 0 0 0	A → Bd	None	Copy A to Bd
CBA		4E	0 1 0 0 1 1 1 0	Bd → A	None	Copy Bd to A
LBI	r,d	- -	0 0 r (d-1) (r = 0:3) (d = 0,9:15) or 33 0 0 1 1 0 0 1 1 - - 1 r d (any r, any d)	r,d → B	Skip until not a LBI	Load B immediate with r,d (Note 6)
LEI	y	33	0 0 1 1 0 0 1 1	y → EN	None	Load EN Immediate (Note 7)
		6 -	0 1 1 0 y			
XABR		12	0 0 0 1 0 0 1 0	A ↔ Br	None	Exchange A with Br (Note 8)

TEST INSTRUCTIONS

SKC		20	0 0 1 0 0 0 0 0		C = 1	Skip if C is True
SKE		21	0 0 1 0 0 0 0 1		A = RAM(B)	Skip if A Equals RAM
SKGZ		33	0 0 1 1 0 0 1 1		$G_{3:0}$ = 0	Skip if G is Zero
		21	0 0 1 0 0 0 0 1			(all 4 bits)
SKGBZ		33	0 0 1 1 0 0 1 1	1st byte		Skip if G Bit is Zero
	0	01	0 0 0 0 0 0 0 1	2nd byte	G_0 = 0	
	1	11	0 0 0 1 0 0 0 1		G_1 = 0	
	2	03	0 0 0 0 0 0 1 1		G_2 = 0	
	3	13	0 0 0 1 0 0 1 1		G_3 = 0	

INSTRUCTION SET (continued)

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
SKMBZ	0	01	0 0 0 0 | 0 0 0 1		$RAM(B)_0 = 0$	Skip if RAM Bit is Zero
	1	11	0 0 0 1 | 0 0 0 1		$RAM(B)_1 = 0$	
	2	03	0 0 0 0 | 0 0 1 1		$RAM(B)_2 = 0$	
	3	13	0 0 0 1 | 0 0 1 1		$RAM(B)_3 = 0$	
SKT		41	0 1 0 0 | 0 0 0 1		A time-base counter carry has occured since last test	Skip on Timer (Note 3)
INPUT/OUTPUT INSTRUCTIONS						
ING		33	0 0 1 1 | 0 0 1 1	G → A	None	Input G Ports to A
		2A	0 0 1 0 | 1 0 1 0			
ININ		33	0 0 1 1 | 0 0 1 1	IN → A	None	Input IN inputs to A
		28	0 0 1 0 | 1 0 0 0			(Note 2)
INIL		33	0 0 1 1 | 0 0 1 1	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A
		29	0 0 1 0 | 1 0 0 1			(Note 3)
INL		33	0 0 1 1 | 0 0 1 1	$L_{7:4}$ → RAM(B)	None	Input L Ports to RAM, A
		2E	0 0 1 0 | 1 1 1 0	$L_{3:0}$ → A		
OBD		33	0 0 1 1 | 0 0 1 1	Bd → D	None	Output Bd to D Outputs
		3E	0 0 1 1 | 1 1 1 0			
OGI	y	33	0 0 1 1 | 0 0 1 1	y → G	None	Output to G Ports
		5 -	0 1 0 1 | y			Immediate
OMG		33	0 0 1 1 | 0 0 1 1	RAM(B) → G	None	Output RAM to G Ports
		3A	0 0 1 1 | 1 0 1 0			
XAS		4F	0 1 0 0 | 1 1 1 1	A ↔ SIO C → SKL	None	Exchange A with SIO
						(Note 3)

Note 1 : All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2 : The ININ instruction is not available on the 24-pin packages since these devices do not contain the IN inputs.

Note 3 : For additional on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4 : The JP instruction allows a jump, while in subroutine page 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5 : A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6 : LBI is a single-byte instruction if d=0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the "d" data minus 1, e.g., to load the lower four bits of B (Bd) with the value 9(1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 7 : Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register)

Note 8 : For 2K ROM devices. A ↔ Br (0 → A3). For 1K ROM devices. A ↔ Br (0,0 → A3, A2).

Note 9 : Do not use CTMA instruction when dual - option is selected and part is running from D0 Clocks.

DESCRIPTION OF SELECTED INSTRUCTIONS

Xas Instruction

XAS (Exchange A with SIO) copies C to the SKL latch and exchanges the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. If SIO is selected as a shift register, an XAS instruction can be performed once every 4 instruction cycles to effect a continuous data stream.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC10:PC8,A,M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB → SC) and replaces the least significant 8 bits of the PC as follows : A → PC(7:4), RAM(B) → PC(3:0), leaving PC(10), PC(9) and PC(8) unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program excecution. Since LQID pushes SB → SC, the previous contents of SC are lost.

Note : LQID uses 2 instruction cycles if executed, one if skipped.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 11-bit word, PC10:8,A,M. PC10, PC9 and PC8 are not affected by JID.

Note : JID uses 2 instruction cycles if executed, one if skipped.

SKT Instruction

The SKT (Skip On Timer) instruction tests the state of the T counter overflow latch (see internal logic, above), executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction allow the processor to generate its own time-base for real-time processing, rather than relying on an external input signal.

Note : If the most significant bit of the T counter is a 1 when a CAMT instruction loads the counter, the overflow flag will be set. The following sample of codes should be used when loading the counter :

```
CAMT ; load T counter
SKT  : skip if overflow flag is set and reset it
NOP
```

IT Instruction

The IT (idle till timer) instruction halts the processor and puts it in an idle state until the time-base counter overflows. Upon overflow, the processor will restart with a delay shorter than one cycle time. This idle state reduces current drain since all logic (except the oscillator and time base counter) is stopped. IT instruction is not allowed if the T counter is mask-programmed as an external event counter (option ≠ 31 = 1).

INIL Instruction

INIL (Input IL Latches to A) inputs 2 latches, IL3 and IL0, CKO and 0 into A. The IL3 and IL0 latches are set if a low-going pulse ("1" to "0") has occured on the IN3 and IN0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction cycles. Execution of an INIL inputs IL3 and IL0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN3 and IN0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO INTO A2. If CKO has not been so programmed, a "1" will be placed in A2. A 0 is input into A1. IL latches are cleared on reset. IL latches are not available on the ETC 9445/C 9421.

Instruction set notes

a. The first word of a program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, they are still fetched from the program memory. Thus program paths take the same number of cycles whether instructions are skipped or executed except for JID, and LQID.

c. The ROM is organized into pages of 64 words each. The Program Counter is a 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID is the last word of a page, it operates as if it were in the next page. For example : a JP Located in the last word of a page will jump to a location in the next page. Also, a JID or LQID located in the last word of every fourth page (i.e. hex address 0FF, 1FF, 2FF, 3FF, 4FF, etc.) will access data in the next group of four pages.

Note : The ETC 9420/C 9421/C 9422 needs only 10 bits to address its ROM. Therefore, the eleventh bit (10) is ignored.

POWER DISSIPATION

The lowest power drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to insure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. A crystal or resonator generated clock input will draw additional current. For example, a 500 kHz crystal input will typical draw 100 µA more than a square-wave input. An R/C oscillator will draw even more current since the input is a slow rising signal.

If using an external squarewave oscillator, the following equation can be used to calculate the ETC 9444/C 9445 operating current drain.

$$I_{CO} = I_Q + V \times 40 \times Fi + V \times 1400 \times Fi/Dv$$

where I_{CO} = chip operating current drain in microamps
I_Q = quiescent leakage current (from curve)
Fi = CKI frequency in MegaHertz
V = chip V_{CC} in volts
Dv = divide by option selected.

For example at 5 volts V_{CC} and 400 kHz (divide by 4)
$I_{CO} = 20 + 5 \times 40 \times 0.4 + 5 \times 1400 \times 0.4/4$
$I_{CO} = 20 + 80 + 700 = 800\ \mu A$

At 2.4 volts V_{CC} and 30 kHz (divide by 4)
$I_{CO} = 6 + 2.4 \times 40 \times 0.03 + 2.4 \times 1400 \times 0.03/4$
$I_{CO} = 6 + 2.88 + 25.2 = 34.08\ \mu A$

POWER DISSIPATION (continued)

If an IT instruction is executed, the chip goes into the IDLE mode until the timer overflows. In IDLE mode, the current drain can be calculated from the following equation :

$Ici = I_Q + V \times 40 \times Fi$

For example, at 5 volts V_{CC} and 400 kHz

$Ici = 20 + 5 \times 40 \times 0.4 = 100\ \mu A$

The total average current will then be the weighted average of the operation current and the idle current :

$$Ita = I_{CO} \times \frac{To}{To+Ti} + Ici \times \frac{Ti}{To+Ti}$$

where : Ita = total average current
I_{CO} = operating current
Ici = idle current
To = operating time
Ti = idle time

I/O options

ETC 9444/C 9445 outputs have the following optional configurations, illustrated in *Figure 11* :

a. Standard—A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL.

b. Low Current—This is the same configuration as a. above except that the sourcing current is much less.

c. Open Drain—An N-channel device to ground only, allowing external pull-up as required by the user's application.

d. Standard TRI-STATE L Ouput—A CMOS output buffer similar to a. witch may be disabled by program control.

e. Low-Current TRI-STATE L Output—This is the same as d. above except that the sourcing current is much less.

f. Open-Drain TRI-STATE L Output—This has the N-channel device to ground only.

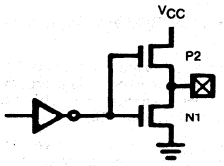
All inputs have the following options :

g. Input with on chip load device to V_{CC}.

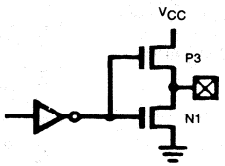
h. Hi-Z input which must be driven by the users logic.

When using either the G or L I/O ports as inputs, a pull-up device is necessary. This can be an external device or the following alternative is available : Select the low-current output option. Now, by setting the output registers to a logic "1" level, the P-channel devices will act as the pull-up load. Note that when using the L ports in this fashion the Q registers must be set to a logic "1" level and the L drivers MUST BE ENABLED by an LEI instruction (see description above).

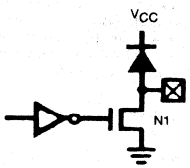
All output drivers use one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in *Figure 12* for each of these devices to allow the designer to effectively use these I/O configurations.



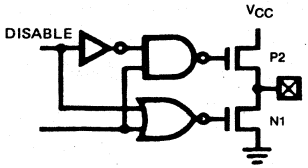
a. Standard Push-Pull Output



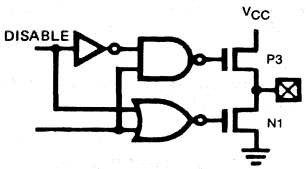
b. Low Current Push-Pull Output



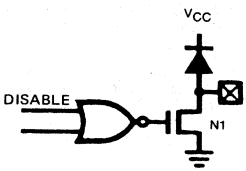
c. Open-Drain Output



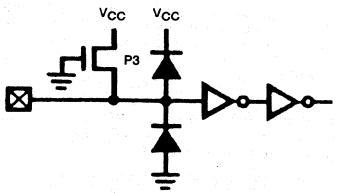
d. Standard TRI-STATE "L" Output



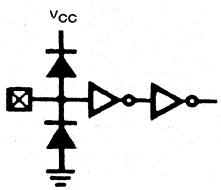
e. Low Current TRI-STATE "L" Output.



f. Open Drain TRI-STATE "L" Output



g. Input with Load



h. HI-Z Input

FIGURE 11 – INPUT/OUTPUT CONFIGURATIONS

POWER DISSIPATION (continued)

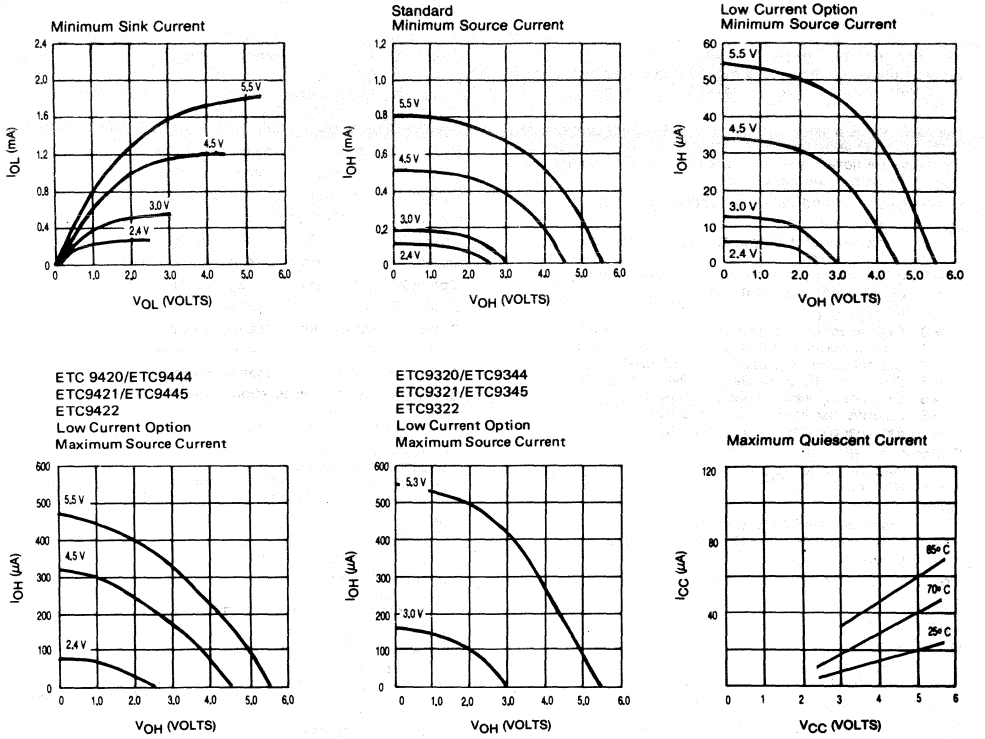


FIGURE 12 – INPUT/OUTPUT CHARACTERISTICS

OPTION LIST

The ETC 9444/C 9420/C 9445/C 9421/C 9422 mask-programmable options are assigned numbers which correspond with the ETC 9344/C 9320/C 9345/C 9321/C 9322 pins.

The following is a list of options. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0 : Ground Pin — no option available.

Option 2 : CKO Pin
- = 0 : clock generator output to crystal/resonator
- = 1 : HALT I/O port
- = 2 : general purpose input with load device to V_{CC}
- = 3 : general purpose input, high-Z

Option 3 : CKI input
- = 0 : Crystal controlled oscillator input divide by 4
- = 1 : Crystal controlled oscillator input divide by 8
- = 2 : Crystal controlled oscillator input divide by 16
- = 4 : Single-pin RC controlled oscillator (divide by 4)
- = 5 : External oscillator input divide by 4
- = 6 : External oscillator input divide by 8
- = 7 : External oscillator input divide by 16

Option 4 : $\overline{\text{RESET}}$ input
- = 0 : load device to V_{CC}
- = 1 : Hi-Z input

Option 5 : L7 Driver
- = 0 : Standard TRI-STATE push-pull output
- = 1 : Low-current TRI-STATE push-pull output
- = 2 : Open-drain TRI-STATE output

Option 6 : L6 Driver—(same as option 5)

Option 7 : L5 Driver—(same as option 5)

Option 8 : L4 Driver—(same as option 5)

Option 9 : IN1 input
- = 0 : load device to V_{CC}
- = 1 : Hi-Z input

Option 10 : IN2 input—(same as option 9)

Option 11 = 0 : V_{CC} Pin—no option available

Option 12 : L3 Driver—(same as option 5)

Option 13 : L2 Driver—(same as option 5)

Option 14 : L1 Driver—(same as option 5)

Option 15 : L0 Driver—(same as option 5)

Option 16 : Si Input — (same as option 9)

Option 17 : SO Driver
- = 0 : Standard push-pull output
- = 1 : Low-current push-pull output
- = 2 : Open-drain output

Option 18 : SK Driver — (same as option 17)

Option 19 : IN0 Input — (same as option 9)

Option 20 : IN3 Input — (same as option 9)

Option 21 : G0 I/O Port — (same as option 17)

Option 22 : G1 I/O Port — (same as option 17)

Option 23 : G2 I/O Port — (same as option 17)

Option 24 : G3 I/O Port — (same as option 17)

Option 25 : D3 Output — (same as option 17)

Option 26 : D2 Output — (same as option 17)

Option 27 : D1 Output — (same as option 17)

Option 28 : D0 Output — (same as option 17)

Option 29 : Internal Initialization Logic
- = 0 : Normal operation
- = 1 : No internal initialization logic

Option 30 : Dual Clock
- = 0 : Normal operation
- = 1 : Dual Clock. D0 RC oscillator
- = 2 : Dual Clock. D0 ext. clock input

} (opt. # 28 must = 2)

Option 31 : Timer
- = 0 : Time-base counter
- = 1 : External event counter

Option 32 : MICROBUS
- = 0 : Normal
- = 1 : MICROBUS (opt. # 31 must = 0)

Option 33 : Chip bonding
(1 K and 2 K Microcontroller)
- = 0 : 28 - pin package
- = 1 : 24 - pin package
- = 2 : Same die purchased in both 24 and 28 pin version
(1 K Microcontroller only)
- = 3 : 20 - pin package
- = 4 : 28- and 20- pin package
- = 5 : 24- and 20- pin package
- = 6 : 28-, 24- and 20- pin package

Note : - If opt # 33 = 2 then opt # 9, 10, 19, 20 and 32 must = 0
- If opt # 33 = 3, 4, 5 or 6 then opt # 9, 10, 19, 20, 21, 22, 30 and 32 must = 0

CROSS REFERENCE	
THOMSON SC	NS
ETC 9420	COP 424 C
ETC 9421	COP 425 C
ETC 9422	COP 426 C
ETC 9444	COP 444 C
ETC 9445	COP 445 C

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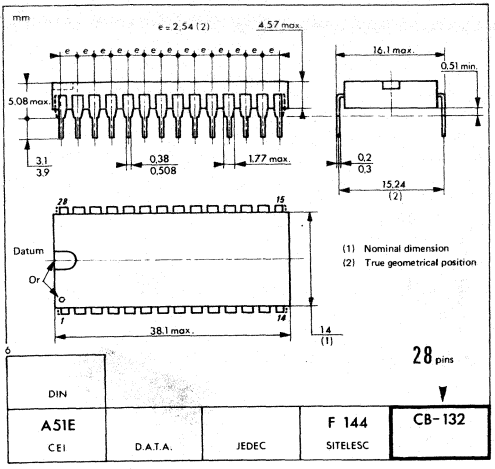
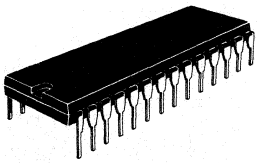
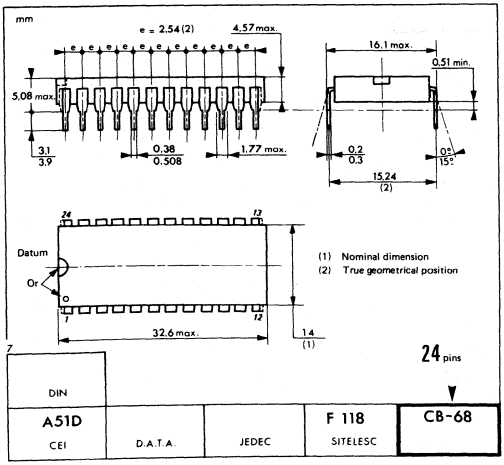
PHYSICAL DIMENSIONS



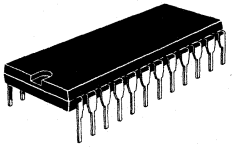
CB-132



N SUFFIX
PLASTIC PACKAGE

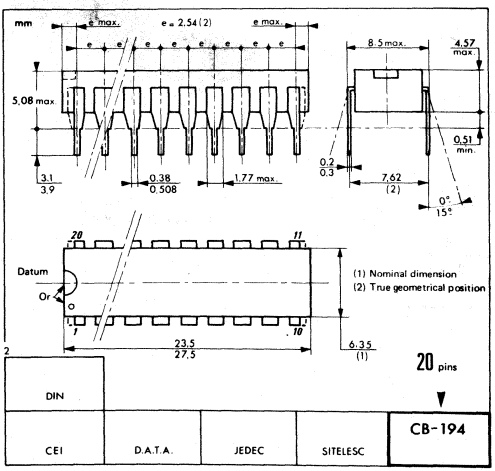


CB-68

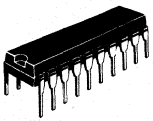


N SUFFIX
PLASTIC PACKAGE

PHYSICAL DIMENSIONS



CB-194



N SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

ETL9420/21/22 • ETL9320/21/22

SINGLE SHIP MICROCONTROLLERS

The ETL9420, ETL9421, ETL9422, ELT9320, ETL9321, and ETL9322 Single-Chip N-Channel Microcontrollers are fully compatible with the COPS® family, fabricated using N-channel, silicon gate XMOS technology. These controller oriented processors are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture, and I/O scheme designed to facilitate keyboard input, display output, and BCD data manipulation. The ETL9421 and ETL9422 are identical to the ETL9420, but with 19 and 15 I/O lines, respectively, instead of 23. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized controller oriented processor at a low end-product cost.

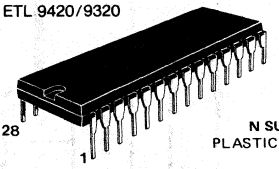
The ETL9320/L9321/L9322 are exact functional equivalents, but extended temperature range versions, of the ETL9420, ETL9421 and ETL9422 respectively.

- Low cost
- Powerful instruction set
- 1 K x 8 ROM, 64 x 4 RAM
- 23 I/O lines (ETL9420)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 16μs instruction time
- Single supply operation (4.5-6.3V)
- Low current drain (9mA max.)
- Internal time-base counter for real-time processing
- Internal binary counter register with MICROWIRE® compatible serial I/O
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS compatible in and out
- Direct drive of LED digit and segment lines
- Software/hardware compatible with other members of ET9400 family
- Extended temperature range device ETL9320/L9321/L9322 (−40°C to + 85°)
- Wider supply range (4.5V − 9.5V) optionally available

NMOS

SINGLE CHIP MICROCONTROLLERS

ETL 9420/9320



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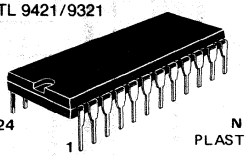
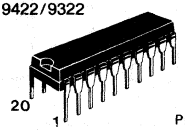
ETL 9421/9321



N SUFFIX
PLASTIC PACKAGE

ETL 9422/9322



N SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT

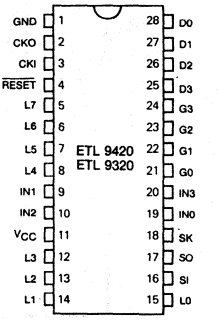


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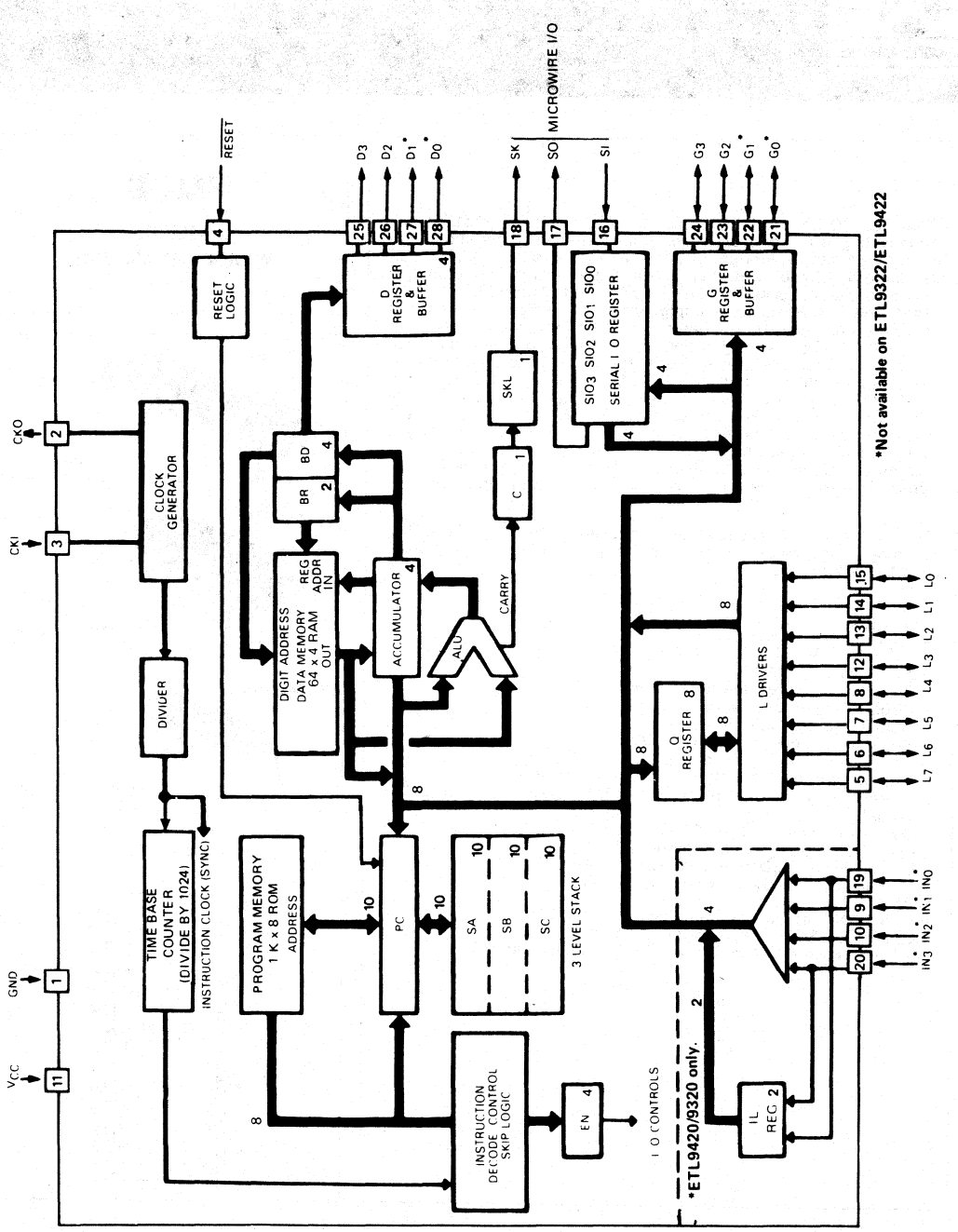
FIGURE 1 – BLOCK DIAGRAM (28-pin version)



ETL9420/L9421/L9422

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	
ETL9420/L9421	0.75 Watt at 25°C 0.4 Watt at 70°C
ETL9422	0.65 Watt at 25°C 0.3 Watt at 70°C
Total Source Current	120mA
Total Sink Current	120mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $0° \leqslant T_A \leqslant +70°C$, $4.5V \leqslant V_{CC} \leqslant 9.5V$ (Unless otherwise specified).

Parameter	Conditions	Min.	Max.	Units
Standard Operating Voltage (V_{CC})	Note 1	4.5	6.3	V
Optional Operating Voltage (V_{CC})		4.5	9.5	V
Power Supply Ripple	peak to peak	—	0.5	V
Operating Supply Current	all inputs and outputs open	—	9	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input (÷32, ÷16, ÷8)				
Logic High (V_{IH})		2.0	—	V
Logic Low (V_{IL})		−0.3	0.4	V
Schmitt Trigger Input (÷4)				
Logic High (V_{IH})		0.7 V_{CC}	—	V
Logic Low (V_{IL})		−0.3	0.6	V
$\overline{\text{RESET}}$ Input Levels	Schmitt Trigger Input			
Logic High		0.7 V_{CC}	—	V
Logic Low		−0.3	0.6	V
SO Input Level (Test mode)		2.0	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0	—	V
Logic High	with TTL trip level options	2.0	—	V
Logic Low	selected, $V_{CC} = 5V \pm 5\%$	−0.3	0.8	V
Logic High	with high trip level options	3.6	—	V
Logic Low	selected	−0.3	1.2	V
Input Capacitance		—	7	pF
Hi-Z Input Leakage		−1	+1	µA
Output Voltage Levels				
LSTTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High (V_{OH})	$I_{OH} = -25\mu A$	2.7	—	V
Logic Low (V_{OL})	$I_{OL} = 0.36mA$	—	0.4	V
CMOS Operation				
Logic High	$I_{OH} = -10\mu A$	$V_{CC} - 1$	—	V
Logic Low	$I_{OL} = +10\mu A$	—	0.2	V

Note 1 : V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

ETL9420/L9421/L9422

DC ELECTRICAL CHARACTERISTICS (continued) $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 9.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	$V_{CC} = 9.5V$, $V_{OL} = 0.4V$	1.8	—	mA
	$V_{CC} = 6.3V$, $V_{OL} = 0.4V$	1.2	—	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.9	—	mA
L_0-L_7 Outputs and Standard G_0-G_3, D_0-D_3 Outputs (I_{OL})	$V_{CC} = 9.5V$, $V_{OL} = 0.4V$	0.8	—	mA
	$V_{CC} = 6.3V$, $V_{OL} = 0.4V$	0.5	—	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.4	—	mA
G_0-G_3 and D_0-D_3 Outputs with High Current Options (I_{OL})	$V_{CC} = 9.5V$, $V_{OL} = 1.0V$	15	—	mA
	$V_{CC} = 6.3V$, $V_{OL} = 1.0V$	11	—	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	7.5	—	mA
G_0-G_3 and D_0-D_3 Outputs with Very High Current Options (I_{OL})	$V_{CC} = 9.5V$, $V_{OL} = 1.0V$	30	—	mA
	$V_{CC} = 6.3V$, $V_{OL} = 1.0V$	22	—	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	15	—	mA
CKI (Single-pin RC oscillator)	$V_{CC} = 4.5V$, $V_{IH} = 3.5V$	2	—	mA
CKO	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.2	—	mA
Output Source Current				
Standard Configuration, All Outputs (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	-140	-800	µA
	$V_{CC} = 6.3V$, $V_{OH} = 2.0V$	-75	-480	µA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	-30	-250	µA
Push-Pull Configuration SO and SK Outputs (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 4.75V$	-1.4	—	mA
	$V_{CC} = 6.3V$, $V_{OH} = 2.4V$	-1.4	—	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.0V$	-1.2	—	mA
LED Configuration, L_0-L_7 Outputs, Low Current Driver Option (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	-1.5	-18	mA
	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	-1.5	-13	mA
LED Configuration, L_0-L_7 Outputs, High Current Driver Option (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	-3.0	-35	mA
	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	-3.0	-25	mA
TRI-STATE® Configuration, L_0-L_7 Outputs, Low Current Driver Option (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 5.5V$	-0.75	—	mA
	$V_{CC} = 6.3V$, $V_{OH} = 3.2V$	-0.8	—	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	-0.9	—	mA
TRI-STATE® Configuration, L_0-L_7 Outputs, High Current Driver Option (I_{OH})	$V_{CC} = 9.5V$, $V_{OH} = 5.5V$	-1.5	—	mA
	$V_{CC} = 6.3V$, $V_{OH} = 3.2V$	-1.6	—	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	-1.8	—	mA
Input Load Source Current	$V_{CC} = 5.0V$, $V_{IL} = 0V$	-10	-140	µA
CKO Output				
RAM Power Supply Option Power Requirement	$V_R = 3.3V$	—	3.0	mA
TRI-STATE® Output Leakage Current		-2.5	+2.5	µA
Total Sink Current Allowed				
All Outputs Combined		—	120	mA
D, G Ports		—	120	mA
L_7-L_4		—	4	mA
L_3-L_0		—	4	mA
All Other Pins		—	1.5	mA
Total Source Current Allowed				
All I/O Combined		—	120	mA
L_7-L_4		—	60	mA
L_3-L_0		—	60	mA
Each L Pin		—	30	mA
All Other Pins		—	1.5	mA

ETL9320/L9321/L9322

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	−40°C to +85°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	
ETL9320, L9321	0.75 Watt at 25°C 0.4 Watt at 85°C
ETL9322	0.65 Watt at 25°C 0.20 Watt at 85°C
Total Source Current	120mA
Total Sink Current	120mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS – $40°C \leq T_A \leq +85°C$, $4.5V \leq V_{CC} \leq 7.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Standard Operating Voltage (V_{CC})	Note 1	4.5	5.5	V
Optional Operating Voltage (V_{CC})		4.5	7.5	V
Power Supply Ripple	peak to peak	—	0.5	V
Operating Supply Current	all inputs and outputs open	—	11	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (V_{IH})		2.2	—	V
Logic Low (V_{IL})		−0.3	0.3	V
Schmitt Trigger Input				
Logic High (V_{IH})		$0.7V_{CC}$	—	V
Logic Low (V_{IL})		−0.3	0.4	V
$\overline{RESET}$ Input Levels	Schmitt Trigger Input			
Logic High		$0.7V_{CC}$	—	V
Logic Low		−0.3	0.4	V
SO Input Level (Test mode)		2.2	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0	—	V
Logic High	with TTL trip level options	2.2	—	V
Logic Low	selected, $V_{CC} = 5V \pm 5\%$	−0.3	0.6	V
Logic High	with high trip level options	3.6	—	V
Logic Low	selected	−0.3	1.2	V
Input Capacitance		—	7	pF
Hi-Z Input Leakage		−2	+2	µA
Output Voltage Levels				
LSTTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High (V_{OH})	$I_{OH} = -20\mu A$	2.7	—	V
Logic Low (V_{OL})	$I_{OL} = 0.36mA$	—	0.4	V
CMOS Operation				
Logic High	$I_{OH} = -10\mu A$	$V_{CC} - 1$	—	V
Logic Low	$I_{OL} = +10\mu A$	—	0.2	V

Note 1 : V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

ETL9320/L9321/L9322

DC ELECTRICAL CHARACTERISTICS (continued – $40°C \leq T_A \leq +85°C$, $4.5V \leq V_{CC} \leq 7.5V$ (Unless otherwise specified).

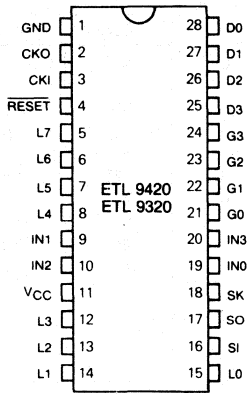
Parameter	Conditions	Min.	Max.	Units
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	$V_{CC} = 7.5V$, $V_{OL} = 0.4V$	1.4	—	mA
	$V_{CC} = 5.5V$, $V_{OL} = 0.4V$	1.0	—	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.8	—	mA
L_0-L_7 Outputs and Standard G_0-G_3, D_0-D_3 Outputs (I_{OL})	$V_{CC} = 7.5V$, $V_{OL} = 0.4V$	0.6	—	mA
	$V_{CC} = 5.5V$, $V_{OL} = 0.4V$	0.5	—	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.4	—	mA
G_0-G_3 and D_0-D_3 Outputs with High Current Options (I_{OL})	$V_{CC} = 7.5V$, $V_{OL} = 1.0V$	12	—	mA
	$V_{CC} = 5.5V$, $V_{OL} = 1.0V$	9	—	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	7	—	mA
G_0-G_3 and D_0-D_3 Outputs with Very High Current Options (I_{OL})	$V_{CC} = 7.5V$, $V_{OL} = 1.0V$	24	—	mA
	$V_{CC} = 5.5V$, $V_{OL} = 1.0V$	18	—	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	14	—	mA
CKI (Single-pin RC oscillator)	$V_{CC} = 4.5V$, $V_{IH} = 3.5V$	2	—	mA
CKO	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.2	—	mA
Output Source Current				
Standard Configuration, All Outputs (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	-100	-900	µA
	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	-55	-600	µA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	-28	-350	µA
Push-Pull Configuration SO and SK Outputs (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 3.75V$	-0.85	—	mA
	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	-1.1	—	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.0V$	-1.2	—	mA
LED Configuration, L_0-L_7 Outputs, Low Current Driver Option (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	-1.4	-27	mA
	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	-1.4	-17	mA
	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	-0.7	-15	mA
LED Configuration, L_0-L_7 Outputs, High Current Driver Option (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	-2.7	-54	mA
	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	-2.7	-34	mA
	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	-1.4	-30	mA
TRI-STATE® Configuration, L_0-L_7 Outputs, Low Current Driver Option (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 4.0V$	-0.7	—	mA
	$V_{CC} = 5.5V$, $V_{OH} = 2.7V$	-0.6	—	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	-0.9	—	mA
TRI-STATE® Configuration, L_0-L_7 Outputs, High Current Driver Option (I_{OH})	$V_{CC} = 7.5V$, $V_{OH} = 4.0V$	-1.4	—	mA
	$V_{CC} = 5.5V$, $V_{OH} = 2.7V$	-1.2	—	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	-1.8	—	mA
Input Load Source Current	$V_{CC} = 5.0V$, $V_{IL} = 0V$	-10	-200	µA
CKO Output RAM Power Supply Option Power Requirement	$V_R = 3.3V$	—	4.0	mA
TRI-STATE® Output Leakage Current		-5	+5	µA
Total Sink Current Allowed				
All Outputs Combined		—	120	mA
D, G Ports		—	120	mA
L_7-L_4		—	4	mA
L_3-L_0		—	4	mA
All Other Pins		—	1.5	mA
Total Source Current Allowed				
All I/O Combined		—	120	mA
L_7-L_4		—	60	mA
L_3-L_0		—	60	mA
Each L Pin		—	30	mA
All Other Pins		—	1.5	mA

AC ELECTRICAL CHARACTERISTICS

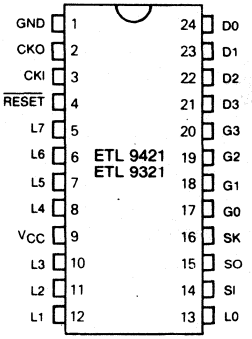
ETL9420/L9421/L9422 : 0°C $\leq T_A \leq$ +70°C, 4.5V $\leq V_{CC} \leq$ 9.5V (Unless otherwise specified)
ETL9320/L9321/L9322 : −40°C $\leq T_A \leq$ +85°C, 4.5V $\leq V_{CC} \leq$ 7.5V (Unless otherwise specified).

Parameter	Conditions	Min.	Max.	Units
Instruction Cycle Time — t_C		16	40	µs
CKI				
Input Frequency — f_I	÷32 mode	0.8	2.0	MHz
	÷16 mode	0.4	1.0	MHz
	÷8 mode	0.2	0.5	MHz
	÷4 mode	0.1	0.25	MHz
Duty Cycle		30	60	%
Rise Time	f_I = 2 MHz	—	120	ns
Fall Time		—	80	ns
CKI Using RC (÷4)	R = 56 kΩ ± 5% C = 100 pF ± 10%			
Instruction Cycle Time		16	28	µs
CKO as SYNC Input				
t_{SYNC}		400	—	ns
INPUTS:				
IN_3-IN_0, G_3-G_0, L_7-L_0				
t_{SETUP}		—	8.0	µs
t_{HOLD}		—	1.3	µs
SI				
t_{SETUP}		—	2.0	µs
t_{HOLD}		—	1.0	µs
OUTPUT PROPAGATION DELAY	Test condition: C_L = 50 pF, R_L = 20 kΩ, V_{OUT} = 1.5V			
SO, SK Outputs				
t_{PD1}, t_{PD0}		—	4.0	µs
All Other Outputs				
t_{PD1}, t_{PD0}		—	5.6	µs

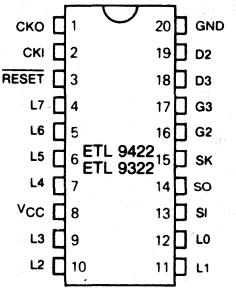
FIGURE 2 – CONNECTION DIAGRAMS



Order number ETL9420/N ETL9320/N
Package N28A



Order Number ETL9421/N, ETL9321/N
Package N24A



Order number ETL9422/N ETL9322/N
Package N20A

Pin	Description
L_7-L_0	8 bidirectional I/O ports with TRI-STATE®
G_3-G_0	4 bidirectional I/O ports
D_3-D_0	4 general purpose outputs
IN_3-IN_0	4 general purpose inputs (ETL9420/L9320 only)
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)

Pin	Description
SK	Logic-controlled clock (or general purpose output)
CKI	System oscillator input
CKO	System oscillator output (or general purpose input, RAM power supply or SYNC input)
$\overline{RESET}$	System reset input
V_{CC}	Power supply
GND	Ground

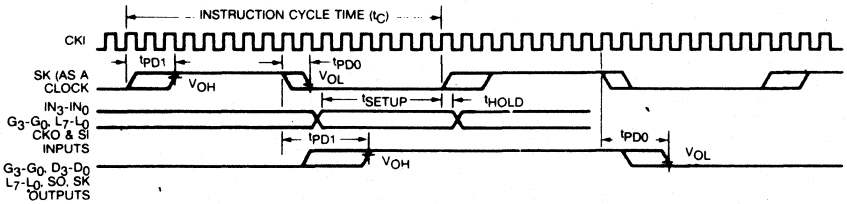


FIGURE 3 – INPUT/OUTPUT TIMING DIAGRAMS (CRYSTAL DIVIDE-BY-16 MODE)

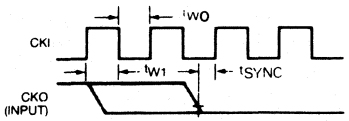


FIGURE 3a – SYNCHRONIZATION TIMING

FUNCTIONAL DESCRIPTION

For ease of reading this description, only ETL9420 and/or ETL9421 are referenced ; however, all such references apply also to ETL9320, L9321, L9322 or ETL9422.

A block diagram of the ETL9420 is given in Figure 1. Data paths arle illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2 volts). When a bit is reset, it is a logic "0" (less than 0.8 volts).

Program Memory

Programm Memory consists of a 1,024 byte ROM. As can be seen by an examination of the ETL9420, L9421, L9422 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQUID instructions, ROM must often be thought of as being organized into 16 pages of 64 words each.

ROM addressing is accomplished by a 10-bit PC register. Its binary value selects one of the 1,024 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 10-bit binary count value. Three levels of subroutine nesting are implemented by the 10-bit subroutine save registers, SA, SB and SC, providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

Data Memory

Data memory consists of a 256-bit RAM, organized as 4 data registers of 16 4-bit digits. RAM addressing is implemented by a 6-bit B register whose upper 2 bits (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the 6-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

Internal Logic

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch data, to input 4 bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

At 4-bit adder performs the arithmetic and logic functions of the ELT9420, L9421, L9422, storing its results in A. It also outputs a carry bit tho the 1 bit C register, most often employed to indicate arithmetic overflow. The C register, in conjuction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below.)

Four general-purpose inputs, IN_3-IN_0, are provided.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. The D outputs can be directly connected to the digits of a multiplexed LED display.

The G register contents are outputs to 4 general-purpose bidirectional I/O ports. G I/O ports can be directly connected to the digits of a multiplexed LED display.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are outputted to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction.)

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa-Sg and decimal point segments of the display.

The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register. (See EN register description, below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/parallel-out shift registers.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

The EN register is an internal 4-bit register loaded under program contol by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

1. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. (See 4 below.) The SK output becomes a logic-controlled clock.
2. With EN_1 set the IN_1 input is enabled as an interrupt input. Immediately following an interrupt, EN_1 is reset to disable further interrupts.
3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables

the L drivers, placing the L I/O ports in a high-impedance input state.

4. EN_3 in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output ; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0". The table below provides a summary of the modes associated with EN_3 and EN_0.

Enable Register Modes — Bits EN_3 and EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = Clock If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = Clock If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

Interrupt

The following features are associated with the IN_1 interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack, pushing in turn the contents of the other subroutine-save registers to the next lower level (PC + 1 → SA → SB → SC). Any previous contents of SC are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN_1 is reset.

b. An interrupt will be acknowledged only after the following conditions are met:
   1. EN_1 has been set.
   2. A low-going pulse ("1" to "0") at least two instruction cycles wide occurs on the IN_1 input.
   3. A currently executing instruction has been completed.
   4. All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed).

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the *end* of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. *At this time*, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines and LQID instructions should not be nested within the interrupt servicing routine since their popping the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

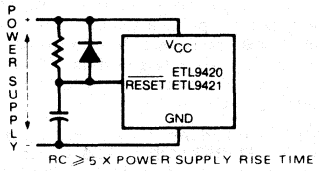
d. The first instruction of the interrupt routine at hex address 0FF must be a NOP.

e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

Initialization

The Reset Logic will initialize (clear) the device upon power-up if the power supply rise time is less than 1ms and greater than 1μs. If the power supply rise time is greater than 1ms, the user must provide an external RC network and diode to the $\overline{RESET}$ pin as shown below. The $\overline{RESET}$ pin is configured as a Schmitt trigger input. If not used it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{RESET}$ input, provided it stays low for at least three instructio cycle times.

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. *Data Memory (RAM) is not cleared upon initialization*. The first instruction at address 0 must be a CLRA.



Power-Up Clear Circuit

Oscillator

There are four basic clock oscillator configurations available as shown by Figure 4.

a. **Crystal Controlled Oscillator.** CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 32 (optional by 16 or 8).

b. **External Oscillator.** CKI is an external clock input signal. The external frequency is divided by 32 (optional by 16 or 8) to give the instruction cycle time. CKO is now available to be used as the RAM power supply (V_R), as a general purpose input, or as a SYNC input.

c. **RC Controlled Oscillator.** CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available as the RAM power supply (V_R) or as a general purpose input

d. **Externally Synchronized Oscillator.** Intended for use in multi-COP systems, CKO is programmed to function as an input connected to the SK output of another COP chip operating at the same frequency (COP chip with L or C suffix) with CKI connected as shown. In this configuration, the SK output connected to CKO must provide a SYNC (instruction cycle) signal to CKO, thereby allowing synchronous data transfer between the COPs using only the SI and SO serial I/O pins in conjunction with the XAS instruction. Note that on power-up SK is automatically enabled as a SYNC output (See Functional Description, Initialization, above).

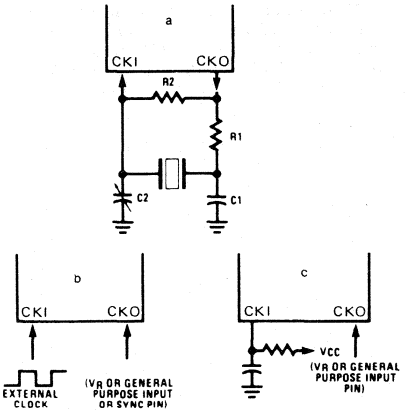
CKO Pin Options

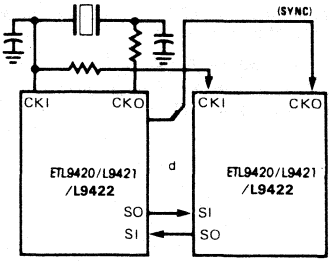
In a crystal controlled oscillator system, CKO is used as an output to the crystal network. As an option CKO can be a SYNC input as described above. As another option CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction. As another option, CKO can be a RAM power supply pin (V_R), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either option is appropriate in application where the ETL9420/L9421/L9422 system timing configuration does not require use of the CKO pin.

RAM Keep-Alive Option (Not available on ETL9422)

Selecting CKO as the RAM power supply (V_R) allows the user to shut off the chip power supply (V_{CC}) and maintain data in the RAM. To insure that RAM data integrity is maintained, the following conditions must be met:

1. $\overline{\text{RESET}}$ must go low before V_{CC} goes below spec during power-off; V_{CC} must be within spec before $\overline{\text{RESET}}$ goes high on power-up.
2. During normal operation V_R must be within the operating range of the chip, with $(V_{CC} - 1) \leq V_R \leq V_{CC}$.
3. V_R must be $\geq$ 3.3V with V_{CC} off.





Crystal Oscillator

Crystal Value	Component Values			
	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)
455 kHz	4.7k	1M	220	220
2.097 MHz	1k	1M	30	6-36

RC Controlled Oscillator

R (kΩ)	C (pF)	Instruction Cycle Time (μs)
51	100	19 ± 15%
82	56	19 ± 13%

Note: 200k $\geq$ R $\geq$ 25k
360 pF $\geq$ C $\geq$ 50 pF

FIGURE 4—ETL9420/L9421/L9422 OSCILLATOR

I/O Options

ETL9420/L9421/L9422 outputs have the following optional configurations, illustrated in Figure 5 :

a. Standard — an enhancement mode device to ground in conjunction with a depletion-mode device to V_{CC}, compatible with LSTTL and CMOS input requirements. Available on SO, SK, and all D and G outputs.

b. Open-Drain — an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, and all D and G outputs.

c. Push-Pull — An enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.

d. Standard L — same as **a.**, but may be disabled. Available on L outputs only.

e. Open Drain L — same as **b.**, but may be disabled. Available on L outputs only.

f. LED Direct Drive — an enhancement-mode device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (See Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display. Available on L outputs only.

g. TRI-STATE® Push-Pull — an enhancement-mode device to ground and V_{CC}. These outputs are TRI-STATE outputs, allowing for connection of these outputs to a data bus shared by other bus drivers. Available on L outputs only.

ETL9420/L9421/L9422 inputs have the following optional configurations.

h. An on-chip depletion load device to V_{CC}.

I. A Hi-Z input which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in Figure 6 for each of these devices to allow the designer to effectively use these I/O configurations in designing a ETL9420/L9421 system.

The SO, SK outputs can be configured as shown in **a.**, **b.**, or **c.** The D and G outputs can be configured as shown in **a.** or **b.** Note that when inputting data to the G ports, the G outputs should be set to "1". The L outputs can be configured as in **d.**, **e.**, **f.** or **g.**

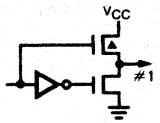
An important point to remember if using configuration **d.** or **f.** with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current (see Figure 6, device 2); however, when the L lines are used as inputs, the disabled depletion device *cannot* be relied on to source sufficient current to pull an input to a logic 1.

ETL9421

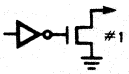
If the ETL9420 is bonded as a 24-pin device, it becomes the ETL9421, illustrated in Figure 2, ETL9420/L9421 Connection Diagrams. Note that the ETL9421 does not contain the four general purpose IN inputs (IN_3-IN_0). Use of this option precludes, of course, use of the IN options and the interrupt feature. All other options are available for the ETL9421.

ETL9422

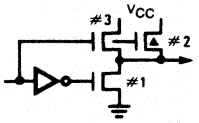
If the ETL9420is bonded as a 20-pin device, it becomes the ETL9422, as illustrated in Figure 2. Note that the ETL9422 contains all the ETL9421 pins except D_0, D_1, G_0, and G_1, ETL9422 also does not allow RAM power supply input as a valid CKO pin option.



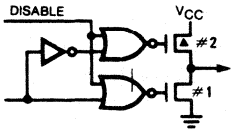
a. Standard Output



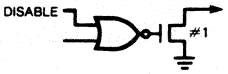
b. Open-Drain Output



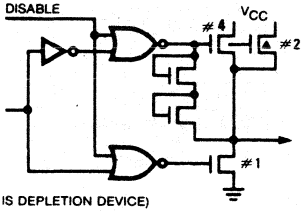
c. Push-Pull Output



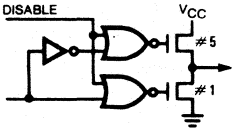
d. Standard L Output



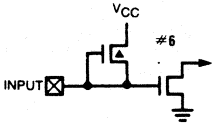
e. Open-Drain L Output



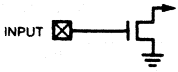
f. LED (L Output)



g. TRI-STATE® Push-Pull (L Output)



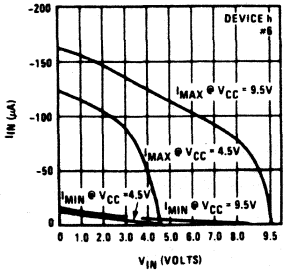
h. Input with Load



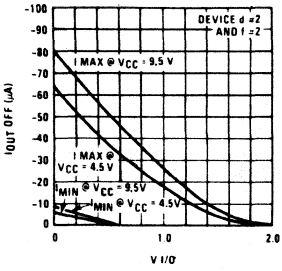
i. Hi-Z Input

FIGURE 5 – OUTPUT CONFIGURATIONS

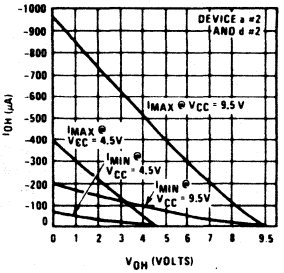
Input current IN_0-IN_3



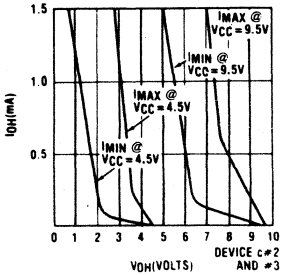
Input current for L_0-L_7 when output programmed OFF by software



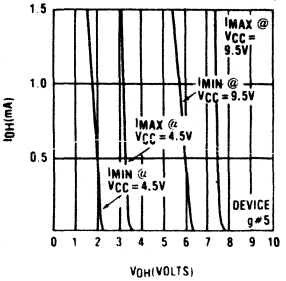
Source current for standard output configuration



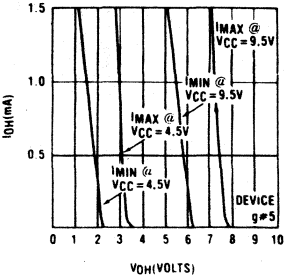
Source current for SO and SK in push-pull configuration



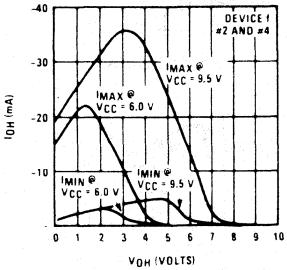
Source Current for L0-L7 in TRI-STATE® Configuration (High Current Option)



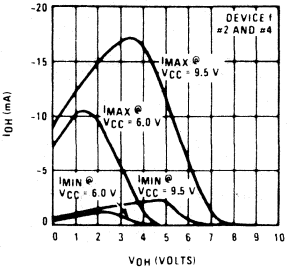
Source Current for L0-L7 in TRI-STATE® Configuration (Low Current Option)



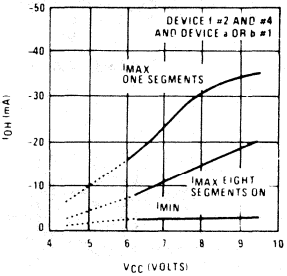
LED output source current (for high current LED option)



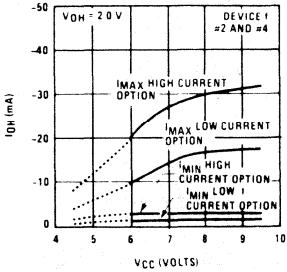
LED output source current (for low current LED option)



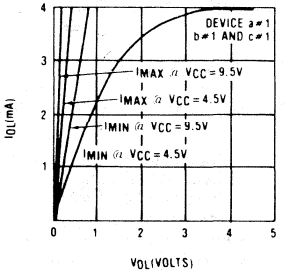
LED Output Direct Segment and Digit Drive (High Current Options on L0-L7) (Very High Current Options on D0-D3 or G0-G3)



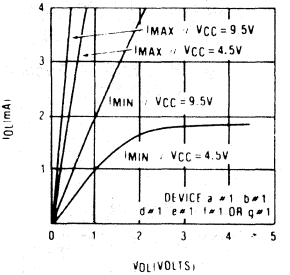
LED Output Direct Segment Drive



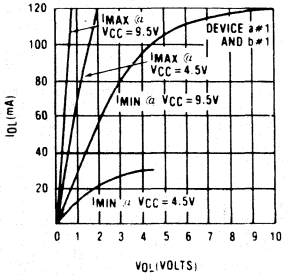
Output sink current for SO and SK



Output sink current for L_0-L_7 and standard drive option for D_0-D_3 and G_0-G_3



Output Sink Current G0-G3 and D0-D3 with Very High Current Option



Output sink current for G_0-G_3 and D_0-D_3 (for high current option)

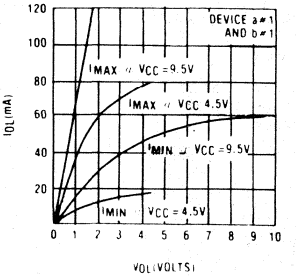
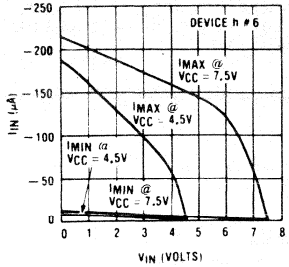
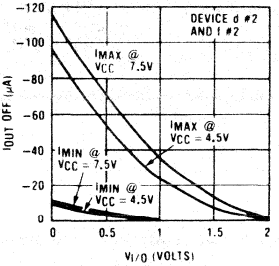


FIGURE 6 – ETL9420/L9421/L9422 INPUT/OUTPUT CHARACTERISTICS

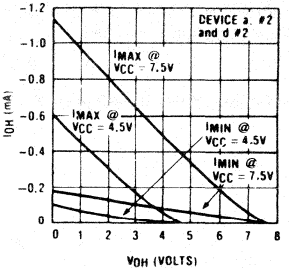
Input IN_0-IN_3



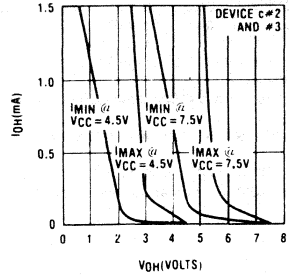
Input Current for L0-L7 when Output Programmed Off by Software



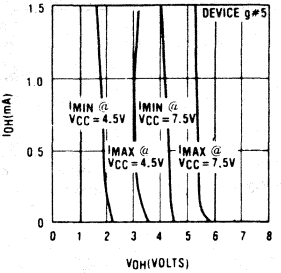
Source current for standard output configuration



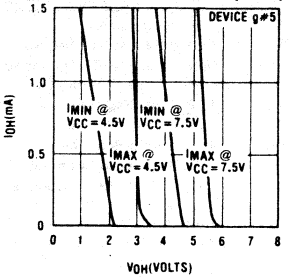
Source current for SO and SK in push-pull configuration



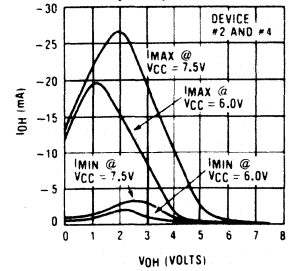
Source Current for L0-L7 in TRI-STATE ® Configuration (High Current Option)



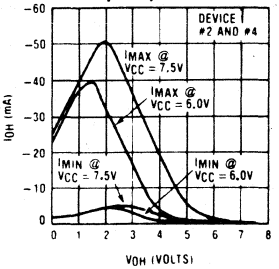
Source Current for L0-L7 in TRI-STATE ® Configuration (Low Current Option)



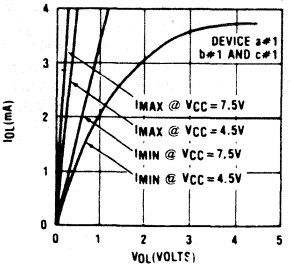
LED output source current (for low current LED option)



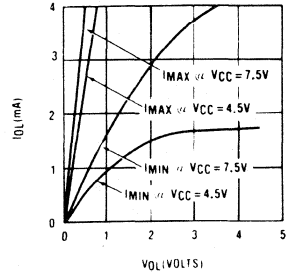
LED output source current (for high current LED option)



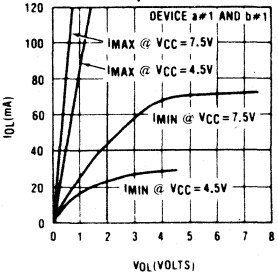
Output sink current for SO and SK



Output sink current for L_0-L_7, standard drive option for D_0-D_3 and G_0-G_3



Output Sink Current G_0-G_3 and D_0-D_3 with Very High Current Option



Output sink current for G_0-G_3 and D_0-D_3 (for high current option)

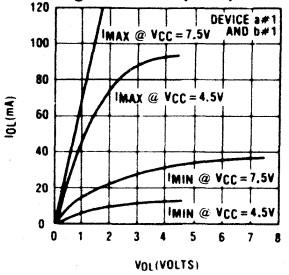


FIGURE 7 – ETL9320/L9321/L9322 INPUT/OUTPUT CHARACTERISTICS

ETL9420/L9421/L9422 - INSTRUCTION SET

Table 1 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 2 provides the mnemonic, operand, machine code, data flow, skip conditions, and description associated with each instruction in the ETL9420/L9421/L9422 instruction set.

TABLE 1 — ETL9420/L9421/L9422 INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
IL	Two 1-bit Latches associated with the IN_3 or IN_0 Inputs
IN	4-bit Input Port
L	8-bit TRI-STATE I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
PC	10-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	10-bit Subroutine Save Register A
SB	10-bit Subroutine Save Register B
SC	10-bit Subroutine Save Register C
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0 - 15 binary (RAM Digit Select)
r	2-bit Operand Field, 0 - 3 binary (RAM Register Select)
a	10-bit Operand Field, 0 - 1023 binary (ROM Address)
y	4-bit Operand Field, 0 - 15 binary (Immediate Data)
RAM(s)	Contents of RAM location addressed by s
ROM(t)	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
−	Minus
←	Replaces
↔	Is exchanged with
=	Is equal to
$\overline{A}$	The ones complement of A
⊕	Exclusive-OR
:	Range of values

TABLE 2 — ETL9420/L9421/L9422 INSTRUCTION SET

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011|0000	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0011|0001	A + RAM(B) → A	None	Add RAM to A
ADT		4A	0100|1010	$A + 10_{10} \rightarrow A$	None	Add Ten to A
AISC	y	5-	0101| y	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CASC		10	0001|0000	$\overline{A}$ + RAM(B) + C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	0000|0000	0 → A	None	Clear A
COMP		40	0100|0000	$\overline{A} \rightarrow A$	None	Ones complement of A to A
NOP		44	0100|0100	None	None	No Operation
RC		32	0011|0010	"0" → C	None	Reset C
SC		22	0010|0010	"1" → C	None	Set C
XOR		02	0000|0010	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1111|1111	ROM ($PC_{9:8}$, A,M) → $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6- --	0110|00|$a_{9:8}$ $a_{7:0}$	a → PC	None	Jump
JP	a	-- -- (all other pages)	1| $a_{6:0}$ (pages 2,3 only) or 11| $a_{5:0}$	a → $PC_{6:0}$ a → $PC_{5:0}$	None	Jump within Page (Note 4)
JSRP	a	--	10| $a_{5:0}$	PC + 1 → SA → SB → SC 0010 → $PC_{9:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6- --	0110|10|$a_{9:8}$ $a_{7:0}$	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
RET		48	0100|1000	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0100|1001	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip

TABLE 2 — ETL9420/L9421/L9422 INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33 3C	0011|0011 0011|1100	$A \rightarrow Q_{7:4}$ $RAM(B) \rightarrow Q_{3:0}$	None	Copy A, RAM to Q
CQMA		33 2C	0011|0011 0010|1100	$Q_{7:4} \rightarrow RAM(B)$ $Q_{3:0} \rightarrow A$	None	Copy Q to RAM, A
LD	r	-5	00| r |0101	$RAM(B) \rightarrow A$ $Br \oplus r \rightarrow Br$	None	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	23 --	0010|0011 00| r | d	$RAM(r,d) \rightarrow A$	None	Load A with RAM pointed to directly by r,d
LQID		BF	1011|1111	$ROM(PC_{9:8},A,M) \rightarrow Q$ $SB \rightarrow SC$	None	Load Q Indirect (Note 3)
RMB	0 1 2 3	4C 45 42 43	0100|1100 0100|0101 0100|0010 0100|0011	$0 \rightarrow RAM(B)_0$ $0 \rightarrow RAM(B)_1$ $0 \rightarrow RAM(B)_2$ $0 \rightarrow RAM(B)_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	0100|1101 0100|1101 0100|0110 0100|1011	$1 \rightarrow RAM(B)_0$ $1 \rightarrow RAM(B)_1$ $1 \rightarrow RAM(B)_2$ $1 \rightarrow RAM(B)_3$	None	Set RAM Bit
STII	y	7-	0111| y	$y \rightarrow RAM(B)$ $Bd + 1 \rightarrow Bd$	None	Store Memory Immediate and Increment Bd
X	r	-6	00| r |0110	$RAM(B) \leftrightarrow A$ $Br \oplus r \rightarrow Br$	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23 --	0010|0011 10| r | d	$RAM(r,d) \leftrightarrow A$	None	Exchange A with RAM pointed to directly by r,d
XDS	r	-7	00| r |0111	$RAM(B) \leftrightarrow A$ $Bd - 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	-4	00| r |0100	$RAM(B) \leftrightarrow A$ $Bd + 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101|0000	$A \rightarrow Bd$	None	Copy A to Bd
CBA		4E	0100|1110	$Bd \rightarrow A$	None	Copy Bd to A
LBI	r,d	-- (d = 0, 9:15) or 33 -- (any d)	00| r |(d - 1) 0011|0011 10| r | d	r,d → B	Skip until not a LBI	Load B Immediate with r,d (Note 6)
LEI	y	33 6-	0011|0011 0110| y	$y \rightarrow EN$	None	Load EN Immediate (Note 7)
XABR		12	0001|0010	$A \leftrightarrow Br\ (0,0 \rightarrow A_3,A_2)$	None	Exchange A with Br

TABLE 2 — ETL9420/L9421/L9422 INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TEST INSTRUCTIONS						
SKC		20	0010 0000		C = "1"	Skip if C is True
SKE		21	0010 0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0011 0011 0010 0001		$G_{3:0} = 0$	Skip if G is Zero (all 4 bits)
SKGBZ		33	0011 0011	1st byte		Skip if G Bit is Zero
	0	01	0000 0001	2nd byte	$G_0 = 0$	
	1	11	0001 0001		$G_1 = 0$	
	2	03	0000 0011		$G_2 = 0$	
	3	13	0001 0011		$G_3 = 0$	
SKMBZ	0	01	0000 0001		$RAM(B)_0 = 0$	Skip if RAM Bit is Zero
	1	11	0001 0001		$RAM(B)_1 = 0$	
	2	03	0000 0011		$RAM(B)_2 = 0$	
	3	13	0001 0011		$RAM(B)_3 = 0$	
SKT		41	0100 0001		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	0011 0011 0010 1010	G → A	None	Input G Ports to A
ININ		33 28	0011 0011 0010 1000	IN → A	None	Input IN Inputs to A (Note 2)
INIL		33 29	0011 0011 0010 1001	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (Note 3)
INL		33 2E	0011 0011 0010 1110	$L_{7:4}$ → RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM,A
OBD		33 3E	0011 0011 0011 1110	Bd → D	None	Output Bd to D Outputs
OGI	y	33 5-	0011 0011 0101 y	y → G	None	Output to G Ports Immediate
OMG		33 3A	0011 0011 0011 1010	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0100 1111	A ↔ SIO, C → SKL	None	Exchange A with SIO (Note 3)

Note 1 : All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2 : The ININ instruction is only available on the 28-pin ETL9420 as the other devices do not contain the IN inputs.

Note 3 : For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4 : The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5 : A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6 : LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14 or 15. The machine code for the lower 4 bits equals the binary value of the "d" data *minus 1*, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 7 : Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description EN Register).

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide note useful to programmers in writing ETL9420/L9421/L9422 programs.

XAS Instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register, above.) If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM addressed by the 10-bit word, $PC_{9:8}$, A, M, PC_9 and PC_8 are not affected by this instruction.

Note that JID requires 2 instruction cycles to execute.

INIL Instruction

INIL (Input IL Latches to A) inputs 2 latches, IL_3 and IL_0 (see Figure 8) and CKO into A. The IL_3 and IL_0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN_3 and IN_0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs IL_3 and IL_0 into A3 and A0 respectively, and resets these latchés to allow them to respond to subsequent low-going pulses. on the IN_3 and IN_0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A "0" is always placed in A1 upon the execution of an INIL. The general purpose inputs IN_3-IN_0 are input to A upon execution of an ININ instruction. (See Table 2, ININ instruction.) INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction. IL latches are *not cleared* on reset.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 10-bit word PC_9, PC_8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB →SC) and replaces the least significant 8 bits of PC as follows: A →$PC_{7:4}$, RAM(B) →$PC_{3:0}$, leaving PC_9 and PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA →PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the contents of SB are placed in SC (SB → SC). Note that LQID takes two instruction cycle times to execute.

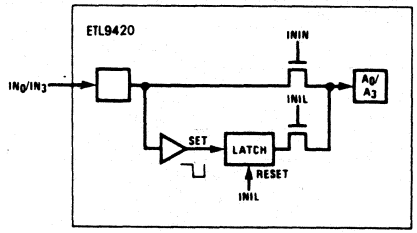


FIGURE 8 – INIL HARDWARE IMPLEMENTATION

SKT Instruction

The SKT (Skip On Timer) instruction tests the state of an internal 10-bit time-base counter. This counter divides the instruction cycle clock frequency by 1024 and provides a latched indication of counter overflow. The SKT instruction tests this latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction, therefore, allow the ELT9420/L9421/L9422 to generate its own tim-base for real-time processing rather than relying on an external input signal.

For example, using a 2.097 MHz crystal as the time-base to the clock generator, the instruction cycle clock frequency will be 65kHz (crystal frequency ÷ 32) and the binary counter output pulse frequency will be 64Hz. For time-of-day or similar real-time processing, the SKT instruction can call a routine which increments a "seconds" counter every 64 ticks.

Instruction Set Notes

a. The first word of a ETL9420/L9421/L9422 programm (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths except JID and LQID take the same number of cycle times whether instructions are skipped or executed. JID and LQID instructions take 2 cycles if executed and 1 cycle if skipped.

c. The ROM is organized into 16 pages of 64 words each. The Program Counter is a 10-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3, 7, 11, or 15 will access data in the next group of four pages.

OPTION LIST

The ETL9420/L9421/L9422 mask-programmable options ar assigned numbers which correspond with the ETL9420 pins.

The following is a list of ETL9420 options. When specifying a ETL9421 chip, Options 9, 10, 19, and 20 must all be set to zero. When specifying a ETL9422 chip, options 9, 10, 19, and 20 must all be set to zero ; options 21 and 22 may not be set to one, three or five ; and option 2 may not be set to one. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Output
- = 0: clock generator output to crystal/resonator (0 not allowable value if Option 3 = 3)
- = 1: pin is RAM power supply (V_R) input (not available on the ETL9422)
- = 2: general purpose input with load device to V_{CC}
- = 3: general purpose input, Hi-Z
- = 4: multi-COP SYNC input (CKI ÷ 32, CKI ÷ 16)
- = 5: multi-COP SYNC input (CKI ÷ 8)

Option 3: CKI Input
- = 0: oscillator input divided by 32 (2 MHz max.)
- = 1: oscillator input divided by 16 (1 MHz max.)
- = 2: oscillator input divided by 8 (500 kHz max.)
- = 3: single-pin RC controlled oscillator (÷4)
- = 4: Schmitt trigger clock input (÷4)

Option 4: RESET Input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 5: L_7 Driver
- = 0: Standard output
- = 1: Open-drain output
- = 2: High current LED direct segment drive output
- = 3: High current TRI-STATE® push-pull output
- = 4: Low-current LED direct segment drive output
- = 5: Low-current TRI-STATE® push-pull output

Option 6: L_6 Driver
same as Option 5

Option 7: L_5 Driver
same as Option 5

Option 8: L_4 Driver
same as Option 5

Option 9: IN_1 Input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 10: IN_2 Input:
same as Option 9

Option 11: V_{CC} pin
- = 0: Standard V_{CC}
- = 1: Optional higher voltage V_{CC}

Option 12: L_3 Driver
same as Option 5

Option 13: L_2 Driver
same as Option 5

Option 14: L_1 Driver
same as Option 5

Option 15: L_0 Driver
same as Option 5

Option 16: SI Input
same as Option 9

Option 17: SO Driver
- = 0: standard output
- = 1: open-drain output
- = 2: push-pull output

Option 18: SK Driver
same as Option 17

Option 19 : IN_0 Input
same as Option 9

Option 20: IN_3 Input
same as Option 9

Option 21: G_0 I/O Port
- = 0: very-high current standard output
- = 1: very-high current open-drain output
- = 2: high current standard output
- = 3: high current open-drain output
- = 4: standard LSTTL output (fanout = 1)
- = 5: open-drain LSTTL output (fanout = 1)

Option 22: G_1 I/O Port
same as Option 21

Option 23: G_2 I/O Port
same as Option 21

Option 24: G_3 I/O Port
same as Option 21

Option 25: D_3 Output
same as Option 21

Option 26: D_2 Output
same as Option 21

Option 27: D_1 Output
same as Option 21

Option 28: D_0 Output
same as Option 21

Option 29: L Input Levels
- = 0: standard TTL input levels ("0" = 0.8V, "1" = 2.0V)
- = 1: higher voltage input levels ("0" = 1.2V, "1" = 3.6V)

Option 30: IN Input Levels
same as Option 29

Option 31: G Input Levels
same as Option 29

Option 32: SI Input Levels
same as Option 29

Option 33: $\overline{\text{RESET}}$ Input
- = 0: Schmitt trigger input
- = 1: standard TTL input levels
- = 2: higher voltage input levels

Option 34: CKO Input Levels (CKO = input; Option 2 = 2,3)
same as Option 29

Option 35 COP Bonding
- = 0: ETL9420 (28-pin device)
- = 1: ETL9421 (24-pin device)
- = 2: 28 and 24-pin versions
- = 3: ETL9422 (20-pin device)
- = 4: 28- and 20-pin versions
- = 5: 24- and 20-pin versions
- = 6: 28-, 24-, and 20-pin versions

TEST MODE (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed ETL9420. With SO forced to logic "1", two test modes are provided, depending upon the value of SI :

a. RAM and Internal Logic Test Mode (SI = 1)

b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user; they are intended for manufacturing test only.

APPLICATION 1 : ETL9420 General Controller

Figure 9 shows an interconnect diagram for a ETL9420 used as a general controller. Operation of the system is as follows :

1. The L_7-L_0 outputs are configured as LED Direct Drive outputs, allowing direct connection to the segments of the display.
2. The D_3-D_0 outputs drive the digits of the multiplexed display directly and scan the columns of the 4 x 4 keyboard matrix.
3. The IN_3-IN_0 inputs are used to input the 4 rows of the keyboard matrix. Reading the IN lines in conjunction with the current value of the D outputs allows detection, debouncing, and decoding of any one of the 16 keyswitches.
4. CKI is configured as a single-pin oscillator input allowing system timing to be controlled by a single-pin RC network. CKO is therefore available for use as a V_R RAM power supply pin. RAM data integrity is thereby assured when the main power supply is shut down (see RAM Keep-Alive option description).
5. SI is selected as the input to a binary counter input. With SIO used as a binary counter, SO and SK can be used as general purpose outputs.
6. The 4 bidirectional G I/O ports (G_3-G_0) are available for use as required by the user's application.

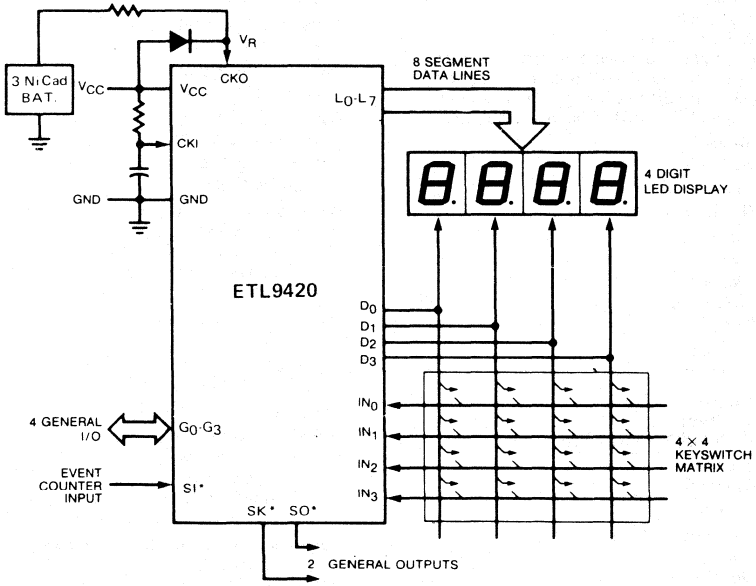


FIGURE 9 – ETL9420 KEYBOARD/DISPLAY INTERFACE

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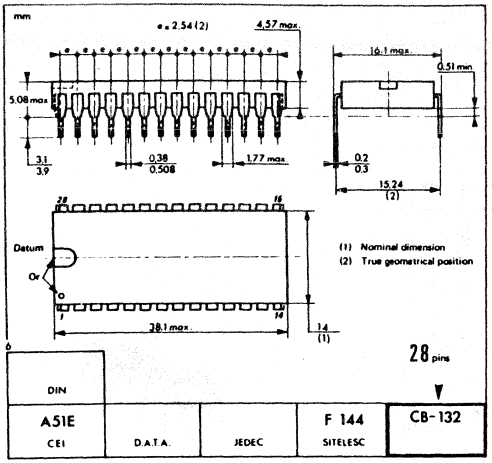
PHYSICAL DIMENSIONS



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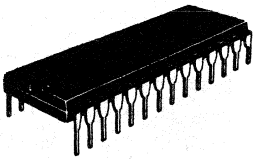
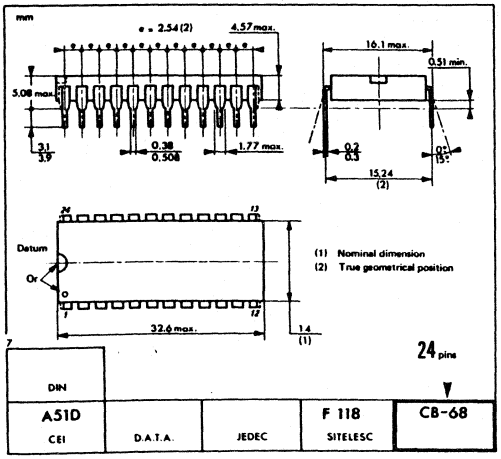


N SUFFIX
PLASTIC PACKAGE



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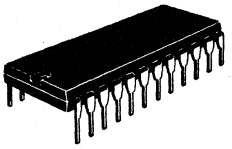

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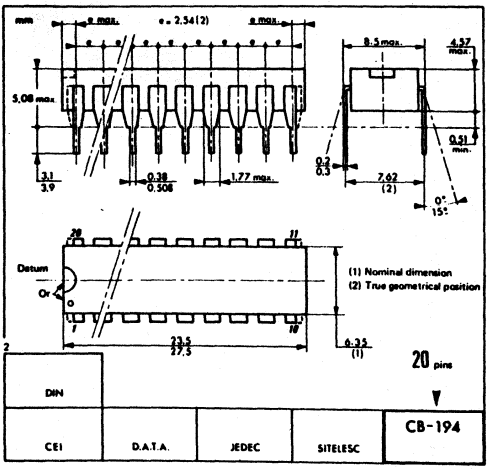

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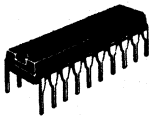

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The ETL9444/L9445 and ETL9344/L9345 Single-Chip N-Channel Microcontrollers are fully compatible with the COPS® family, fabricated using N-channel, silicon gate XMOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The ETL9445 is identical to the ETL9444, except with 19 I/O lines instead of 23 : They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized controller oriented processor at a low end-product cost.

The ETL9344/L9345 are exact functional equivalents, but extended temperature range versions of the ETL9444/L9445 respectively.

- Low cost
- Powerful instruction set
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- 23 I/O lines (ETL9444)
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- Three-level subroutine stack
- 16 μs instruction time
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- Internal binary counter register with MICROWIRE® serial I/O capability
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- Direct drive of LED digit and segment lines
- Software/hardware compatible with other members of ET 9400 family
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- Wider supply range (4.5-9.5V) optionally available

NMOS

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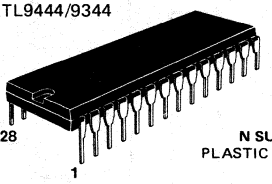
ETL9444/9344



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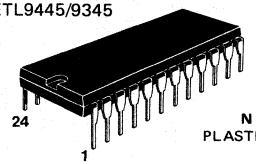

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PIN ASSIGNMENT

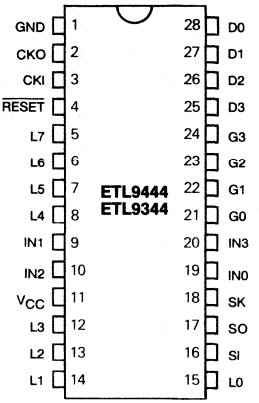

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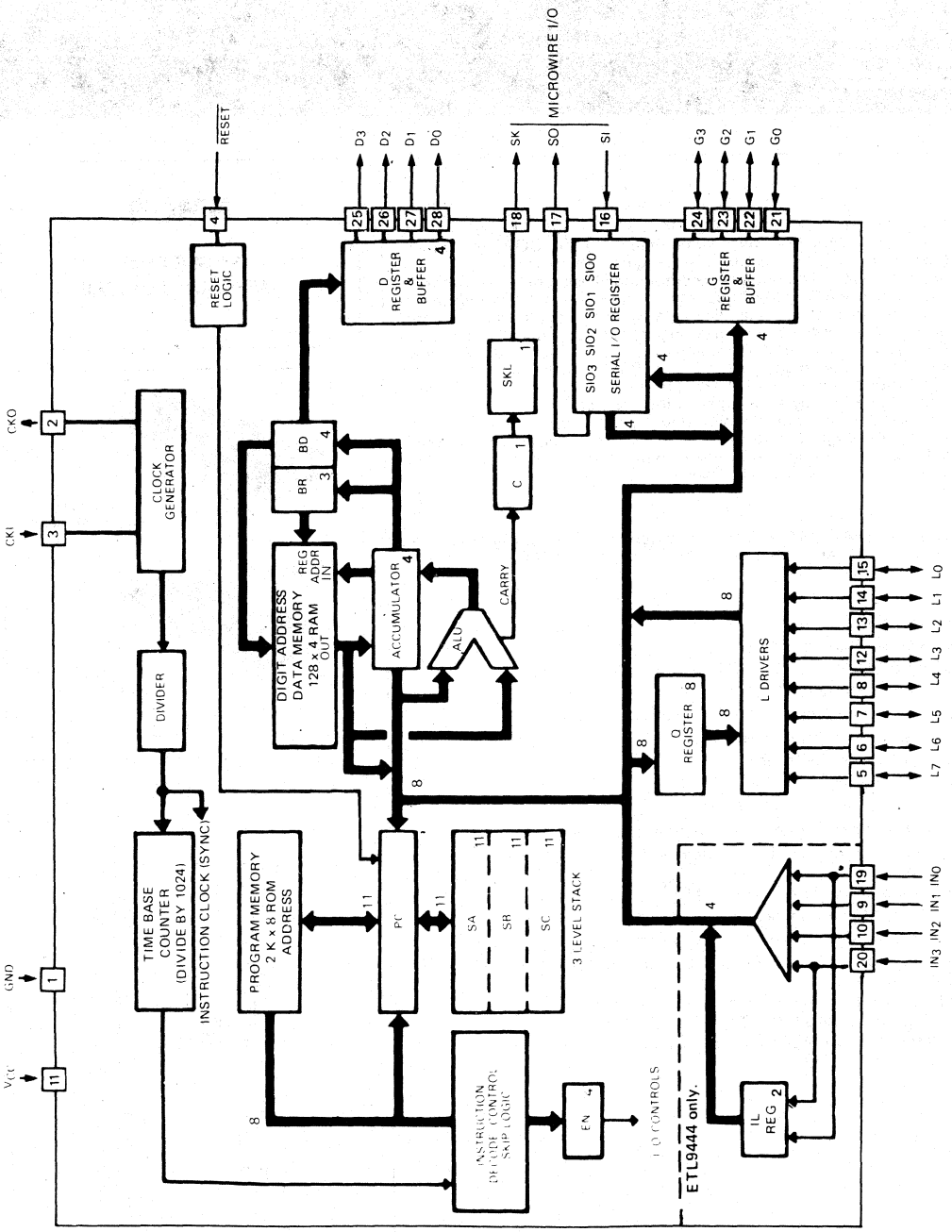
FIGURE 1 – BLOCK DIAGRAM (28-pin version)



ETL9444/L9445

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	0.75 Watt at 25°C 0.4 Watt at 70°C
Total Source Current	120 mA
Total Sink Current	120 mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 9.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Standard Operating Voltage (V_{CC})	Note 1	4.5	6.3	V
Optional Operating Voltage (V_{CC})		4.5	9.5	V
Power Supply Ripple	peak to peak	–	0.5	V
Operating Supply Current	all inputs and outputs open	–	13	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input (÷32, ÷16, ÷8)				
Logic High (V_{IH})		2.0	–	V
Logic Low (V_{IL})		−0.3	0.4	V
Schmitt Trigger Input (÷4)				
Logic High (V_{IH})		0.7 V_{CC}	–	V
Logic Low (V_{IL})		−0.3	0.6	V
$\overline{\text{RESET}}$ Input Levels	Schmitt trigger input			
Logic High		0.7 V_{CC}	–	V
Logic Low		−0.3	0.6	V
SO Input Level (Test mode)		2.0	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0	–	V
Logic High	with TTL trip level options	2.0	–	V
Logic Low	selected, $V_{CC} = 5V \pm 5\%$	−0.3	0.8	V
Logic High	with high trip level options	3.6	–	V
Logic Low	selected	−0.3	1.2	V
Input Capacitance		–	7	pF
Hi-Z Input Leakage		−1	+1	µA
Output Voltage Levels				
LSTTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High (V_{OH})	$I_{OH} = -25\mu A$	2.7	–	V
Logic Low (V_{OL})	$I_{OL} = 0.36mA$	–	0.4	V
CMOS Operation				
Logic High	$I_{OH} = -10\mu A$	$V_{CC} - 1$	–	V
Logic Low	$I_{OL} = +10\mu A$	–	0.2	V

Note 1 : V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

ETL9444/L9445

DC ELECTRICAL CHARACTERISTICS (continued) $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 9.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	$V_{CC} = 9.5V$, $V_{OL} = 0.4V$	1.8	–	mA
	$V_{CC} = 6.3V$, $V_{OL} = 0.4V$	1.2	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.9	–	mA
L_0-L_7 Outputs and Standard	$V_{CC} = 9.5V$, $V_{OL} = 0.4V$	0.8	–	mA
G_0-G_3, D_0-D_3 Outputs (I_{OL})	$V_{CC} = 6.3V$, $V_{OL} = 0.4V$	0.5	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.4	–	mA
G_0-G_3 and D_0-D_3 Outputs with	$V_{CC} = 9.5V$, $V_{OL} = 1.0V$	15	–	mA
High Current Options (I_{OL})	$V_{CC} = 6.3V$, $V_{OL} = 1.0V$	11	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	7.5	–	mA
G_0-G_3 and D_0-D_3 Outputs with	$V_{CC} = 9.5V$, $V_{OL} = 1.0V$	30	–	mA
Very High Current Options (I_{OL})	$V_{CC} = 6.3V$, $V_{OL} = 1.0V$	22	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	15	–	mA
CKI (Single-pin RC oscillator)	$V_{CC} = 4.5V$, $V_{IH} = 3.5V$	2	–	mA
CKO	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.2	–	mA
Output Source Current				
Standard Configuration,	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−140	−800	µA
All Outputs (I_{OH})	$V_{CC} = 6.3V$, $V_{OH} = 2.0V$	−75	−480	µA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	−30	−250	µA
Push-Pull Configuration	$V_{CC} = 9.5V$, $V_{OH} = 4.75V$	−1.4	–	mA
SO and SK Outputs (I_{OH})	$V_{CC} = 6.3V$, $V_{OH} = 2.4V$	−1.4	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.0V$	−1.2	–	mA
LED Configuration, L_0-L_7				
Outputs, Low Current	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−1.5	−18	mA
Driver Option (I_{OH})	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−1.5	−13	mA
LED Configuration, L_0-L_7				
Outputs, High Current	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−3.0	−35	mA
Driver Option (I_{OH})	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−3.0	−25	mA
TRI-STATE® Configuration,	$V_{CC} = 9.5V$, $V_{OH} = 5.5V$	−0.75	–	mA
L_0-L_7 Outputs, Low	$V_{CC} = 6.3V$, $V_{OH} = 3.2V$	−0.8	–	mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−0.9	–	mA
TRI-STATE® Configuration,	$V_{CC} = 9.5V$, $V_{OH} = 5.5V$	−1.5	–	mA
L_0-L_7 Outputs, High	$V_{CC} = 6.3V$, $V_{OH} = 3.2V$	−1.6	–	mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−1.8	–	mA
Input Load Source Current	$V_{CC} = 5.0V$, $V_{IL} = 0V$	−10	−140	µA
CKO Output				
RAM Power Supply Option				
Power Requirement	$V_R = 3.3V$	–	6.0	mA
TRI-STATE® Output Leakage Current		−2.5	+2.5	µA
Total Sink Current Allowed				
All Outputs Combined		–	120	mA
D, G Ports		–	120	mA
L_7-L_4		–	4	mA
L_3-L_0		–	4	mA
All Other Pins		–	1.5	mA
Total Source Current Allowed				
All I/O Combined		–	120	mA
L_7-L_4		–	60	mA
L_3-L_0		–	60	mA
Each L Pin		–	30	mA
All Other Pins		–	1.5	mA

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	−40°C to +85°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	0.75 Watt at 25°C 0.25 Watt at 85°C
Total Source Current	120 mA
Total Sink Current	120 mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS — $40°C \leq T_A \leq +85°C$, $4.5V \leq V_{CC} \leq 7.5V$ (Unless otherwise specified)

Parameter	Conditions	Min.	Max.	Units
Standard Operating Voltage (V_{CC})	Note 1	4.5	5.5	V
Optional Operating Voltage (V_{CC})		4.5	7.5	V
Power Supply Ripple	peak to peak	–	0.5	V
Operating Supply Current	all inputs and outputs open	–	15	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (V_{IH})		2.2	–	V
Logic Low (V_{IL})		−0.3	0.3	V
Schmitt Trigger Input				
Logic High (V_{IH})		0.7 V_{CC}	–	V
Logic Low (V_{IL})		−0.3	0.4	V
$\overline{\text{RESET}}$ Input Levels	Schmitt Trigger Input			
Logic High		0.7 V_{CC}	–	V
Logic Low		−0.3	0.4	V
SO Input Level (Test mode)		2.2	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0	–	V
Logic High	with TTL trip level options	2.2	–	V
Logic Low	selected, $V_{CC} = 5V \pm 5\%$	−0.3	0.6	V
Logic High	with high trip level options	3.6	–	V
Logic Low	selected	−0.3	1.2	V
Input Capacitance		–	7	pF
Hi-Z Input Leakage		−2	+2	µA
Output Voltage Levels				
LSTTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High (V_{OH})	$I_{OH} = -20\mu A$	2.7	–	V
Logic Low (V_{OL})	$I_{OL} = 0.36mA$	–	0.4	V
CMOS Operation				
Logic High	$I_{OH} = -10\mu A$	$V_{CC} - 1$	–	V
Logic Low	$I_{OL} = +10\mu A$	–	0.2	V

Note 1 : V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

ETL9344/L9345

DC ELECTRICAL CHARACTERISTICS (continued) $-40°C \leq T_A \leq +85°C$, $4.5V \leq V_{CC} \leq 7.5V$ (Unless otherwise specified).

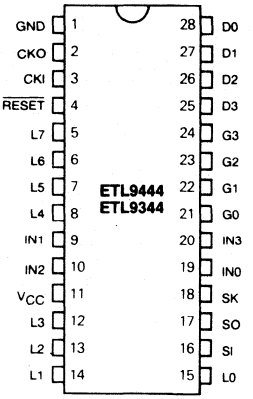
Parameter	Conditions	Min.	Max.	Units
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	$V_{CC} = 7.5V$, $V_{OL} = 0.4V$	1.4	–	mA
	$V_{CC} = 5.5V$, $V_{OL} = 0.4V$	1.0	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.8	–	mA
L_0-L_7 Outputs, and Standard	$V_{CC} = 7.5V$, $V_{OL} = 0.4V$	0.6	–	mA
G_0-G_3, D_0-D_3 Outputs (I_{OL})	$V_{CC} = 5.5V$, $V_{OL} = 0.4V$	0.5	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.4	–	mA
G_0-G_3 and D_0-D_3 Outputs with	$V_{CC} = 7.5V$, $V_{OL} = 1.0V$	12	–	mA
High Current Options (I_{OL})	$V_{CC} = 5.5V$, $V_{OL} = 1.0V$	9	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	7	–	mA
G_0-G_3 and D_0-D_3 Outputs with	$V_{CC} = 7.5V$, $V_{OL} = 1.0V$	24	–	mA
Very High Current Options (I_{OL})	$V_{CC} = 5.5V$, $V_{OL} = 1.0V$	18	–	mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	14	–	mA
CKI (Single-pin RC oscillator)	$V_{CC} = 4.5V$, $V_{IH} = 3.5V$	2	–	mA
CKO	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	0.2	–	mA
Output Source Current				
Standard Configuration,	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	−100	−900	μA
All Outputs (I_{OH})	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	−55	−600	μA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	−28	−350	μA
Push-Pull Configuration	$V_{CC} = 7.5V$, $V_{OH} = 3.75V$	−0.85	–	mA
SO and SK Outputs (I_{OH})	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	−1.1	–	mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.0V$	−1.2	–	mA
LED Configuration, L_0-L_7	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	−1.4	−27	mA
Outputs, Low Current	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−1.4	−17	mA
Driver Option (I_{OH})	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	−0.7	−15	mA
LED Configuration, L_0-L_7	$V_{CC} = 7.5V$, $V_{OH} = 2.0V$	−2.7	−54	mA
Outputs, High Current	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−2.7	−34	mA
Driver Option (I_{OH})	$V_{CC} = 5.5V$, $V_{OH} = 2.0V$	−1.4	−30	mA
TRI-STATE® Configuration,	$V_{CC} = 7.5V$, $V_{OH} = 4.0V$	−0.7	–	mA
L_0-L_7 Outputs, Low	$V_{CC} = 5.5V$, $V_{OH} = 2.7V$	−0.6	–	mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−0.9	–	mA
TRI-STATE® Configuration,	$V_{CC} = 7.5V$, $V_{OH} = 4.0V$	−1.4	–	mA
L_0-L_7 Outputs, High	$V_{CC} = 5.5V$, $V_{OH} = 2.7V$	−1.2	–	mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−1.8	–	mA
Input Load Source Current	$V_{CC} = 5.0V$, $V_{IL} = 0V$	−10	−200	μA
CKO Output				
RAM Power Supply Option				
Power Requirement	$V_R = 3.3V$	–	8.0	mA
TRI-STATE® Output Leakage Current		−5	+5	μA
Total Sink Current Allowed				
All Outputs Combined		–	120	mA
D, G Ports		–	120	mA
L_7-L_4		–	4	mA
L_3-L_0		–	4	mA
All Other Pins		–	1.5	mA
Total Source Current Allowed				
All I/O Combined		–	120	mA
L_7-L_4		–	60	mA
L_3-L_0		–	60	mA
Each L Pin		–	30	mA
All Other Pins		–	1.5	mA

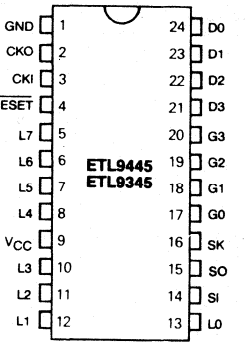
AC ELECTRICAL CHARACTERISTICS

ETL9444/L9445 : 0°C ≤ T_A ≤ 70°C, 4.5V ≤ V_{CC} ≤ 9.5V (Unless otherwise specified)
ETL9344/L9345 : −40°C ≤ T_A ≤ +85°C, 4.5V ≤ V_{CC} ≤ 7.5V (Unless otherwise specified).

Parameter	Conditions	Min.	Max.	Units
Instruction Cycle Time — t_C		16	40	µs
CKI				
Input Frequency — f_I	÷32 mode	0 8	2.0	MHz
	÷16 mode	0.4	1.0	MHz
	÷8 mode	0.2	0.5	MHz
	÷4 mode	0.1	0.25	MHz
Duty Cycle		30	60	%
Rise Time	f_I = 2 MHz	–	120	ns
Fall Time		–	80	ns
CKI Using RC (÷4)	R = 56 kΩ ± 5% C = 100 pF ± 10%			
Instruction Cycle Time		16	28	µs
CKO as SYNC Input				
t_{SYNC}		400	–	ns
INPUTS:				
IN_3-IN_0, G_3-G_0, L_7-L_0				
t_{SETUP}		–	8.0	µs
t_{HOLD}		–	1.3	µs
SI				
t_{SETUP}		–	2.0	µs
t_{HOLD}		–	1.0	µs
OUTPUT PROPAGATION DELAY	Test condition: C_L = 50 pF, R_L = 20 kΩ, V_{OUT} = 1.5V			
SO, SK Outputs				
t_{pd1}, t_{pd0}		–	4.0	µs
All Other Outputs				
t_{pd1}, t_{pd0}		–	5.6	µs

FIGURE 2 – CONNECTION DIAGRAMS





Pin	Description
L_7-L_0	8 bidirectional I/O ports with TRI-STATE®
G_3-G_0	4 bidirectional I/O ports
D_3-D_0	4 general purpose outputs
IN_3-IN_0	4 general purpose inputs (COP444L only)
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)

Pin	Description
SK	Logic-controlled clock (or general purpose output)
CKI	System oscillator input
CKO	System oscillator output (or general purpose input, RAM power supply, or SYNC input)
$\overline{RESET}$	System reset input
V_{CC}	Power supply
GND	Ground

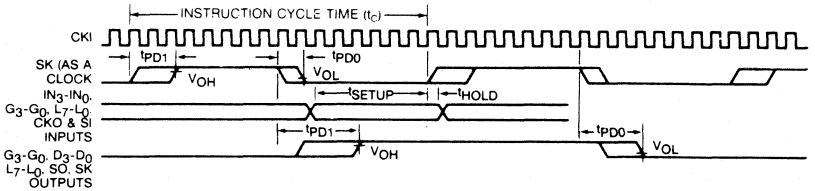


FIGURE 3 – INPUT/OUTPUT TIMING DIAGRAMS (CRYSTAL DIVIDE-BY-16 MODE)

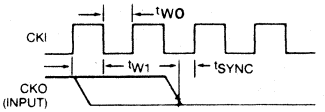


FIGURE 3a – SYNCHRONIZATION TIMING

FUNCTIONAL DESCRIPTION

A block diagram of the ETL9444 is given in Figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2 volts). When a bit is reset, it is a logic "0" (less than 0.8 volts).

All functional references to the ETL9444/L9445 also apply to the ETL9344/L9345.

Program Memory

Program Memory consists of a 2048 byte ROM. As can be seen by an examination of the ETL9444/L9445 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID, and LQID instructions, ROM must often be thought of as being organized into 32 pages of 64 words each.

ROM addressing is accomplished by a 11-bit PC register. Its binary value selects one of the 2048 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value. Three levels of subroutine nesting are implemented by the 11-bit subroutine save registers, SA, SB, and SC; providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

Data Memory

Data memory consists of a 512-bit RAM, organized as 8 data registers of 16 4-bit digits. RAM addressing is implemented by a 7-bit B register whose upper 3 bits (Br) select 1 of 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the 7-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

Internal Logic

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch data, to input 4 bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing its results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below.)

Four general-purpose inputs, IN_3-IN_0, are provided.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. The D outputs can be directly connected to the digits of a multiplexed LED display.

The G register contents are outputs to 4 general-purpose bidirectional I/O ports. G I/O ports can be directly connected to the digits of a multiplexed LED display.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction.)

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa-Sg and decimal point segments of the display.

The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register. (See EN register description, below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/parallel-out shift registers.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0)

1. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") ocurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. (See 4 below.) The SK output becomes a logic-controlled clock.
2. With EN_1 set the IN_1 input is enabled as an interrupt input. Immediately following an interrupt, EN_1 is reset to disable further interrupts.

3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high-impedance input state.
4. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0". The table below provides a summary of the modes associated with EN_3 and EN_0.

Enable Register Modes — Bits EN_3 and EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = CLOCK If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = CLOCK If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

Interrupt

The following features are associated with the IN_1 interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack, pushing in turn the contents of the other subroutine-save registers to the next lower level (PC + 1 → SA → SB → SC). Any previous contents of SC are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN_1 is reset.

b. An interrupt will be acknowledged only after the following conditions are met:
   1. EN_1 has been set.
   2. A low-going pulse ("1" to "0") at least two instruction cycles wide occurs on the IN_1 input.
   3. A currently executing instruction has been completed.
   4. All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.

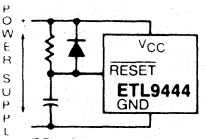
c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the *end* of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. *At this time*, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines and LQID instructions should not be nested within the interrupt service routine, since their popping the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The first instruction of the interrupt routine at hex address 0FF must be a NOP.

e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

Initialization

The Reset Logic will initialize (clear) the device upon power-up if the power supply rise time is less than 1 ms and greater than 1 µs. If the power supply rise time is greater than 1 ms, the user use provide an external RC network and diode to the $\overline{RESET}$ pin as shown below. If the RC network is not used, the $\overline{RESET}$ pin must be pulled up to V_{CC} either by the internal load or by an external resistor (≥ 40 kΩ) to V_{CC}. The $\overline{RESET}$ pin is configured as a Schmitt trigger input. Initialization will occur whenever a logic "0" is applied to the $\overline{RESET}$ input, provided it stays low for at least three instruction cycle times.



RC = 5 x power supply Rise time (R = 40 k)

Power up clear circuit

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. *Data Memory (RAM) is not cleared upon initialization.* The first instruction at address 0 must be a CLRA.

Oscillator

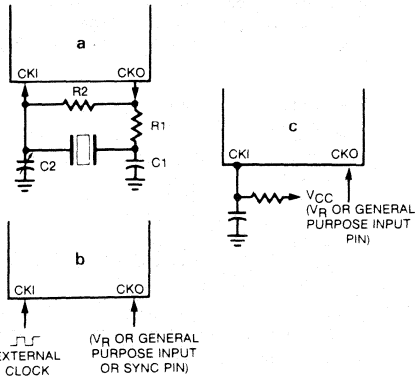
There are four basic clock oscillator configurations available as shown by Figure 4.

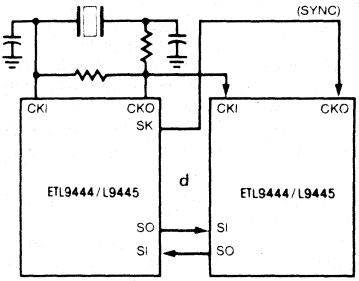
a. Crystal Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 32 (optional by 16 or 8).

b. External Oscillator. CKI is an external clock input signal. The external frequency is divided by 32 (optional by 16 or 8) to give the instruction cycle time. CKO is now available to be used as the RAM power supply (V_R), as a general purpose input, or as a SYNC input.

c. RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available as the RAM power supply (V_R) or as a general purpose input.

d. Externally Synchronized Oscillator. Intended for use in multi-COP systems, CKO is programmed to function as an input connected to the SK output of another COP chip operating at the same frequency (COP chip with L or C suffix) with CKI connected as shown. In this configuration, the SK output connected to CKO must provide a SYNC (instruction cycle) signal to CKO, thereby allowing synchronous data transfer between the COPs using only the SI and SO serial I/O pins in conjunction with the XAS instruction. Note that on power-up SK is automatically enabled as a SYNC output. (See Functional Description, Initialization, above.)





Crystal Oscillator

Crystal Value	Component Values			
	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)
455 kHz	4.7k	1M	220	220
2.097 MHz	1k	1M	30	6-36

RC Controlled Oscillator

R (kΩ)	C (pF)	Instruction Cycle Time (μs)
51	100	19 ± 15%
82	56	19 ± 13%

Note: 200 kΩ ≥ R ≥ 25 kΩ
360 pF ≥ C ≥ 50 pF

FIGURE 4 – ETL9444/L9445 OSCILLATOR

CKO Pin Options

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. As an option CKO can be a SYNC input as described above. As another option CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction. As another option, CKO can be a RAM power supply pin (V_R), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either option is appropriate in applications where the ETL9444/L9445 system timing configuration does not require use of the CKO pin.

I/O Options

ETL9444/L9445 outputs have the following optional configurations, illustrated in Figure 5 :

a. Standard — an enhancement mode device to ground in conjunction with a depletion-mode device to V_{CC}, compatible with LSTTL and CMOS input requirements. Available on SO, SK, and all D and G outputs.

b. Open-Drain — an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, and all D and G outputs.

c. Push-Pull — An enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.

d. Standard L — same as **a.**, but may be disabled. Available on L outputs only.

e. Open Drain L — same as **b.**, but may be disabled. Available on L outputs only.

f. LED Direct Drive — an enhancement-mode device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (See Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display. Available on L outputs only.

g. TRI-STATE® Push-Pull — an enhancement-mode device to ground and V_{CC}. These outputs are TRI-STATE outputs, allowing for connection of these outputs to a data bus shared by other bus drivers. Available on L outputs only.

ETL9444/L9445 inputs have the following optional configurations :

h. An on-chip depletion load device to V_{CC}.

i. A Hi-Z input which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT} curves are given in Figure 6 for each of these devices to allow the designer to effectively use these I/O configurations in designing a system.

The SO, SK outputs can be configured as shown in **a.**, **b.**, or **c.** The D and G outputs can be configured as shown in **a.** or **b.** Note that when inputting data to the G ports, the G outputs should be set to "1." The L outputs can be configured as in **d.**, **e.**, **f.** or **g.**

An important point to remember if using configuration **d.** or **f.** with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current (see Figure 6, device 2); however, when the L-lines are used as inputs, the disabled depletion device can *not* be relied on to source sufficient current to pull an input to logic "1".

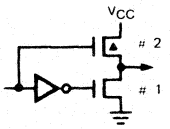
RAM Keep-Alive Option

Selecting CKO as the RAM power supply (V_R) allows the user to shut off the chip power supply (V_{CC}) and maintain data in the RAM.
To insure that RAM data integrity is maintained, the following conditions *must* be met:

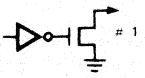
1. $\overline{\text{RESET}}$ must go low before V_{CC} goes low during power off; V_{CC} must go high before $\overline{\text{RESET}}$ goes high on power-up.
2. V_R must be within the operating range of the chip, and equal to $V_{CC} \pm 1$V during normal operation.
3. V_R must be $\geq$ 3.3V with V_{CC} off.

ETL9445

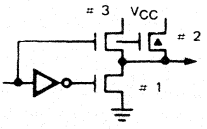
If the ETL9444 is bonded as a 24-pin device, it becomes the ETL9445, illustrated in Figure 2, ETL9444 Connection Diagrams. Note that the ETL9445 does not contain the four general purpose IN inputs (IN_3-IN_0). Use of this option precludes, of course, use of the IN options and the interrupt feature, which uses IN_1. All other options are available for the ETL9445.



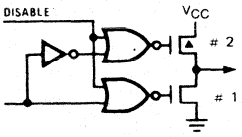
a. Standard Output



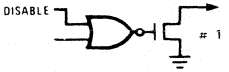
b. Open-Drain Output



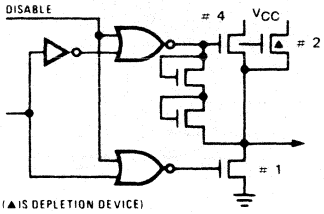
c. Push-Pull Output



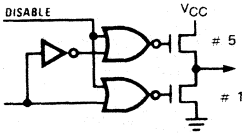
d. Standard L Output



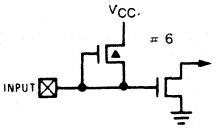
e. Open-Drain L Output



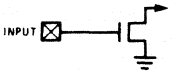
f. LED (L Output)



g. TRI-STATE®Push-Pull (L Output)



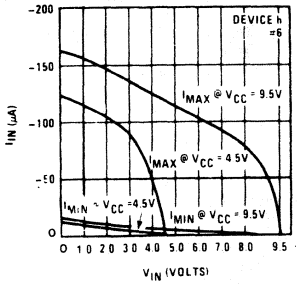
h. Input with Load



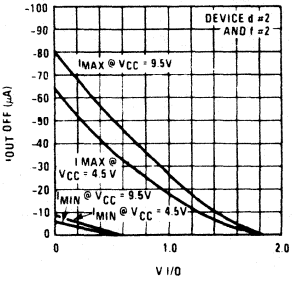
i. Hi-Z Input

FIGURE 5 – OUTPUT CONFIGURATIONS

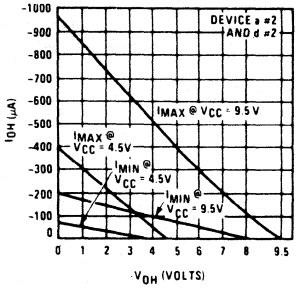
Current for Inputs with Load Device



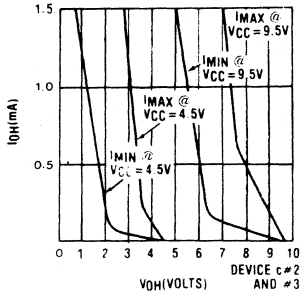
Input Current for L_0 through L_7 when Output Programmed Off by Software



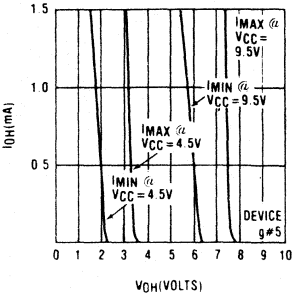
Source Current for Standard Output Configuration



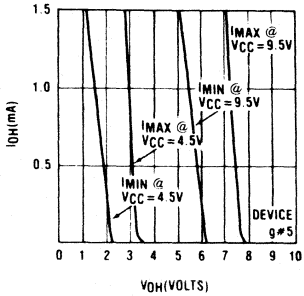
Source Current for SO and SK in Push-Pull Configuration



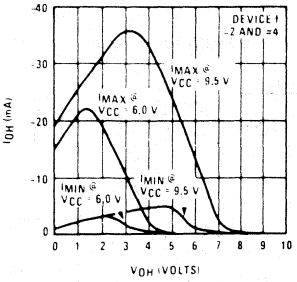
Source Current for L_0 through L_7 in TRI-STATE®Configuration (High Current Option)



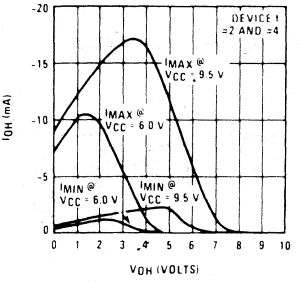
Source Current for L_0 through L_7 in TRI-STATE®Configuration (Low Current Option)



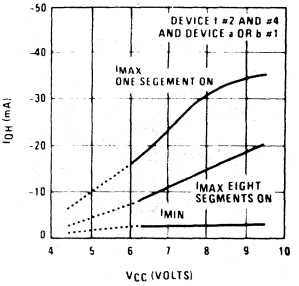
LED Output Source Current
(for High Current LED Option)



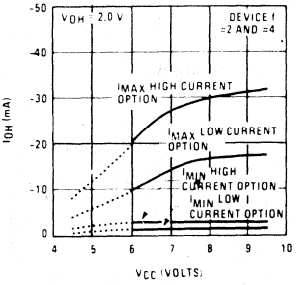
LED Output Source Current
(for Low Current LED Option)



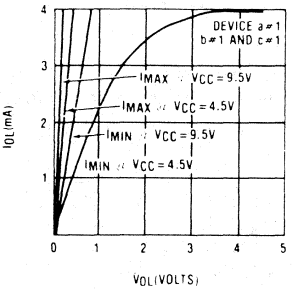
LED Output Direct Segment
Drive
High Current Options on L_0-L_7
Very High Current Options on
D_0-D_3 or G_0-G_3.



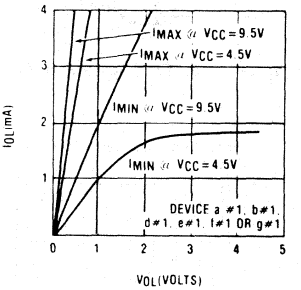
LED Output Direct Segment
Drive



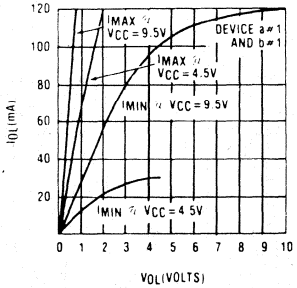
Output Sink Current for SO
and SK



Output Sink Current for L_0-L_7
and Standard Drive Option for
D_0-D_3 and G_0-G_3



Output Sink Current
G_0-G_3 and D_0-D_3 with Very
High Current Option



Output Sink Current for G_0-G_3
and D_0-D_3 (for High Current
Option)

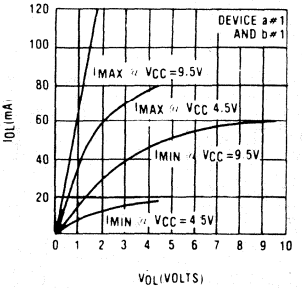
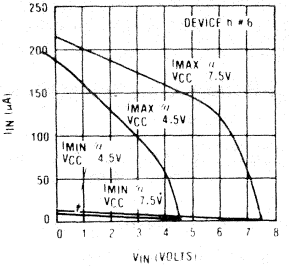
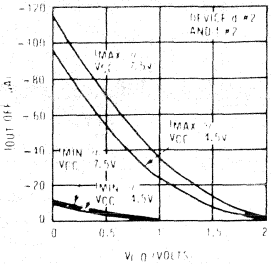


FIGURE 6a – ETL9444/L9445 INPUT/OUTPUT CHARACTERISTICS

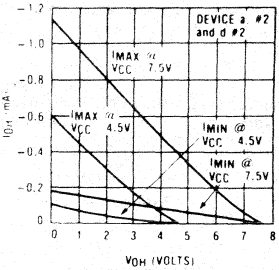
Input Current $IN_0 - IN_3$



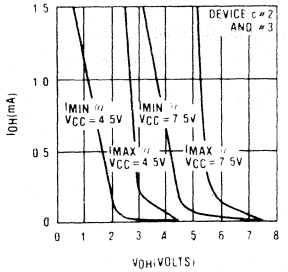
Input Current for L0-L7 when Output Programmed Off by Software



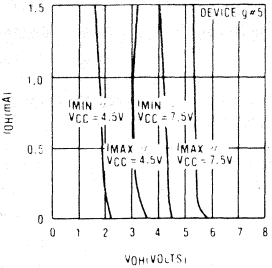
Source Current for Standard Output Configuration



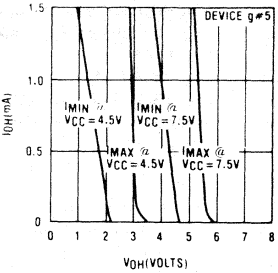
Source Current for SO and SK in Push-Pull Configuration



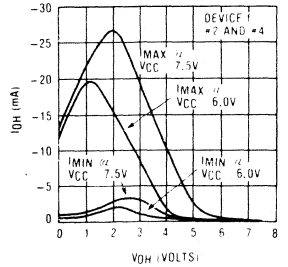
Source Current for L0-L7 in TRI-STATE® Configuration (High Current Option)



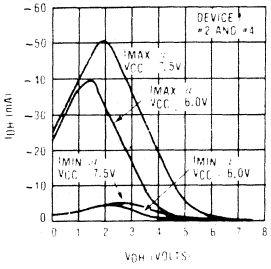
Source Current for L0-L7 in TRI-STATE® Configuration (Low Current Option)



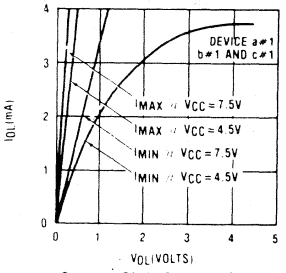
LED Output Source Current (for Low Current LED Option)



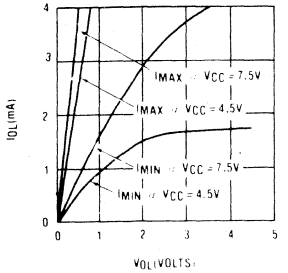
LED Output Source Current (for High Current LED Option)



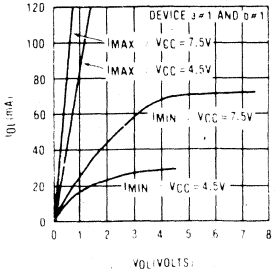
Output Sink Current for SO and SK



Output Sink Current for $L_0 - L_7$ and Standard Drive Option for $D_0 - D_3$ and $G_0 - G$



Output Sink Current $G_0 - G_3$ and $D_0 - D_3$ with Very High Current Option



Output Sink Current for $G_0 - G_3$ and $D_0 - D_3$ (for High Current Option)

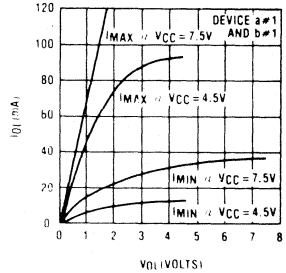


FIGURE 6b – ETL9344/L9345 INPUT/OUTPUT CHARACTERISTICS

ETL9444/L9445,ETL9344/L9345 Instruction Set

Table 1 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 2 provides the mnemonic, operand, machine code, data flow, skip conditions, and description associated with each instruction in the ETL9444/L9445 instruction set.

TABLE 1 – ETL9444/L9445 ETL9344/L9345 INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	7-bit RAM Address Register
Br	Upper 3 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
IL	Two 1-bit latches associated with the IN_3 or IN_0 inputs
IN	4-bit Input Port
L	8-bit TRI-STATE® I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
PC	11-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	11-bit Subroutine Save Register A
SB	11-bit Subroutine Save Register B
SC	11-bit Subroutine Save Register C
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0-15 binary (RAM Digit Select)
r	3-bit Operand Field, 0-7 binary (RAM Register Select)
a	11-bit Operand Field, 0-2047 binary (ROM Address)
y	4-bit Operand Field, 0-15 binary (Immediate Data)
RAM(s)	Contents of RAM location addressed by s
ROM(t)	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
—	Minus
⟶	Replaces
⟷	Is exchanged with
=	Is equal to
$\overline{A}$	The one's complement of A
⊕	Exclusive-OR
:	Range of values

TABLE 2 – ETL9444/L9445 INSTRUCTION SET

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011|0000	A + C + RAM(B) → A Carry → C	Carry	Add with Carry. Skip on Carry
ADD		31	0011|0001	A + RAM(B) → A	None	Add RAM to A
ADT		4A	0100|1010	A + 10_{10} → A	None	Add Ten to A
AISC	y	5-	0101| y	A + y → A	Carry	Add Immediate. Skip on Carry (y ≠ 0)
CASC		10	0001|0000	$\overline{A}$ + RAM(B) + C → A Carry → C	Carry	Complement and Add with Carry. Skip on Carry
CLRA		00	0000|0000	0 → A	None	Clear A
COMP		40	0100|0000	$\overline{A}$ → A	None	Ones complement of A to A
NOP		44	0100|0100	None	None	No Operation
RC		32	0011|0010	"0" → C	None	Reset C
SC		22	0010|0010	"1" → C	None	Set C
XOR		02	0000|0010	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1111|1111	ROM ($PC_{10:8}$, A,M) → $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6- --	0110|0|$a_{10:8}$ $a_{7:0}$	a → PC	None	Jump
JP	a	-- or -- all other pages)	1| $a_{6:0}$ (pages 2,3 only) 11| $a_{5:0}$	a → $PC_{6:0}$ a → $PC_{5:0}$	None	Jump within Page (Note 4)
JSRP	a	--	10| $a_{5:0}$	PC + 1 → SA → SB → SC 00010 → $PC_{10:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6- --	0110|1|$a_{10:8}$ $a_{7:0}$	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
RET		48	0100|1000	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0100|1001	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip

TABLE 2 – ETL9444/L9445 INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33 3C	0011|0011 0011|1100	$A \rightarrow Q_{7\,4}$ $RAM(B) \rightarrow Q_{3\,0}$	None	Copy A, RAM to Q
COMA		33 2C	0011|0011 0010|1100	$Q_{7\,4} \rightarrow RAM(B)$ $Q_{3\,0} \rightarrow A$	None	Copy Q to RAM, A
LD	r	-5	00| r |0101 (r = 0:3)	$RAM(B) \rightarrow A$ $Br \oplus r \rightarrow Br$	None	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	23 --	0010|0011 0| r | d	$RAM(r,d) \rightarrow A$	None	Load A with RAM pointed to directly by r,d
LQID		BF	1011|1111	$ROM(PC_{10\,8}.A.M) \rightarrow Q$ $SB \rightarrow SC$	None	Load Q Indirect (Note 3)
RMB	0 1 2 3	4C 45 42 43	0100|1100 0100|0101 0100|0010 0100|0011	$0 \rightarrow RAM(B)_0$ $0 \rightarrow RAM(B)_1$ $0 \rightarrow RAM(B)_2$ $0 \rightarrow RAM(B)_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	0100|1101 0100|1101 0100|0110 0100|1011	$1 \rightarrow RAM(B)_0$ $1 \rightarrow RAM(B)_1$ $1 \rightarrow RAM(B)_2$ $1 \rightarrow RAM(B)_3$	None	Set RAM Bit
STII	y	7-	0111| y	$y \rightarrow RAM(B)$ $Bd + 1 \rightarrow Bd$	None	Store Memory Immediate and Increment Bd
X	r	-6	00| r |0110 (r = 0:3)	$RAM(B) \leftrightarrow A$ $Br \oplus r \rightarrow Br$	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23 --	0010|0011 1| r | d	$RAM(r,d) \leftrightarrow A$	None	Exchange A with RAM pointed to directly by r,d
XDS	r	-7	00| r |0111 (r = 0:3)	$RAM(B) \leftrightarrow A$ $Bd - 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	-4	00| r |0100 (r = 0:3)	$RAM(B) \leftrightarrow A$ $Bd + 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101|0000	$A \rightarrow Bd$	None	Copy A to Bd
CBA		4E	0100|1110	$Bd \rightarrow A$	None	Copy Bd to A
LBI	r,d	-- 33 --	00| r |(d - 1) (r = 0:3, d = 0, 9:15) or 0011|0011 1| r | d (any r, any d)	r,d → B	Skip until not a LBI	Load B Immediate with r,d (Note 6)
LEI	y	33 6-	0011|0001 0110| y	$y \rightarrow EN$	None	Load EN Immediate (Note 7)
XABR		12	0001|0010	$A \leftrightarrow Br\ (0 \rightarrow A_3)$	None	Exchange A with Br

TABLE 2 – ETL9444/L9445 INSTRUCTION SET (continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TEST INSTRUCTIONS						
SKC		20	0 0 1 0 | 0 0 0 0		C = "1"	Skip if C is True
SKE		21	0 0 1 0 | 0 0 0 1		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0 0 1 1 | 0 0 1 1 0 0 1 0 | 0 0 0 1		$G_{3:0}$ = 0	Skip if G is Zero (all 4 bits)
SKGBZ		33	0 0 1 1 | 0 0 1 1	1st byte		Skip if G Bit is Zero
	0	01	0 0 0 0 | 0 0 0 1	2nd byte	G_0 = 0	
	1	11	0 0 0 1 | 0 0 0 1		G_1 = 0	
	2	03	0 0 0 0 | 0 0 1 1		G_2 = 0	
	3	13	0 0 0 1 | 0 0 1 1		G_3 = 0	
SKMBZ	0	01	0 0 0 0 | 0 0 0 1		$RAM(B)_0$ = 0	Skip if RAM Bit is Zero
	1	11	0 0 0 1 | 0 0 0 1		$RAM(B)_1$ = 0	
	2	03	0 0 0 0 | 0 0 1 1		$RAM(B)_2$ = 0	
	3	13	0 0 0 1 | 0 0 1 1		$RAM(B)_3$ = 0	
SKT		41	0 1 0 0 | 0 0 0 1		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	0 0 1 1 | 0 0 1 1 0 0 1 0 | 1 0 1 0	G → A	None	Input G Ports to A
ININ		33 28	0 0 1 1 | 0 0 1 1 0 0 1 0 | 1 0 0 0	IN → A	None	Input IN Inputs to A (Note 2)
INIL		33 29	0 0 1 1 | 0 0 1 1 0 0 1 0 | 1 0 0 1	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (Note 3)
INL		33 2E	0 0 1 1 | 0 0 1 1 0 0 1 0 | 1 1 1 0	$L_{7:4}$ · RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM A
OBD		33 3E	0 0 1 1 | 0 0 1 1 0 0 1 1 | 1 1 1 0	Bd → D	None	Output Bd to D Outputs
OGI	y	33 5–	0 0 1 1 | 0 0 1 1 0 1 0 1 | y	y → G	None	Output to G Ports Immediate
OMG		33 3A	0 0 1 1 | 0 0 1 1 0 0 1 1 | 1 0 1 0	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0 1 0 0 | 1 1 1 1	A ←→ SIO, C → SKL	None	Exchange A with SIO (Note 3)

Note 1 : All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2 : The ININ instruction is not available on the 24-pin ETL9445 or ETL9345 since these devices do not contain the IN inputs.

Note 3 : For additional information on the operation of the XAS, JID, LQUID, INIL, and SKT instructions, see below.

Note 4 : The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5 : A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6 : LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14 or 15. The machine code for the lower 4 bits equals the binary value of the "d" data *minus 1*, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8(1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 7 : Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register).

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing ETL9444/L9445 programs.

XAS Instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register, above.) If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM addressed by the 11-bit word, $PC_{10:8}$ A, M. PC_{10}, PC_9 and PC_8 are not affected by this instruction.

Note that JID requires 2 instruction cycles to execute.

INIL Instruction

INIL (Input IL Latches to A) inputs 2 latches, IL_3 and IL_0 (see Figure 7) and CKO into A. The IL_3 and IL_0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN_3 and IN_0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs IL_3 and IL_0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN_3 and IN_0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A "0" is always placed in A1 upon the execution of an INIL. The general purpose inputs IN_3-IN_0 are input to A upon execution of an ININ instruction. (See Table 2, ININ instruction.) INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction.

Note : IL latches are not cleared on reset : IL_3 and IL_0 *not* input on ETL9444/L9445.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC_{10}, PC_9, PC_8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB →SC) and replaces the least significant 8 bits of PC as follows: A — $PC_{7:4}$, RAM(B) → $PC_{3:0}$, leaving PC_{10}, PC_9 and PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA →PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the contents of SB are placed in SC (SB → SC). Note that LQID takes two instruction cycle times to execute.

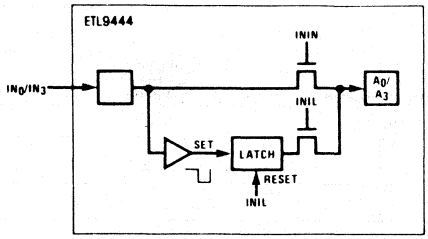


FIGURE 7 – INIL HARDWARE IMPLEMENTATION

SKT Instruction

The SKT (Skip On Timer) instruction tests the state of an internal 10-bit time-base counter. This counter divides the instruction cycle clock frequency by 1024 and provides a latched indication of counter overflow. The SKT instruction tests this latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction, therefore, allow the ETL9344/L9345 to generate its own time-base for real-time processing rather than relying on an external input signal.

For example, using a 2.097 MHz crystal as the time-base to the clock generator, the instruction cycle clock frequency will be 65 kHz (crystal frequency ÷ 32) and the binary counter output pulse frequency will be 64 Hz. For time-of-day or similar real-time processing, the SKT instruction can call a routine which increments a "seconds" counter every 64 ticks.

Instruction Set Notes

a. The first word of a ETL9444/L9445 program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths except JID and LQID take the same number of cycle times whether instructions are skipped or executed. JID and LQID instructions take 2 cycles if executed and 1 cycle if skipped.

c. The ROM is organized into 32 pages of 64 words each. The Program Counter is an 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: a JP located in the last work of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3, 7, 11, 15, 19, 23, or 27 will access data in the next group of four pages.

OPTION LIST

The ETL9444/L9445 mask-programmable options are assigned numbers which correspond with the ETL9444 pins.

The following is a list of ETL9444 options. When specifying ETL9445 chip, Options 9, 10, 19, and 20 must all be set to zero. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Output
- = 0: clock generator output to crystal/resonator (0 not allowable value if option 3 = 3)
- = 1: pin is RAM power supply (V_R) input
- = 2: general purpose input, load device to V_{CC}
- = 3: general purpose input, Hi-Z
- = 4: multi-COP SYNC input (CKI ÷ 32, CKI ÷ 16)
- = 5: multi-COP SYNC input (CKI ÷ 8)

Option 3: CKI Input
- = 0: oscillator input divided by 32 (2 MHz max.)
- = 1: oscillator input divided by 16 (1 MHz max.)
- = 2: oscillator input divided by 8 (500 kHz max.)
- = 3: single-pin RC controlled oscillator divided by 4
- = 4: oscillator input divided by 4 (Schmitt)

Option 4: $\overline{\text{RESET}}$ Input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 5: L_7 Driver
- = 0: Standard output
- = 1: Open-drain output
- = 2: High current LED direct segment drive output
- = 3: High current TRI-STATE® push-pull output
- = 4: Low-current LED direct segment drive output
- = 5: Low-current TRI-STATE® push-pull output

Option 6: L_6 Driver
same as Option 5

Option 7: L_5 Driver
same as Option 5

Option 8: L_4 Driver
same as Option 5

Option 9: IN_1 Input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 10: IN_2 Input
same as Option 9

Option 11: V_{CC} pin
- = 0: 4.5V to 6.3V operation
- = 1: 4.5V to 9.5V operation

Option 12: L_3 Driver
same as Option 5

Option 14: L_2 Driver
same as Option 5

Option 14: L_1 Driver
same as Option 5

Option 15: L_0 Driver
same as Option 5

Option 16: SI Input
same as Option 9

Option 17: SO Driver
- = 0: standard output
- = 1: open-drain output
- = 2: push-pull output

Option 18: SK Driver
same as Option 17

Option 19: IN_0 Input
same as Option 9

Option 20: IN_3 Input
same as Option 9

Option 21: G_0 I/O Port
- = 0: very-high current standard output
- = 1: very-high current open-drain output
- = 2: high current standard output
- = 3: high current open-drain output
- = 4: standard LSTTL output (fanout = 1)
- = 5: open-drain LSTTL output (fanout = 1)

Option 22: G_1 I/O Port
same as Option 21

Option 23: G_2 I/O Port
same as Option 21

Option 24: G_3 I/O Port
same as Option 21

Option 25: D_3 Output
same as Option 21

Option 26: D_2 Output
same as Option 21

Option 27: D_1 Output
same as Option 21

Option 28: D_0 Output
same as Option 21

Option 29: L Input Levels
- = 0: standard TTL input levels ("0" = 0.8V, "1" = 2.0V)
- = 1: higher voltage input levels ("0" = 1.2V, "1" = 3.6V)

Option 30: IN Input Levels
same as Option 29

Option 31: G Input Levels
same as Option 29

Option 32: SI Input Levels
same as Option 29

Option 33: RESET Input
- = 0: Schmitt trigger input
- = 1: standard TTL input levels
- = 2: higher voltage input levels

Option 34: CKO Input Levels (CKO = input Option 2 = 2,3)
same as Option 29

Option 35 COP Bonding
- = 0: ETL9444 (28-pin device)
- = 1: ETL9445 (24-pin device)
- = 2: both 28 and 24-pin versions

TEST MODE (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed ETL9444. With SO forced to logic "1", two test modes are provided, depending upon the value of SI :

a. RAM and Internal Logic Test Mode (SI = 1)

b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user ; they are intended for manufacturing test only.

APPLICATION EXAMPLE : ETL9444 General Controller

Figure 8 shows and interconnect diagram for a ETL9444 used as a general controller. Operation of the system is as follows :

1. The L_7-L_0 outputs are configured as LED Direct Drive outputs, allowing direct connection to the segments of the display.
2. The D_3-D_0 outputs drive the digits of the multiplexed display directly and scan the columns of the 4 x 4 keyboard matrix.
3. The IN_3-IN_0 inputs are used to input the 4 rows of the keyboard matrix. Reading the IN lines in conjunction with the current value of the D outputs allows detection, debouncing, and decoding of any one of the 16 keyswitches.
4. CKI is configured as a single-pin oscillator input allowing system timing to be controlled by a single-pin RC network. CKO is therefore available for use as a general-purpose input.
5. SI is selected as the input to a binary counter input. With SIO used as a binary counter, SO and SK can be used as general purpose outputs.
6. The 4 bidirectional G I/O ports (G_3-G_0) are available for use as required by the user's application.
7. Normal reset operation is selected.

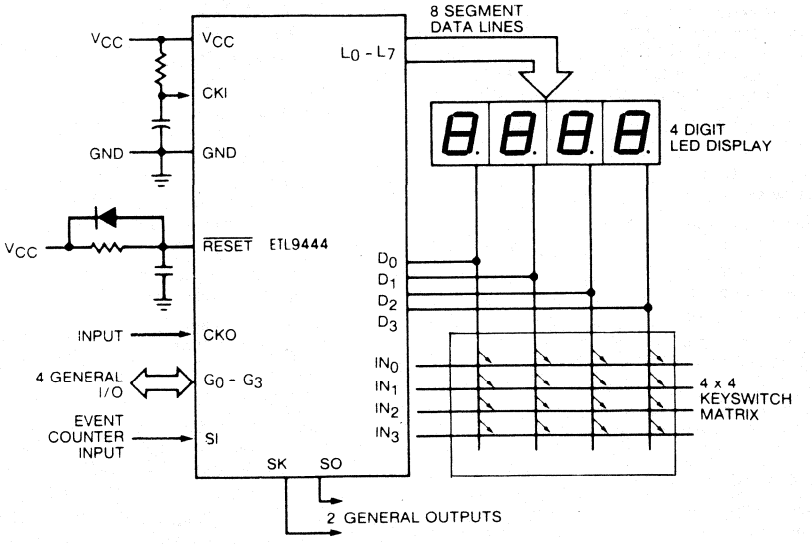


FIGURE 8 – ETL9444 KEYBOARD/DISPLAY INTERFACE

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PHYSICAL DIMENSIONS

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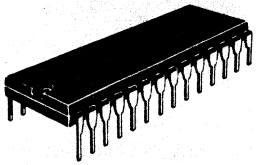
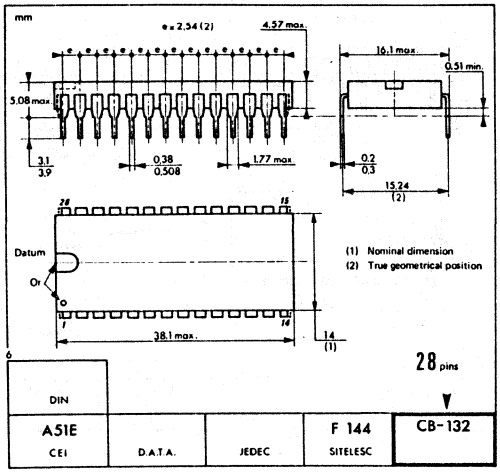


N SUFFIX
PLASTIC PACKAGE



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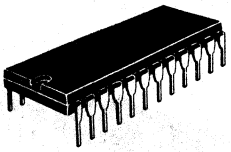

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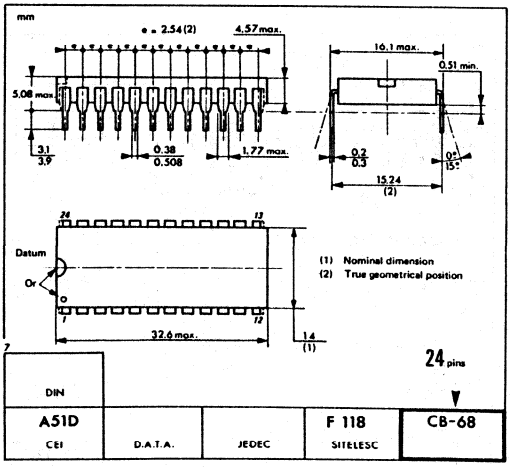

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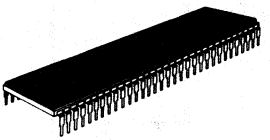

PLASTIC PACKAGE

GENERAL DESCRIPTION

The TS94104 ROMless N-channel microcontroller is a member of the TS94100 family, fabricated using N-channel, silicon gate XMOS technology.
The TS94104 contains the internal logic of the TS94100 microcontroller family except ROM.

This internal logic is identical to the TS94144 except that the ROM is removed and extra pins are added to output the ROM address and to input the ROM data. The TS94104 can be configured, by means of external pins, to function as a TS94120 or TS94144. Pins have been added to allow the user to select the various functional options that are available on TS94100 family. The TS94104 is primarily entended for a program development and debug for the TS94120 and TS94144 devices prior to masking the final part.
The TS94104 is also appropriate in low volume applications or when the program might be evolutive.

FEATURES

- Accurate emulation of the TS94100 family.
- Powerful instruction set (52 instructions).
- Addresses 2K x 8 external ROM.
- 128 x 4 RAM.
- Interrupt sources: external, internal counter or dual-time peripheral.
- 3-level subroutine stack.
- 4 μs instruction cycle.
- Single supply operation (4.5 V - 5.5 V).
- Low-current drain (15 mA max.).
- Programmable read/write 8 bit internal counter.
- Internal shift register with serial I/O.
- Watch-dog feature.
- Dual timer peripheral for complex waveforms generation and measurements.
- General purpose and tri-state outputs.
- TTL compatible.
- Direct drive of LED digit and segment line.
- Direct drive of TRIAC.
- Extended temperature (— 40°C to + 85°C) available.
- Software compatible with the other member of ET9400, TS94100 families.

PIN ASSIGNMENT

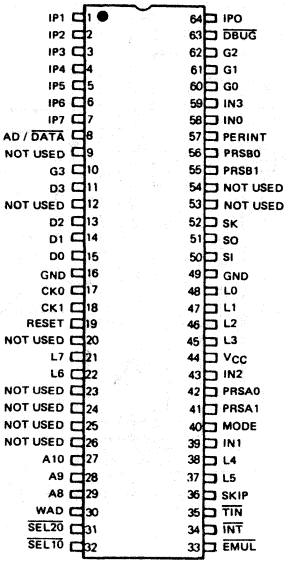

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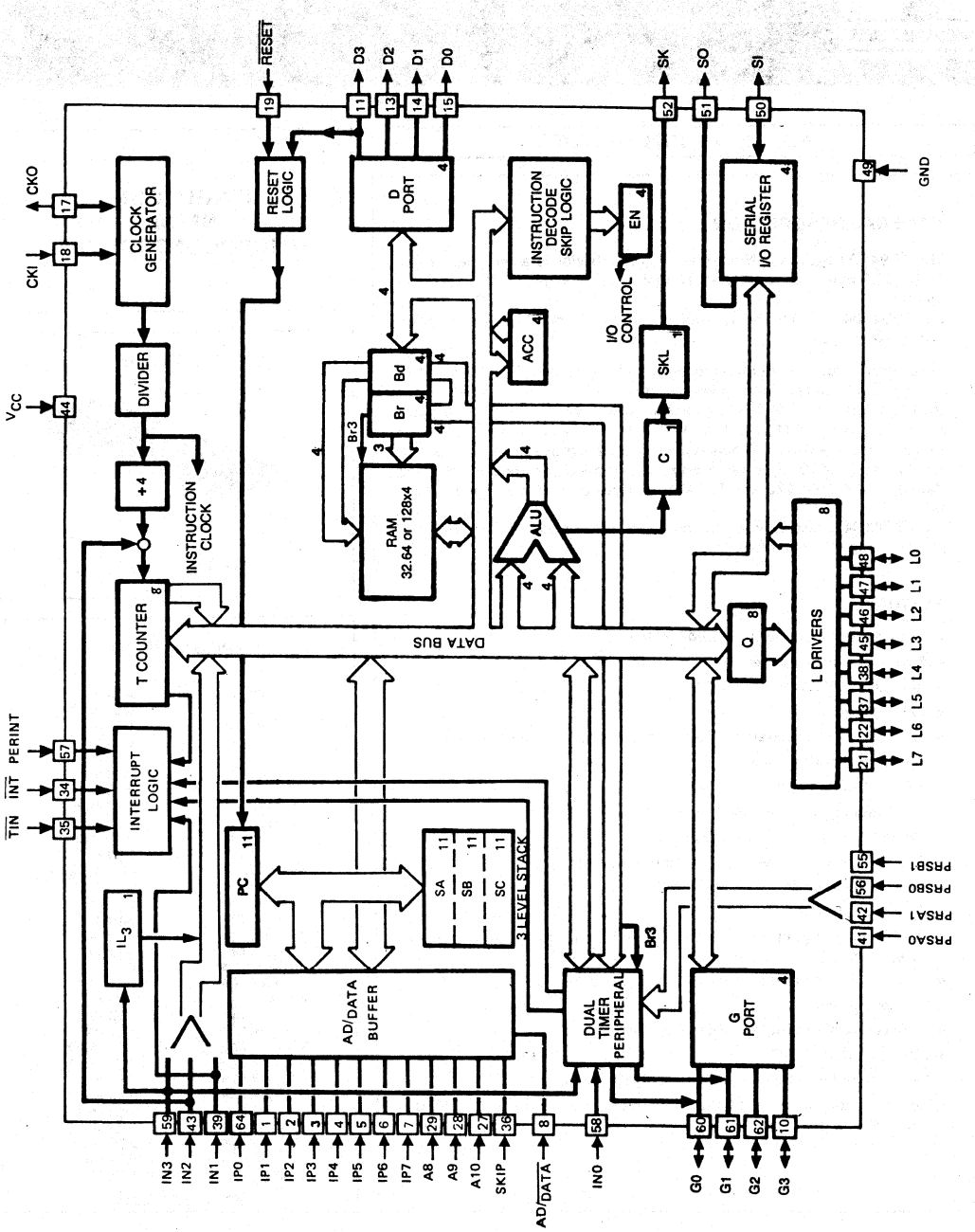
FIGURE 1 : BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The internal architecture is shown in Figure 1. Data paths are illustred in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" when it is reset, it is a logic "0".

PROGRAM MEMORY

Program memory consists of a 2K byte external ROM memory (typically an EPROM).

These bytes of ROM may be program instructions, constants or ROM addressing data.

ROM addressing is accomplished by a 11-bit PC register which selects one of the 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value.

Three levels of subroutine nesting are implemented by a three levels deep stack. Each subroutine call (or interrupt) pushes the next PC address into the stack. Each return pops the stack back into the PC register.

DATA MEMORY

Data memory consists of a 512-bit RAM organized as 8 data registers of 16 x 4-bit digits. RAM addressing is implemented by a 7-bit B register whose upper 3 bits (Br) select 1 or 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register.

To emulate with accuracy the TS94120, the size of the RAM available to the user may be reduced by using $\overline{\text{SEL10}}$ and $\overline{\text{SEL20}}$ pins to obtain the following configurations:

— a 128 digits RAM is available, thus emulating an TS94144,

— the user RAM is physically halved to 64 digits (256 bits) thus emulating an TS94120,

The upper most bit of Br (Br3) register is only used to select between the RAM and the peripheral.

While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with the A register (accumulator), they may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the immediate operand field of these instructions.

The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

INTERNAL LOGIC

A 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd field of the B register, to load and input 4 bits out of the 8-bits Q latch, to input 4 bits out of a ROM word, to input G or IN ports, and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing the results in A with eventually a carry bit in the 1-bit C register. The C register in conjunction with the XAS instruction and the EN register is also related to the SK output control.

The 8-bit T counter is a binary up counter which can be loaded to and from M and A using CAMT and CTMA instructions. This counter may be running in two modes depending on $\overline{\text{TIN}}$: as a timer or as an external event counter. When the T counter overflows, an overflow flag will be set (see SKT instruction below). Note that T counter is cleared on reset. A functional block diagram of the timer/counter is illustrated in Figure 4.

3 general-purpose inputs, IN3-IN1, are provided. Note that IN3 can be considered as a dual-timer input. IN0 is an analog input connected to an internal comparator.

The D register provides, 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. D3 is also used as the watchdog input when the watchdog option is selected.

The G register is a 2-bit general-purpose bidirectional I/O port (G3-G2). G0-G1 are the outputs of the peripheral and can also be used as general-purpose inputs.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Q register contents are transferred to the L I/O ports when the L drivers are enabled under program control (see LEI instruction).

L driver, when enabled, outputs the content of latched Q data to the L I/O ports. Contents of L may be read directly into A and M.

The SIO register is a 4-bit serial-in/serial-out shift register for the serial out. SIO content can be exchanged with A.

The XAS instruction copies C into the SKL Latch.

When SKL = 1, SK is a clock output
When SKL = 0, SK outputs a value depending upon the contents of EN0 and EN3.

The « EN register » is an internal 4-bit register loaded under program control by the LEI instruction. Each bit selects or inhibits the dedicated feature associated with each bit of the EN register (EN3-EN0).

- With EN1 set, the CPU interrupt is enabled.
- With EN2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN2 disables the L drivers, setting the L port as high impedance inputs.
- EN3, in conjunction with EN0, affects the SO and the SK outputs (see table 1).
  - — When EN3 = 0, SO outputs EN0 and SK outputs the clock anded with the content of the SKL latch,
  - — when EN3 = 1, SO is the output of the serial shifter, while SK outputs the clock (if SKL = 1) or the EN0 bit (if SKL = 0).

  Even when SO is disabled (as SIO output), data goes on shifting through SIO and can be exchanged with A via an XAS.

TABLE 1. ENABLE REGISTER MODES - BITS EN0 AND EN3

EN3	EN0	SO	SK after XAS
0	0	0	If SKL = 1, SK = Clock If SKL = 0, SK = 0
0	1	1	
1	0	Serial out	If SKL = 1, SK = Clock If SKL = 0, SK = EN0
1	1	Serial out	

INTERRUPT SOURCES

There are 3 possible interrupt sources (see Figure 4).

- Counter overflow or external interrupt ($\overline{INT}$ pin). External interrupt is triggered on the falling edge of a zero pulse. The zero pulse must be at least 2 instruction cycles wide on the external pin IN1 (or internal counter overflow).
- 2 peripheral interrupt sources (see peripheral description).

Each interrupt source has its own enable bit (EN1 for the CPU interrupt, ENA and ENB for the peripheral interrupts) and its own flag (F1 for the CPU interrupt, FA and FB for the peripheral interrupts, see Figure 15). An interrupt is enabled when its associated enable bit is set. Its associated flag is set when the interrupt is requested (for example, timer overflow for the CPU interrupt).

Note that the FA, FB, ENA, ENB bits, but also the F1 bit are implemented in the peripheral registers.

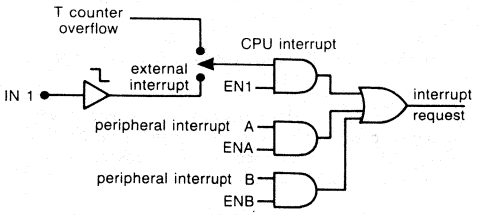


FIGURE 2: INTERRUPT BLOCK DIAGRAM

The following features are associated with interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

- The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack:
  PC + 1 → SA → SB → SC. Any previous contents of SC is lost. The program counter is set to hex address 0FF (the last word of page 3) and all incoming interrupts are disabled without clearing the enable bits.

- An interrupt will be acknowledged only after the following conditions:
  - — An interrupt request has been generated.
  - — The associated enable bit is set.
  - — A currently executing instruction has been completed.
  - — All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed).

- Upon acknowledgement of an interrupt, bit Br3 of the B register is saved (and later restored upon « popping » off the stack by a RET instruction), then Br3 is cleared, allowing the user to begin his interrupt subroutine in the RAM space addressing.

- Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon « popping » off the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the end of the interrupt routine, a RET instruction is executed to « pop » the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines should not be nested within the interrupt servicing routine since « popping » the stack will enable any previously saved main program skips, interfering with the orderly execution sequence of the interrupt routine.

- The first instruction at hex address 0FF must be a NOP.

- **When an interrupt is acknowledged, other interrupt sources are internally disabled until the end of the interrupt servicing routine.**

RESET

The RESET pin is configured as a Schmitt trigger input. If not used it should be connected to Vcc. Initialization will occur whenever a logic « 0 » is applied to the RESET input for at least three instruction cycles.

Upon initialization, the PC register is cleared to 0 (ROM address 0) the A, B, C, D, EN, G2-G3, T counter, IL latches registers and the peripheral registers CRA, CRB, IMR are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA. RC must be greather than 5 times power supply rise time.

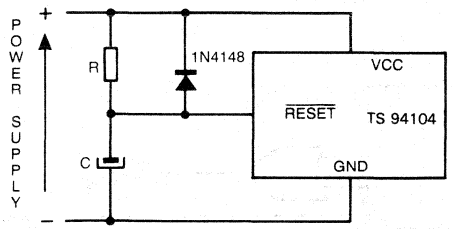


FIGURE 3: POWER-UP CLEAR CIRCUIT

T COUNTER

There are two modes selected by TIN pin.

— $\overline{TIN}$ = 0: TIME BASE COUNTER
Instruction cycle clock (CKI divided by 10) is divided by 4 x 256 = 1024 (see figure 6). For example, using a 1.0 MHz crystal, therefore getting a 10 μs instruction cycle period, TS94104 allows accurate timings between 10 μs* (1 count) and 10.24 ms (1024 counts). Longer timings can be achieved with software control (count of multiple overflows).

— $\overline{TIN}$ = 1: EXTERNAL EVENT COUNTER
Any pulse lasting more than 2 instructions cycle on IN2 will increment the T counter (on falling edge).

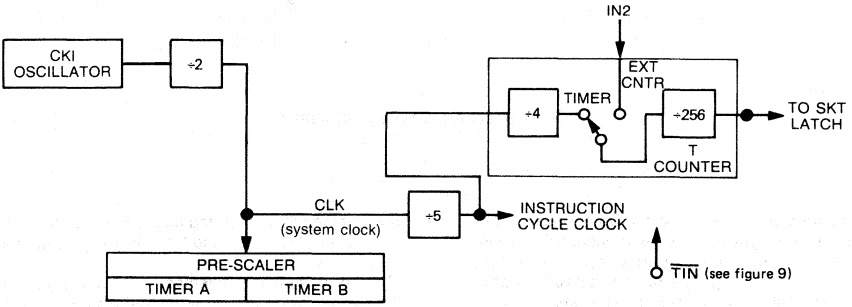


FIGURE 4: CLOCK AND CPU COUNTER BLOCK DIAGRAM

OSCILLATOR

CKI is configured as a TTL compatible external clock input (equivalent to option 3.2 for a TS94100). Instruction cycle time is the external frequency divided by 10. (equivalent to option 4.1 for a TS94100).

WATCHDOG

Watchdog mode is selected with WAD input

WAD = 0 NO WATCHDOG
WAD = 1 D3 IS THE WATCHDOG INPUT

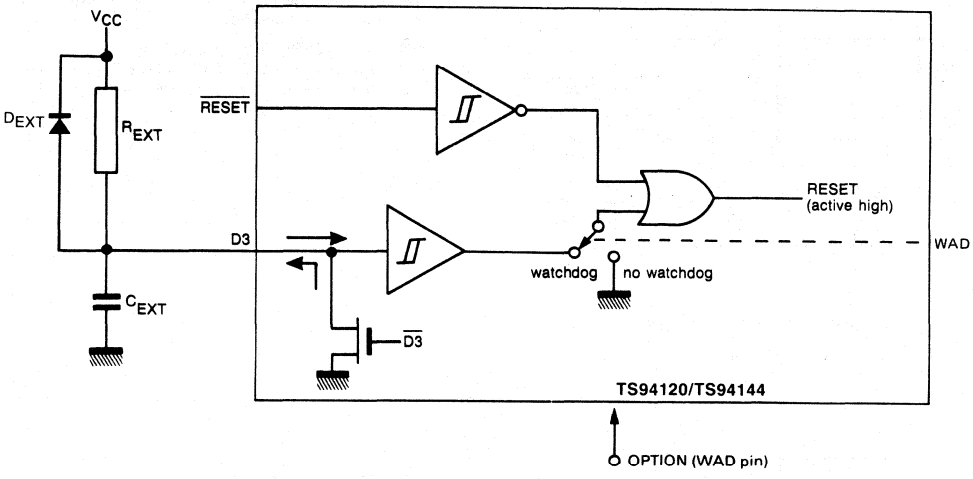


FIGURE 5: D3 AS WATCHDOG INPUT

In the watchdog mode, a « 1 » on pin D3 activates the internal reset (see Figure 5). The user needs only to connect a pull-up resistor and a capacitor on D3, and insert a watchdog loop in his program. This software loop will periodically outputs a « 0 » on D3 when the program is normally executed. When the microcontroller is trapped in another loop, the watchdog loop is not any more efficient and C_{ext} is charged up to Vcc, thus triggering the chip reset.

Open-drain option is selected on D3. The $R_{EXT} \times C_{EXT}$ time constant on D3 is related to the period of the software watchdog loop. D_{EXT} speeds up the C_{EXT} discharge time during power off.

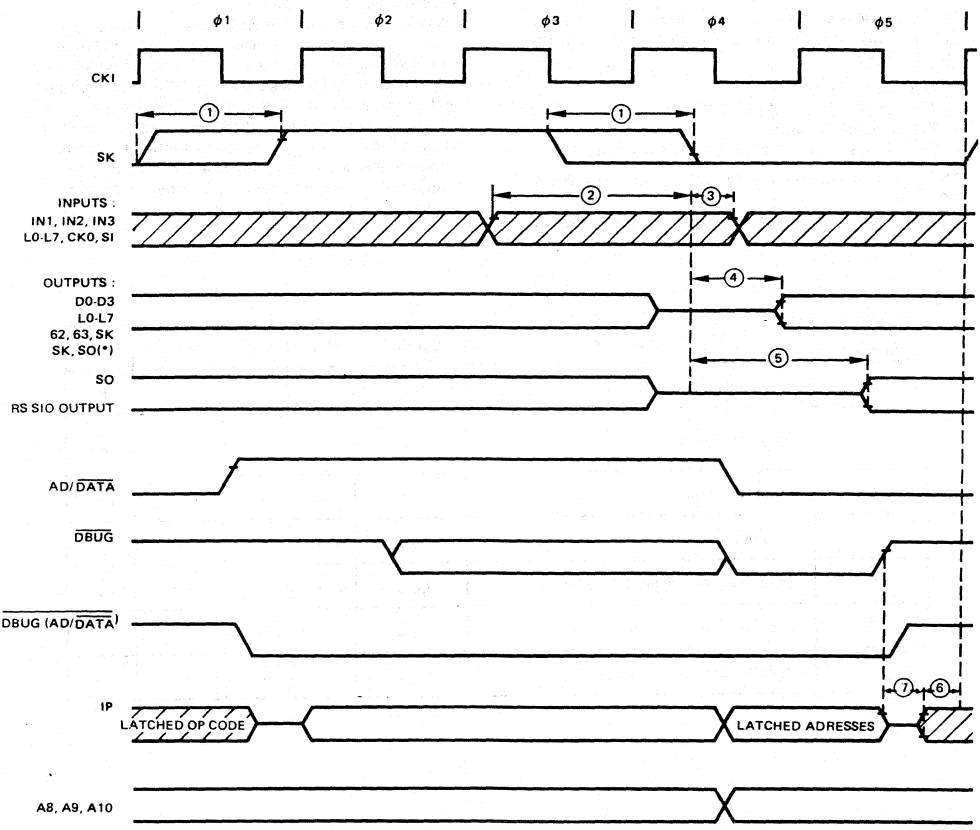
EXTERNAL MEMORY INTERFACE

The TS94104 is designed to be running with an external program memory. This memory requires the following characteristics:

— random addressing,
— TTL compatible 3-STATE OUTPUTS,
— TTL compatible inputs
— access time (from CS to output): 800 ns max.

These requirements are typically met with most EPROMS.
During operation, the address of the next instruction is sent out on A8, A9 and A10 and IP0-IP7 while $\overline{AD/DATA}$ is high (logic "1" = address mode).
Address data on the IP lines is stored into an external latch on the high to low transition of the AD/DATA line. When $\overline{AD/DATA}$ is low (logic "0" = data mode) the output of the memory is sent on the IP0-IP7 bus, and is latched inside the microcontroller on the rising edge of $\overline{AD/DATA}$. Note that $\overline{AD/DATA}$ output has a period of one instruction time, and specifies whether the IP bus is outputing addresses or inputing data. A simplified block diagram of the external memory interface is shown on Figure 6.

Ident. number	Characteristics	Symbol	Min.	Typ.	Max.	Unit
1	SK propagation delay	t_{s1}	—	—	2	µs
2	Input set up delay	t_{setup}	$t_c/10$ +1.3	—	—	µs
3	Input Hold time	t_{hold}	100	—	—	ns
4	Output propagation delay	t_{pd1}	$t_c/10$	—	1.0	µs
5	SO propagation delay (SO as SIO output)	t_{pd0}	$t_c/10$	—	1.0	µs
6	IP set up delay (Opcode)	t_{opcod}	—	—	—	—
7	IP buffer propagation delay	t_{buff}	—	—	—	—



(*) SO AS AN OUTPUT WHEN (EN0, EN3) = (0,0) OR (1,0) OR (1,1)

— SK has 50% duty cycle when used as a clock.

— Outputs are sampled (by MCU) on the rising edge of SK (except IP0-IP7, A8-A10).

— Inputs are sampled on the SK falling edge.

— The external address bus (IP0-IP7, A8-A10) is sampled on the falling edge of AD/DATA.

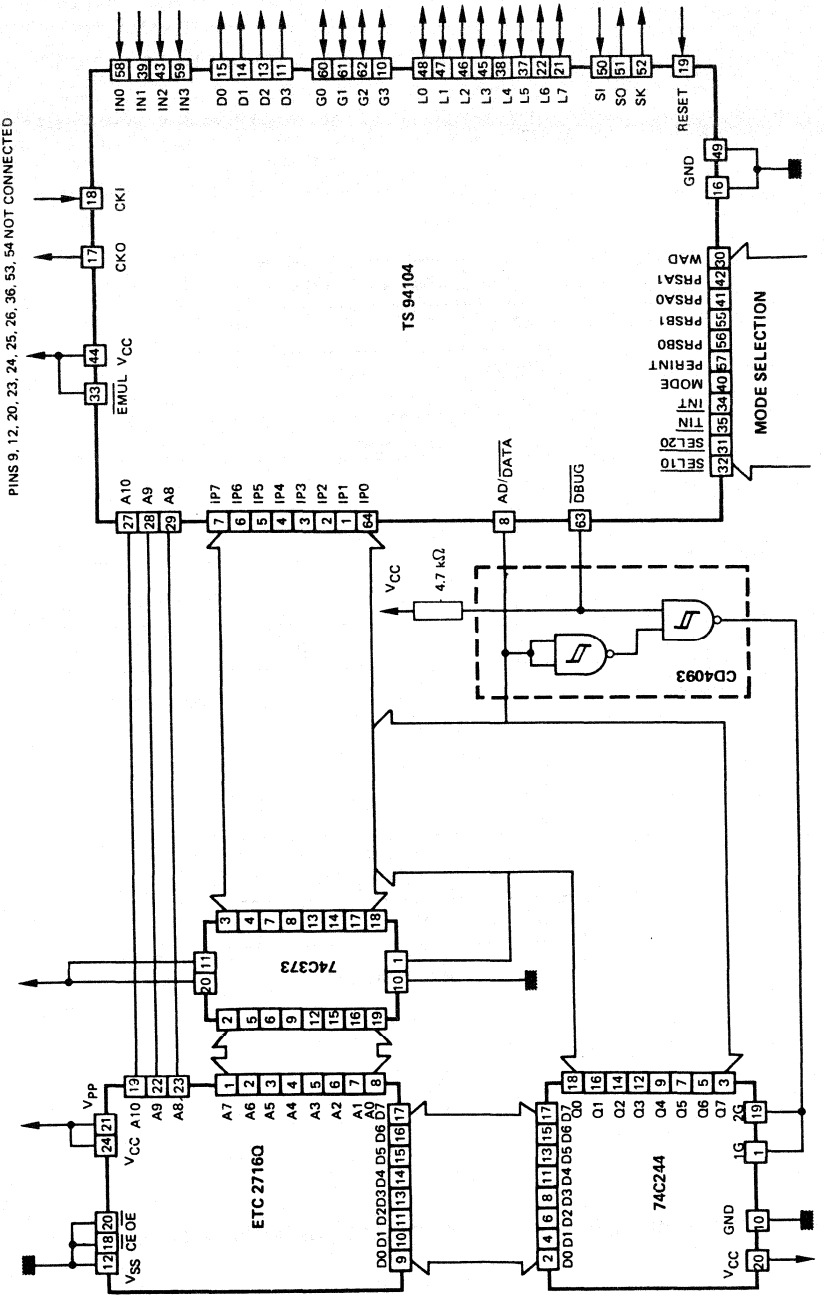
— The IP0-IP7 inputs have to be referenced to the rising edge of AD/DATA.

Note:

— Consider we are executing an instruction (from /1 to /5). The address sampled on /5 on the address bus is the address of next instruction, but the SKIP status sampled on the SKIP output is the status of the instruction currently under execution.

— The SKIP output = 1 when the current instruction is skipped, except for LBI's skipped after an LBI.

FIGURE 6


PINS 9, 12, 20, 23, 24, 25, 26, 36, 53, 54 NOT CONNECTED
TS 94104
MODE SELECTION
CD4093
74C373
ETC 2716Q
74C244
IN0 IN1 IN2 IN3
D0 D1 D2 D3
G0 G1 G2 G3
L0 L1 L2 L3 L4 L5 L6 L7
SI SO SK
RESET
GND
CKI
CKO
EMUL
VCC
WAD
PRSA1
PRSA0
PRSB1
PRSB0
PERINT
MODE
INT
TIN
SEL20
SEL10
A10 A9 A8
IP7 IP6 IP5 IP4 IP3 IP2 IP1 IP0
AD/DATA
DBUG
4.7 kΩ
VPP
VSS
CE OE
A7 A6 A5 A4 A3 A2 A1 A0
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
1G 2G

DUAL TIMER

Dual Timer is identical to TS94100 family. Please refer to the TS94100 specification.

INSTRUCTION SET

TS94104 instruction set is identical to the TS94100 instruction set. Please refer to the TS94100 specification.

ELECTRICAL CHARACTERISTICS

TS94104 electrical characteristics are identical to the TS94100. Please refer to the TS94100 specifications.

MODE SELECTION

TS94104 can emulate the whole TS94100 family (i.e. 1K and 2K ROM) by simply connecting $\overline{SEL10}$ and $\overline{SEL20}$ pins to Vcc or GND. In addition, most TS94100 family mask options can be choosen by setting extra pins to Vcc or GND as shown on figure 7, figure 8.

	TS94144	TS94120
$\overline{SEL10}$	1	1
$\overline{SEL20}$	1	0

MCU SIZE

	Prescaler	Event counter
$\overline{TIN}$	0	1

COUNTER INPUT

	No watchdog	D3 pin as watchdog input
WAD	0	1

WATCHDOG

	External interrupt	Timer overflow
$\overline{INT}$	0	1

INTERRUPT SOURCE

FIGURE 7

ROMLESS - I/O AND OSCILLATOR OPTIONS SELECTED

	÷ 1	÷ 5	÷ 20	÷ 40
PRSA0	0	1	0	1
PRSA1	0	0	1	1

TIMER A PRESCALER

	Period measurement	Duty cycle measurement
MODE	0	1

TIMER B: PERIOD/DUTY CYCLE (MRB0 = 0)
(MRB1 = 0)

	÷ 1	÷ 5	÷ 20	÷ 40
PRSB0	0	1	0	1
PRSB1	0	0	1	1

TIMER B PRESCALER

	High to low transition on IN0	Every transition of IN0
PERINT	0	1

IN0 TRANSITION

FIGURE 8

PIN NAME

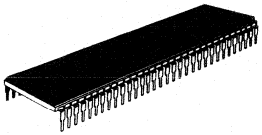
IP0-IP7	I/O for ROM address and data
A8-A9-A10	Address Most Significant Bits
SKIP	SKIP status output
AD/$\overline{\text{DATA}}$	Address out/data in (demux special)
$\overline{\text{INT}}$	Select pin for external interrupt or timer overflow (CPU)
$\overline{\text{TIN}}$	Select pin for prescaler or event counter (CPU)
$\overline{\text{SEL10}}$-$\overline{\text{SEL20}}$	Select pin for the RAM size (TS94210 or TS94144)
$\overline{\text{DBUG}}$	Output enable signal for external EPROM, and select pin for debug modes (not to be used by the customer)
$\overline{\text{EMUL}}$	Emulation pin: internal timer and peripheral halt, interrupts masking
WAD	Select pin for watchdog option
MODE	Select pin for period measurement or duty cycle measurement
PERINT	Select pin for high to low or every transition of IN0 (dual timer)
PRSA0 PRSA1	Select pin for prescaler division of TIMER A
PRSB0 PRSB1	Select pin for prescaler division of TIMER B

ROMLESS EXTRA PINS - FUNCTIONAL DESCRIPTION

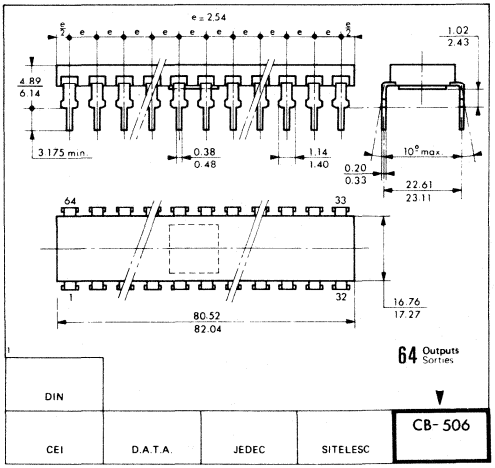
		OPTION
CKO PIN CONFIGURATION	GENERAL PURPOSE INPUT, LOAD DEVICE TO Vcc	1-1
CKO INPUT LEVEL	STANDARD TTL INPUT LEVELS	2-0
CKI INPUT CONFIGURATION	EXTERNAL CLOCK	3-2
CKI DIVIDER	CKI FREQUENCY DIVIDED BY 10	4-1
RESET PIN CONFIGURATION	LOAD DEVICE TO Vcc	5-0
IN1-IN3 INPUT CONFIGURATION	LOAD DEVICE TO Vcc	6-0
IN1-IN3 INPUT LEVELS	STANDARD TTL INPUT LEVELS	7-0
S1 INPUT LEVELS	STANDARD TTL INPUT LEVELS	8-0
S0 OUTPUT CONFIGURATION	GENERAL PURPOSE TTL OUTPUT	9-0
SK OUTPUT CONFIGURATION	GENERAL PURPOSE HIGH CURRENT OUTPUT	10-1
L0, L1, L2 OUTPUT DRIVER	3 STATE PUSH-PULL OUTPUT	11-5, 12-5, 13-5
L3 OUTPUT CONFIGURATION	3 STATE GENERAL PURPOSE TTL OUTPUT	14-0
L4 OUTPUT CONFIGURATION	3 STATE GENERAL PURPOSE VERY HIGH CURRENT OUTPUT	15-1
L5 OUTPUT CONFIGURATION	OPEN DRAIN TTL OUTPUT	16-2
L6 OUTPUT CONFIGURATION	OPEN DRAIN VERY HIGH CURRENT OUTPUT	17-3
L7 OUTPUT CONFIGURATION	3 STATE PUSH-PULL TTL OUTPUT	18-4
L INPUT LEVEL	HIGHER VOLTAGE INPUT LEVEL	19-1
G2-G3 OUTPUT CONFIGURATION	GENERAL PURPOSE OUTPUT	20-0, 21-0
G INPUT LEVEL	STANDARD TTL INPUT LEVELS	22-0
D0-D3 OUTPUT CONFIGURATION	OPEN-DRAIN OUTPUT	23-1, 24-1, 25-1, 26-1
G0 OUTPUT LEVEL FOR STA=0	LOGICAL 1	34-1
G1 OUTPUT LEVEL FOR STB=0	LOGICAL 1	35-1

PHYSICAL DIMENSIONS

CB-506



PLASTIC PACKAGE



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NOTES

Printed in France

THOMSON COMPONENTS MICONDUCTEURS

TS94120 • TS94144

SINGLE SHIP MICROCONTROLLERS

ADVANCE INFORMATION

The TS94120/144 single chip NMOS microcontrollers are members of the TS94000 family, fabricated using N-channel silicon gate XMOS technology. The TS94120/144 contain the internal logic of the microcontrollers ET9410/20/44 (system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions). Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture, and I/O scheme designed to facilitate keyboard input, display output, BCD data manipulation and triac drive. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized low cost controller. TS94100 family offers a dual 16-bit timer perfectly suited for universal motor speed control (phase control), accurate time measurements and waveform generation.

- Low cost
- 23 I/O lines
- Single supply operation (4.5 V to 5.5 V)
- Low-current drain (13 mA max)
- General purpose and 3-state outputs
- TTL compatible inputs
- TTL compatible outputs
- Temperature range (0° to + 70°C)
- Extended temperature range (— 40°C to + 85°C) available.

CPU

- Powerful instruction set (52 instructions)
- ROM: 2K x 8 (TS94144), 1K x 8 (TS94120)
- RAM: 128 x 4 (TS94144), 64 x 4 (TS94120)
- 2 interrupt sources: external pin or internal timer overflow
- 3-level subroutine stack
- 4 μs instruction cycle time
- Programmable read/write 8-bit internal timer/event counter
- Internal shift register with serial I/O
- Watchdog feature
- Direct drive of LED digit and segment line
- Software compatible with the other members of ET9400, ETL9400 and ETC9400 families.

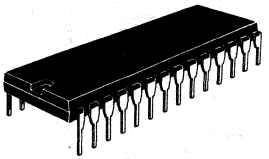
DUAL TIMER PERIPHERAL

- Two 8-bit and one 16-bit independent timers/counters
- 2 independent programmable prescalers
- Maximum working frequency: 1.25 MHz
- 16 software programmable working modes including delayed and calibrated pulse triggering, complex waveform generation, period and duty-cycle measurements
- 3 interrupt sources
- Zero-crossing detector
- Direct drive of triac

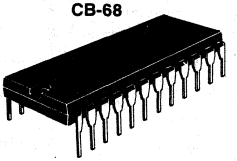
NMOS

SINGLE CHIP MICROCONTROLLERS

CASES
CB-132

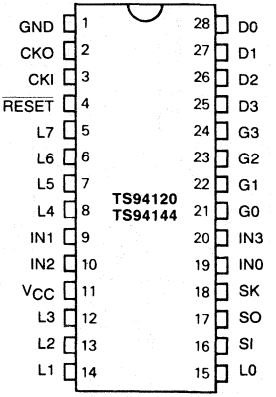


CB-68



P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT



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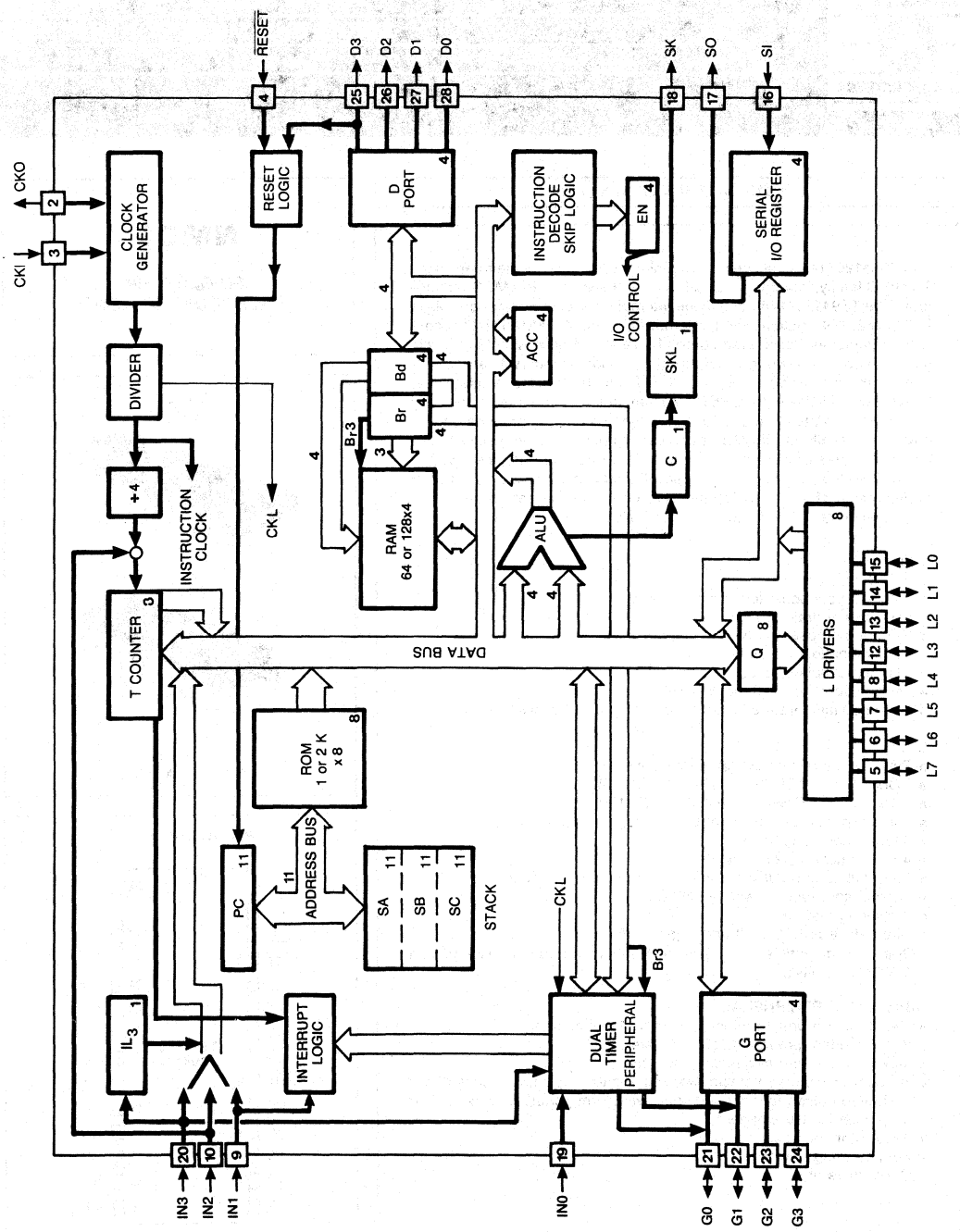


FIGURE 1 - BLOCK DIAGRAM

CPU FUNCTIONAL DESCRIPTION

The internal architecture is shown in Figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. A bit set is a logic « 1 », when a bit reset is a logic « 0 ».

PROGRAM MEMORY

Program memory consists of ROM:
- 1024 bytes for the TS94120
- 2048 bytes for the TS94144

These bytes of ROM can be either program instructions, constants or ROM addressing data.

ROM addressing is accomplished by a 11-bit PC register which selects one of the 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value.

- For TS94120 the 10 lower bits of PC are used to address the internal ROM

Three levels of subroutine nesting are implemented by a three level deep stack. Each subroutine call (or interrupt) pushes the next PC address onto the stack. Each return (RET) pops off the stack back into the PC register.

DATA MEMORY

Data memory consists of a 512-bit RAM for the TS94144 organized as 8 data registers of 16 x 4-bit digits. RAM addressing is implemented by a 8-bit B register whose upper 3 bits Br0, Br1, Br2 select 1 of 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register.

Data memory consists of a 256-bit RAM for the TS94120 organized as 4 data registers of 16 x 4 bits digits. The B register is 8 bits long. Upper 2 bits Br0, Br1 select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 x 4-bit digits in the selected data register. Br2 is not used to address the RAM and so 2 addresses with a different value of Br2 will access the same word in the RAM.

For TS94120/144, the uppermost bit Br3 of B register is only used to select either the peripheral or RAM.

While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with the A register (accumulator), they may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the immediate operand field of these instructions.

The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

INTERNAL LOGIC

A 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd field of the B register, to load and input 4 bits out of the 8-bits Q latch, to input 4 bits out of a ROM word, to input G or IN ports, and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing the results in A with eventually a carry bit in the 1-bit C register. The C register in conjunction with the XAS instruction and the EN register is also related to the SK output control.

The 8-bit T counter is a binary up counter which can be loaded to and from M and A using CAMT and CTMA instructions. This counter may be running in two modes depending on a mask-programmable option: as a timer or as an external event counter. When the T counter overflows, an overflow flag will be set (see SKT instruction below). Note that T counter is cleared on reset. A functional block diagram of the timer/counter is illustrated in Figure 4.

3 general-purpose inputs, IN3-IN1, are provided. Note that IN3 can be considered as a dual-timer input.

IN0 is an analog input connected to an internal comparator.

The D register provides, 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. D3 is also used as the watchdog input when the watchdog option is selected.

The G register is a 2-bit general-purpose bidirectional I/O port (G3-G2). G0-G1 are the outputs of the peripheral and can also be used as general-purpose inputs.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Q register contents are transferred to the L I/O ports when the L drivers are enabled under program control (see LEI instruction).

L driver, when enabled, outputs the content of latched Q data to the L I/O ports. Contents of L may be read directly into A and M.

The SIO register is a 4-bit serial-in/serial-out shift register for the serial out. SIO content can be exchanged with A.

The XAS instruction copies C into the SKL Latch.

When SKL = 1, SK is a clock output
When SKL = 0, SK outputs a value depending upon the contents of EN0 and EN3.

THE « EN register » is an internal 4-bit register loaded under program control by the LEI instruction. Each bit selects or inhibits the dedicated feature associated with each bit of the EN register (EN3-EN0).

- With EN1 set, the CPU interrupt is enabled.
- With EN2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN2 disables the L drivers, setting the L port as high impedance inputs.
- EN3, in conjunction with EN0, affects the SO and the SK outputs (see table 1).
  - — When EN3 = 0, SO outputs EN0 and SK outputs the clock anded with the content of the SKL latch,
  - — when EN3 = 1, SO is the output of the serial shifter, while SK outputs the clock (if SKL = 1) or the EN0 bit (if SKL = 0).

  Even when SO is disabled (as SIO output), data goes on shifting through SIO and can be exchanged with A via an XAS.

TABLE 1. ENABLE REGISTER MODES - BITS EN0 AND EN3

EN3	EN0	SO	SK after XAS
0	0	0	If SKL = 1, SK = Clock If SKL = 0, SK = 0
0	1	1	
1	0	Serial out	If SKL = 1, SK = Clock If SKL = 0, SK = EN0
1	1	Serial out	

INTERRUPT SOURCES

There are 3 possible interrupt sources (see Figure 2).

- Counter overflow or external interrupt (mask option). External interrupt is triggered on the falling edge of a zero pulse. The zero pulse must be at least 2 instruction cycles wide on the external pin IN1 (or internal counter overflow).
- 2 peripheral interrupt sources (see peripheral description).

Each interrupt source has its own enable bit (EN1 for the CPU interrupt, ENA and ENB for the peripheral interrupts) and its own flag (F1 for the CPU interrupt, FA and FB for the peripheral interrupts, see Figure 13). An interrupt is enabled when its associated enable bit is set. Its associated flag is set when the interrupt is requested (for example, timer overflow for the CPU interrupt).

Note that the FA, FB, ENA, ENB bits, but also the F1 bit are implemented in the peripheral registers.

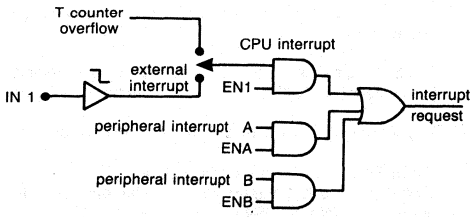


FIGURE 2: INTERRUPT BLOCK DIAGRAM

The following features are associated with interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

- The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack:
  PC + 1 → SA → SB → SC. Any previous contents of SC is lost. The program counter is set to hex address 0FF (the last word of page 3) and all incoming interrupts are disabled without clearing the enable bits.

- An interrupt will be acknowledged only after the following conditions:
  - — An interrupt request has been generated.
  - — The associated enable bit is set.
  - — A currently executing instruction has been completed.
  - — All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed).

- Upon acknowledgement of an interrupt, bit Br3 of the B register is saved (and later restored upon « popping » off the stack by a RET instruction), then Br3 is cleared, allowing the user to begin his interrupt subroutine in the RAM space addressing.

- Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon « popping » off the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the end of the interrupt routine, a RET instruction is executed to « pop » the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines should not be nested within the interrupt servicing routine since « popping » the stack will enable any previously saved main program skips, interfering with the orderly execution sequence of the interrupt routine.

- The first instruction at hex address 0FF must be a NOP.
- When an interrupt is acknowledged, other interrupt sources are internally disabled until the end of interrupt servicing subroutine.

RESET

The RESET pin is configured as a Schmitt trigger input. If not used it should be connected to Vcc. Initialization will occur whenever a logic « 0 » is applied to the RESET input for at least three instruction cycles.

Upon initialization, the PC register is cleared to 0 (ROM address 0) the A, B, C, D, EN, G2-G3, T counter, IL latches registers and the peripheral registers CRA, CRB, IMR are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. Data

Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA. RC must be greather than 5 times power supply rise time.

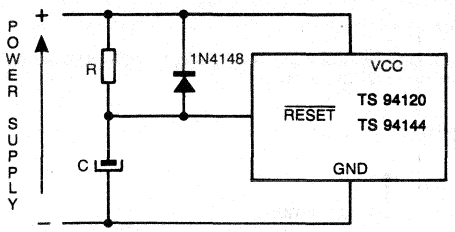


FIGURE 3: POWER-UP CLEAR CIRCUIT

T COUNTER

There are two modes selected by mask option:

- Time-base counter. In this mode, the instruction cycle frequency generated from CKI passes through a 2-bit (divide-by-4) prescaler. The output of this prescaler increments the 8-bit counter thus providing a 10-bit timer. T counter prescaler is cleared by a CAMT instruction or on reset.

  For example, using a 1.25 MHz crystal with a divide-by-5 option, the instruction cycle frequency of 250 KHz increments the 10-bit timer every 4 µs. By presetting the counter and detecting overflow, accurate timeouts between 16 µs (4 counts) and 4.096 ms (1024 counts) are possible. Longer timeouts can be achieved by accumulating, under software control, multiple overflows.

- External event counter. With this option, a low-going pulse (« 1 » to « 0 ») lasting more than 2 instruction cycles on the IN2 input will increment the 8-bit T counter.

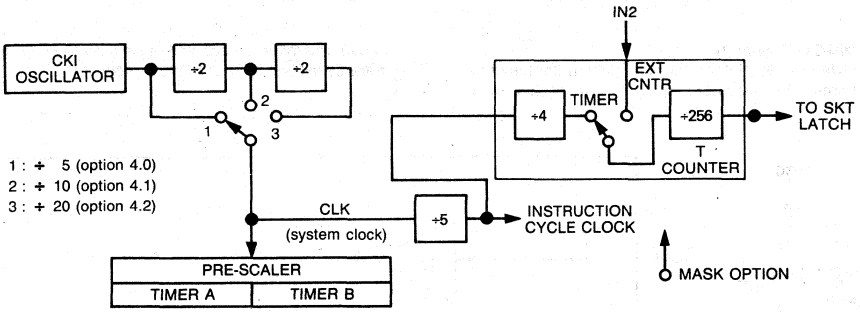


FIGURE 4: CLOCK AND CPU COUNTER BLOCK DIAGRAM

OSCILLATOR

There are three basic clock oscillator configurations available as shown in Figures 5 and 6.

- Crystal Controller Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 20 (optional by 10 or 5).

- External Oscillator. CKI is an external clock input signal. The external frequency is divided by 10 to give the instruction cycle time. CKO is available to be used as a general purpose input.

- RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 10 to give the instruction cycle time. CKO is in this case available to be used as a general purpose input (see INIL instruction).

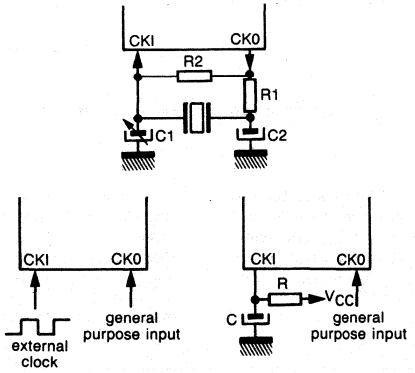


FIGURE 5: OSCILLATOR EXTERNAL CONFIGURATION

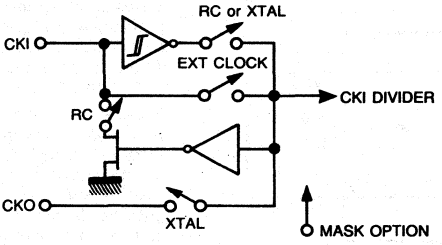


FIGURE 6: OSCILLATOR MASK OPTIONS

WATCHDOG (Figure 7)
This mode may be chosen by mask option. In this case, D3 becomes the watchdog input. This mode is a basic need for microcontrollers working in a noisy environment, where parasitics may crash the program.

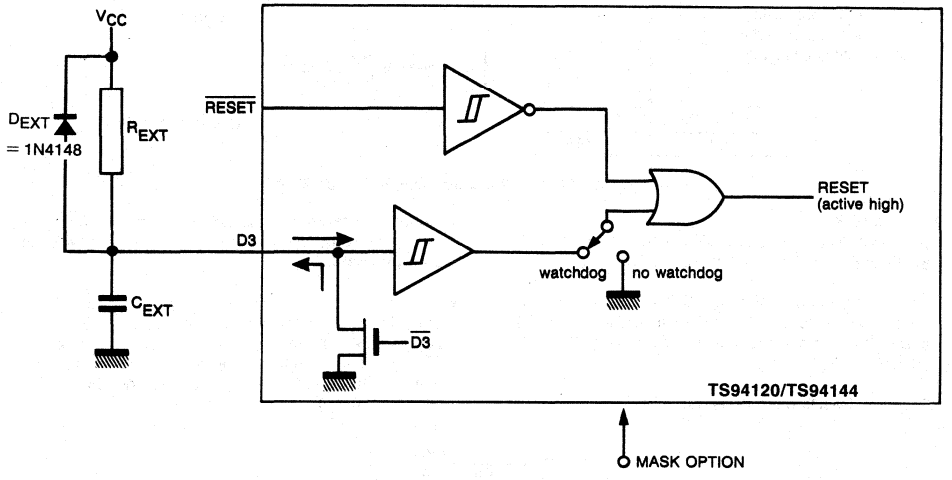


FIGURE 7: D3 AS WATCHDOG INPUT

In the watchdog mode, a « 1 » on pin D3 activates the internal reset (see Figure 7). The user needs only to connect a pull-up resistor and a capacitor on D3, and insert a watchdog loop in his program. This software loop will periodically outputs a « 0 » on D3 when the program is normally executed. When the microcontroller is trapped in another loop, the watchdog loop is not any more efficient and C_{ext} is charged up to Vcc, thus triggering the chip reset.
Open-drain option has to be selected on D3 when the watchdog mode is chosen. The $R_{EXT} \times C_{EXT}$ time constant on D3 is related to the period of the software watchdog loop. D_{EXT} speeds up the C_{EXT} discharge time during power off.

DUAL TIMER

FUNCTIONAL OVERVIEW

A block diagram of the peripheral is given in Figure 8. It consists of two truly independent blocks. Block A consists of two 8-bit registers (RW0-RW1, RD0-RD1) and two 8 bit binary down-counters (CW0-CW1, CD0-CD1) organized as two register-counter pairs. The block B consists of a sixteen bit register (RB0-RB3) and a 16-bit binary down counter (CB0-CB3). The operating modes are software programmable through CRA and CRB control registers. Most of the modes are driven by block A and B clocks (CLKA, CLKB) which are respectively generated by the A or B prescalers. These prescalers are mask-option programmable. The following options are available: the system clock (CLK) may be divided by 1, 5, 20, 40.

Block A is a complex waveform generator. In most of the modes, each 8 bit pair is running alternatively, using the autoreload procedure. The CD counter starts to run. It counts down to zero, at which time the output flip-flop of block A is toggled. The data in the RD register is then reloaded automatically into the CD counter, which stays idle. In the same time, the RW/CW 8 bit pair starts running. When CW counts down to zero, the output flip-flop is toggled again, CW is reloaded with RW contents and stays idle. The RD/CD pair can start running again and so on. In the pulse burst generation mode, the CD/RD pair is running alone: the output flip-flop is toggled each time the CD counter counts down to zero. The CW/RW pair does not drive the output flip-flop, but counts the pulses generated by the CD/RD pair. Block A output is G0, input is IN0.

Block B performs measurement and generation functions. In the frequency generation and frequency divider mode, the 16-bit pair is running, using the autoreload procedure. In the measurement mode, while the counter is running, an automatic transfer to the register is performed each time a measure is ended. This is determined by a mask-option: if the period measurement mode is selected, a measure is ended each time a high to low transition occurs on the IN3 pin. If the duty-cycle measurement mode is selected, a measure is ended each time a high to low or low to high transition occurs on the IN3 pin. In the external event counter mode, the counter counts down the external pulses, register RB latching up counter CB state every instruction cycle t_C. Block B output is G1, input is IN3.

In all modes of blocks A and B, there is no initial autoreload, and the counters start, regardless of their content.

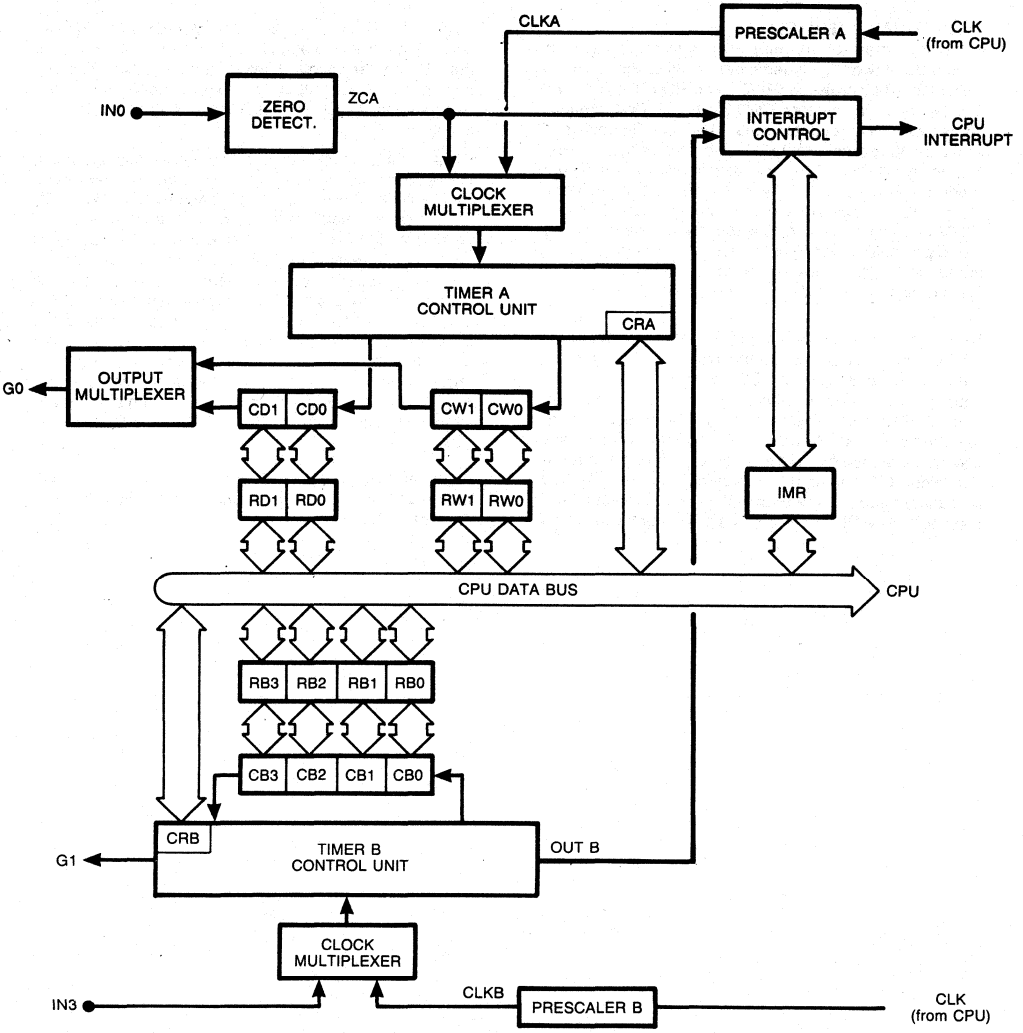

CLKA
PRESCALER A
CLK
(from CPU)
IN0
ZERO
DETECT.
ZCA
INTERRUPT
CONTROL
CPU
INTERRUPT
CLOCK
MULTIPLEXER
TIMER A
CONTROL UNIT
CRA
G0
OUTPUT
MULTIPLEXER
CD1
CD0
CW1
CW0
RD1
RD0
RW1
RW0
IMR
CPU DATA BUS
CPU
RB3
RB2
RB1
RB0
CB3
CB2
CB1
CB0
CRB
G1
TIMER B
CONTROL UNIT
OUT B
CLOCK
MULTIPLEXER
IN3
CLKB
PRESCALER B
CLK
(from CPU)

FIGURE 8

PERIPHERAL REGISTERS

The Dual-Timer contains several registers that interface with the CPU :

- two 8-bit data registers (RD0-RD1) and (RW0-RW1) for block A, and one-16 bit data register (RB0-RB1-RB2-RB3) for block B.
- two 4-bit control registers (1 per block) CRA and CRB managing the selection mode, the output on the pins G0 and G1 and start-up for both blocks.
- One 4-bit interrupt management register (IMR). This register contains the enable bits and the interrupt flags.

CRA: Control Register

F1	STA	MRA1	MRA0
3	2	1	0

STA: Start/Stop bit and output enable on pin G0
MRA1-MRA0: Block A mode selection
F1: CPU interrupt flag

CRB: Control Register

CSB	STB	MRB1	MRB0
3	2	1	0

STB: Start/Stop bit

CSB: Output enable on pin G1
MRB1-MRB0: Block B mode selection

IMR: Interrupt Management Register

ENB	ENA	FB	FA
3	2	1	0

FA, FB: Interrupt flag of blocks A and B
ENA, ENB : Interrupt enable bits of blocks A and B

FIGURE 9: CONTROL REGISTERS (CRA AND CRB) AND INTERRUPT MANAGEMENT REGISTER (IMR)

All these registers are memory mapped as 4-bit memory words (See Figure 10) and are addressed by Bd and the lower bit Br0 of Br (See Figure 11).

Br0 \ Bd	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RD1	RD0	RW1	RW0												CRA
1	RB3	RB2	RB1	RB0			IMR									CRB

FIGURE 10: REGISTERS MEMORY MAPPING

All the instructions referenced to the RAM may be used for the peripheral, including bit manipulation instructions. Br3, the uppermost bit of Br controls the switching between the RAM and the peripheral when using memory reference instructions.

Two instructions are able to alter the content of Br3:

— XABr, that exchanges A with Br, and in particular A3 with Br3,
— TMB, that complements Br3.

When Br3 = 0, RAM is accessed
When Br3 = 1, peripheral registers are accessed

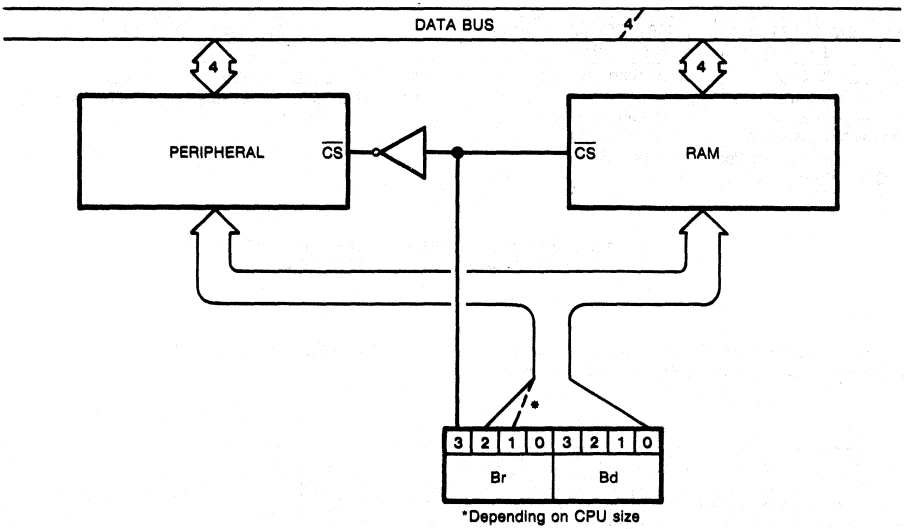


FIGURE 11: PERIPHERAL AND RAM ADDRESSING BLOCK DIAGRAM

Note that, as Br1 and Br2 are not used to address the registers, there is redundancy in the addressing: that is, 2 addresses where only Br1 (or Br2) is different will access the same register.

- Each peripheral memory word may be read at any time, even during reloading: the value read is always valid.

- On the other hand, the user cannot write in a peripheral memory word while the peripheral internal logic is trying to reload it.

To ensure a good start of the timer, the Start/Stop bit (STA, STB) should not be set while setting a new mode (MRA0-MRA1, MRB0-MRB1): one instruction cycle is required, for stabilization.

Counters access:
Data transfer between counters and registers (RD ↔ CD, RW ↔ CW, RB ↔ CB) exchanges words of 16 bits (or 8 bits). This transfer is done with a single instruction (2 bytes opcode) as shown on table 2.

MNEMONIC	OPCODE	DATA FLOW
TRCA	23 8A	RD → CD RW → CW
TCRA	23 8B	CD → RD CW → RW
TRCB	23 9A	RB → CB
TCRB	23 9B	CB → RB

TABLE 2: 16-BIT TRANSFER INSTRUCTIONS

Opcodes of these 16 bits transfer instructions are XAD opcodes addressing unused peripheral addresses, and are valid only when Br3 = 1. TRCA, TCRA, TRCB and TCRB instructions load accumulator A with F(Rex).

Important remark

Note that transfer is equivalent to:

XAD 0A for transfer (RW, RD) towards (CW, CD)
XAD 0B for transfer (CW, CD) towards (RW, RD)
XAD 1A for transfer RB towards CB
XAD 1B for transfer CB towards RB

} when $B_r3 = 1$

These four transfer instructions are therefore compatible with the ET9400 set of instructions. XAD instruction has a different meaning when Br3 = 1.

CONTROL REGISTERS CRA AND CRB

— The MRA0-MRA1 and MRB0-MRB1 bits select the operating mode of block A and block B. The mode selected by MRB0 = MRB1 = 0 is mask option programmable: period measurement, or duty-cycle measurement.

Block A

MRA1	MRA0	OPERATING MODE
0	0	Triggered pulse generation
0	1	Pulse burst generation
1	0	Duty cycle generation
1	1	Analog period counter

Block B

MRB1	MRB0	OPERATING MODE	
0	0	Period measurement Duty-cycle measurement	} mask programmable option
0	1	External event counter	
1	0	Frequency generation	
1	1	Frequency divider	

TABLE 3: OPERATING MODE CODING THROUGH MRA0- MRA1 AND MRB0-MRB1 BITS

— Setting STA and STB to zero stops the counters which stays idle. At the same time, the A and B flip flop outputs are forced to predefined values (« 0 » or « 1 » selectable by mask option).

— Setting STA and STB to 1, makes the respective counters run in the selected mode. In the pulse burst mode, STA is automatically reset when the burst is generated.

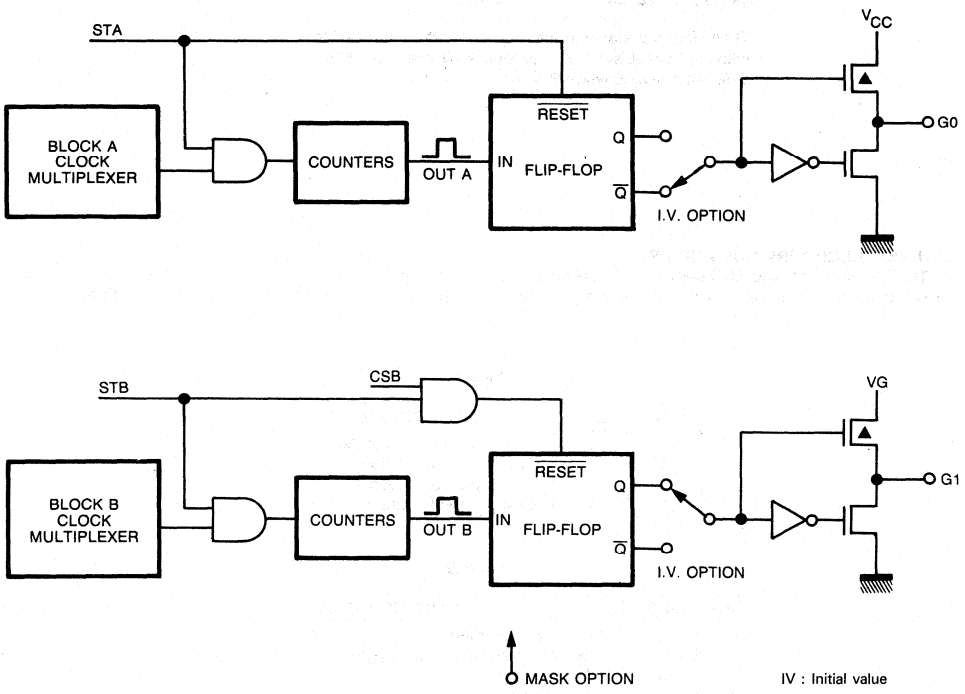


FIGURE 12: OUTPUT CONTROL

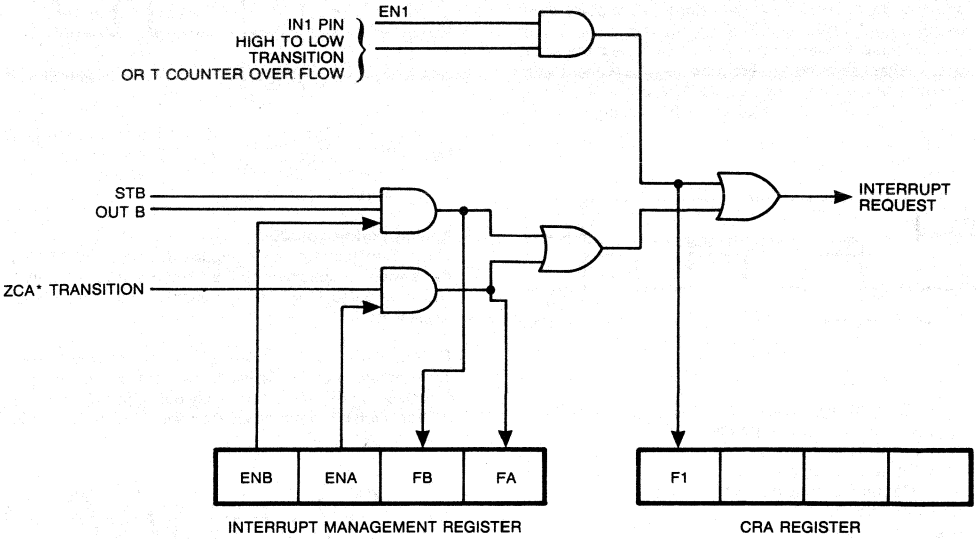
Setting the CSB bit to zero disconnects the pin G1 from the CB counter : counter is running and G1 is forced to 1 or 0 (depending on mask option)

G0 (and G1) pins can be used as a general purpose CPU input, as long as it has been previously set to output a 1.

If proper start is required, the counters should be initialized before the start up. In other words, the first G0 (or G1) transition (counter underflow) occurs at a defined time after start up only if the counter C was previously loaded (see nota-1).

SYSTEM RESET
Upon reset CRA, CRB and IMR peripheral registers are cleared. CD/RD, CW/RW and CB/RB are unchanged.

DUAL TIMER INTERRUPT MANAGEMENT
The Dual Timer interrupts are controlled by the IMR register.



* : ZCA is the Zero crossing detector output (see Option 32)

FIGURE 13: INTERRUPT MANAGEMENT

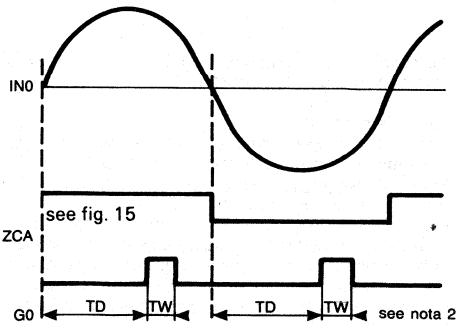
The Dual Timer interrupt sources, one for each block, are software selectable through the enable bits ENA and ENB (IMR register). Each interrupt in turn sets the FA or FB flag in the IMR register when activated. F1 (bit 3 of CRA register) is set when a CPU interrupt is generated. These flags will be used in the interrupt subroutine to locate the interrupt source. These flags will have to be reset by the user interrupt subroutine. It should be noted that Timer B interrupt is disabled through the start bit STB, when this block is not running. The peripheral interrupt requests are enabled by the ENA bit, or by the ENB and STB bits. The block A interrupt source is mask option programmable: an interrupt request is generated either on each transition of the zero crossing detector output or on high to low transition of the zero crossing detector output. Block B interrupt requests are generated on each pulse on OUTB.

BLOCK A MODE DESCRIPTION

Remark: all the following timings are drawn in the case where I.V. (Initial value) of G0 is 0.

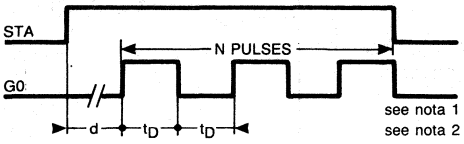
Triggered pulse generation
This mode outputs a pulse triggered by the zero-crossing of a signal at IN0. The delay from the zero-crossing is specified by the content of RD. The pulse width is specified by the content of RW.

$t_D = D. t_{CLKA} + 2.5\ t_{CLK}$
$t_W = (W + 1). t_{CLKA}$
Where t_{CLK} = System clock period ;
t_{CLKA} = Block A clock period
D = Content of register RD
W = Content of register RW
$1 \leqslant D \leqslant 255$
$0 \leqslant W \leqslant 255$



Nota 2: initial value of G0 can either be 1 or 0 (depending on mask option 3.4).

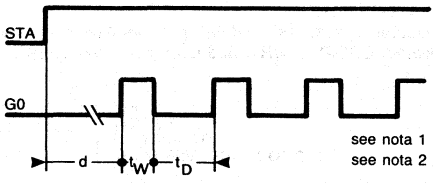
Pulse burst generation
This mode outputs on G0 a specified number of pulses of a specified width. The number of pulses is specified by the contents of register RW, while the pulse width is specified by the contents of register RD. The pulse burst is generated each time STA is set to a « 1 ». CD is automatically loaded from register RD, at each transition of G0. After the W pulses are transmitted, counter CW is automatically loaded from register RW, and STA is reset. Setting STA to 1 will repeat the previous sequence.



$t_D = (D + 1).\ t_{CLKA}$
t_{CLKA} = Block A clock period
N = (W + 1)
D = Content of register RD
W = Content of register RW
d: delay (see nota 1)
$0 \leqslant D,W \leqslant 255$

Nota 1: If counter CD is not loaded with a defined value before start up, d will be $t_{CLKA} \leqslant d \leqslant 255.\ t_{CLKA}$. Note that this undefined value of d is equivalent to an undefined delay in outputing the waveform. In order to control this delay time d, user should load counter CD (in addition to register RD).

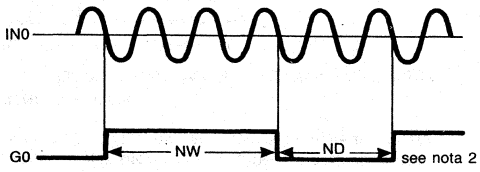
Duty-cycle generation
This mode generates a rectangular waveform on G0. Pulse width is specified by the contents of register RW, inter-pulse length is specified by the content of register RD (be carefull with I.V: see nota 2)



$t_D = (D + 1).\ t_{CLKA}$ W = Content of register RW
$t_W = (W + 1).\ t_{CLKA}$ d: delay (see nota 1)
D = Content of register RD $0 \leqslant D,W \leqslant 255$
t_{CLKA} = Block A clock period

Analog period counter
This mode generates a rectangular waveform on G0. The pulse width is specified by the contents of register RW, and inter-pulse length is specified by the contents of register RD.

The counter is not controlled by the clock of block A, but decrements each IN0 falling edge. G0 transition is synchronised on SK. Maximum delay between IN0 = 0V and G0 transition is therefore less than equal to one SK period ($4\ \mu s \leqslant t_{SK} \leqslant 10\ \mu s$).



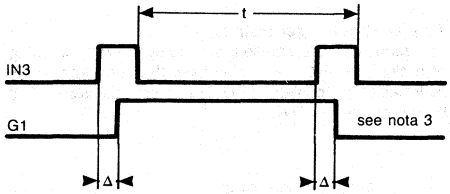
ND = (D + 1)
NW = (W + 1)
Where W = Contents of register RW
D = Contents of register RD
$0 \leqslant D,W \leqslant 255$

Remark: analog signal frequency should not exceed $1/2tc$.
$F_{IN0} \leqslant 1/2tc$.

BLOCK B MODE DESCRIPTION

Remark: all the following timings are drawn in the case where I.V (initial value) fo G1 is 0.

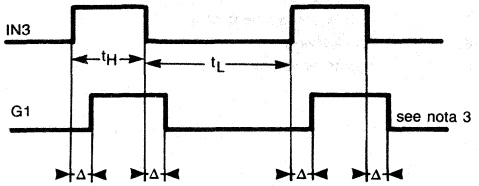
Measurement mode
This mode is mask-option programmable: period measurement mode, or duty-cycle measurement mode.
Period measurement mode: This mode measures the period of an external waveform on IN3.
On the high to low transition, counter CB is transferred to register RB, and then cleared. As the counter is counting down from zero, the value read from the register is a two's complement value. The register can be read at any time, even when being changed: the data is always valid.



$t = (N + 1)\ t_{CLKB}$
Where t_{CLKB} = Block B clock period
N = Two's complement value of register RB
$0 \leqslant N \leqslant 2^{16}-1$
$\Delta = 1,5 \times t_{CLK}$
t_{CLK} = System clock period

The output G1 toggles each time a counter to register transfer is performed.

Duty-cycle measurement mode: From an external signal on IN3, the counter CB starts, counting the pulse width high. On the falling edge of IN3, CB is transferred to the register RB, and then cleared. Then, counter CB starts counting the IN3 inter-pulse length. On rising edge, CB is transfered to RB, CB is cleared, and duty cycle measurement starts again. G1 output toggles each time a counter to register transfer is performed. The user has to read the register contents before it is changed by the next measurement. This can be done by an interrupt, or by monitoring IN3 or G1.



$t_H = (NH + 1).\ t_{CLKB}$
$t_L = (NL + 1).\ t_{CLKB}$
t_{CLKB} = Block B clock perdiod
$\Delta = 1{,}5 \times t_{CLK}$

NL, NH = Two's complement value of register RB contents
$0 \leqslant NL, NH \leqslant 2^{16}-1$

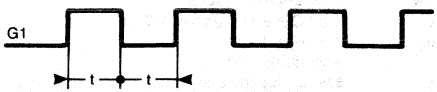
Nota 3: initial value of G1 can either be 1 or 0 (depending on mask option 35)

External event counter
In this mode, counter CB is an external events (or pulses) counter. There is no automatic clear of the counter: it counts down from whatever state it was. Thus, to ease the reading of the information, the counter should be preloaded. Preloading the counter with all zeroes will give the two's complement of the count, preloading the counter with all ones will give the one's complement of the count. The counter decrements on the falling edge of IN3 pin. The counter, counts down and eventually rolls over from 0000 to FFFF (Hex).

The register RB acts as a « capture-latch », being loaded by the counter's value every instruction cycle. Thus, it enables a simple monitoring of the count.

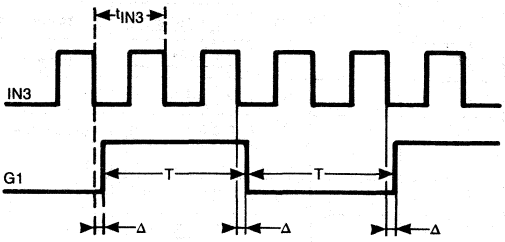
G1 toggles every time counter CB counts through « 0 ».

Frequency generation
This mode generates a square wave on G1. The period is determined by the contents of register RB. Using the autoreload procedure, the counter is only loaded when it counts down through zero. Therefore, it may be necessary to initially load the counter (see nota 1). IN3 has no effect in this mode.



$t = (N + 1)\ t_{CLKB}$; Period $= 2\ (N + 1)\ t_{CLKB}$
Where N = Content of counter RB
$0 \leqslant N \leqslant 2^{16}-1$
t_{CLKB} = Block B clock period

Frequency divider
This mode generates a square wave on G1. The period is determined by the contents of register RB, and by the external frequency applied on IN3 pin. The counter decrements on the high to low transition of IN3 pin. Using the autoreload procedure, the counter is only loaded when it counts down through zero. Therefore, it may be necessary to initially load the counter.



$\Delta = 2{,}5\ t_{CLK}$
$t = (N + 1)\ t_{IN3}$; Period $= 2\ (N + 1)\ t_{IN3}$
Where N = contents of counter RB
$O \leqslant N \leqslant 2^{16}-1$
t_{CLK} = System clock period

Symbol	Definition
Internal Architecture Symbols	
A	4-bit Accumulator
B	8-bit RAM address register
Br	Upper 4 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry register
D	4-bit Data output port
EN	4-bit Enable register
G	4-bit General purpose I/O port
IL	One 1-bit (IN_3) latch
IN	4-bit input port
L	8-bit 3-state I/O port
M	4-bit contents of RAM addressed by B
PC	11-bit ROM address program counter
Q	8-bit latch for L port
SA, SB, SC	11-bit 3-level subroutine stack
SIO	4 bit Shift register
SK	Logic-controlled clock output
SKL	1-bit lach for SK output
T	8-bit timer

Instruction operand symbols	
d	4-bit operand field, 0-15 binary (RAM digit select)
r	3-bit operand field, 0-7 (RAM register select)
a	11-bit operand field, 0-2047 (1023)
y	4-bit Operand field, 0-15 (immediate data)
RAM(x)	RAM addressed by variable x
ROM(x)	ROM addressed by variable x

Operational Symbols	
+	Plus
−	Minus
→	Replaces
↔	is exchanged with
=	is equal to
$\overline{A}$	one's complement of A
⊕	exclusive-or
:	range of values

TS94100 INSTRUCTION SET

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0 0 1 1 | 0 0 0 0	A+C+RAM(B) → A Carry → C	Carry	Add with carry, Skip on Carry
ADD		31	0 0 1 1 | 0 0 0 1	A+RAM(B) → A	None	Add RAM to A
ADT		4A	0 1 0 0 | 1 0 1 0	A+10_{10} → A	None	Add TEN to A
AISC	y	5—	0 1 0 1 | y	A+y → A	Carry	Add Immediate Skip on Carry (y ≠ 0)
CASC		10	0 0 0 1 | 0 0 0 0	$\overline{A}$+RAM(B)+C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	0 0 0 0 | 0 0 0 0	0 → A	None	Clear A
COMP		40	0 1 0 0 | 0 0 0 0	$\overline{A}$ → A	None	Ones complement of A to A
NOP		44	0 1 0 0 | 0 1 0 0	None	None	No Operation
RC		32	0 0 1 1 | 0 0 1 0	"0" → C	none	Reset C
SC		22	0 0 1 0 | 0 0 1 0	"1" → C	None	Set C
XOR		02	0 0 0 0 | 0 0 1 0	A⊕ RAM(B) → A	None	Exclusive-OR RAM with A

INSTRUCTION SET (continued)

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS						
CAMT		33 3F	0011 0011 0011 1111	A → $T_{7:4}$ RAM(B) → $T_{3:0}$	None	Copy A, RAM to T
CTMA		33 2F	0011 0011 0010 1111	$T_{7:4}$ → RAM(B) $T_{3:0}$ → A	None	Copy T to RAM, A
CAMQ		33 3C	0011 0011 0011 1100	A → $Q_{7:4}$ RAM(B) → $Q_{3:0}$	None	Copy A, RAM to Q
CQMA		33 2C	0011 0011 0010 1100	$Q_{7:4}$ → RAM(B) $Q_{3:0}$ → A	None	Copy Q to RAM, A
LD	r	—5	00 r 0101 (r = 0,3)	RAM(B) → A Br ⊕ r → Br	None	Load RAM into A Exclusive-OR Br with r
LDD	r.d	23	0010 0011 0 r d	RAM(r,d) → A	None	Load A with RAM pointed to directly by r, d
LQID		BF	1011 1111	ROM($PC_{10:8}$,A,M) → Q	None	Load Q indirect (Note 3)
RMB	0 1 2 3	40 45 42 43	0100 1100 0100 0101 0100 0010 0100 0011	0 → RAM(B)$_0$ 0 → RAM(B)$_1$ 0 → RAM(B)$_2$ 0 → RAM(B)$_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	0100 1101 0100 0111 0100 0110 0100 1011	1 → RAM(B)$_0$ 1 → RAM(B)$_1$ 1 → RAM(B)$_2$ 1 → RAM(B)$_3$	None	Set RAM Bit
STII	y	7—	0111 y	y → RAM(B) Bd + 1 → Bd	None	Store Memory immediate and increment Bd
TCRA		23 8B	0010 0011 1000 1011	CD → RD 1111 → A CW → RW	None	Transfer Counter to Register (Timer A) (Note 8)
TCRB		23 9B	0010 0011 1001 1011	CB → RB 1111 → A	None	Transfer Counter to Register (Timer B) (Note 8)
TMB		33 35	0011 0011 0011 0101	$\overline{Br3}$ → B_r3	None	One's complement of B_r3 to B_r3 (Toggle memory bank)
TRCA		23 8A	0010 0011 1000 1010	RD → CD 1111 → A RW → CW	None	Transfer Register to Counter (Timer A) (Note 8)
TRCB		23 9A	0010 0011 1001 1010	RB → CB 1111 → A	None	Transfer Register to Counter (Timer B) (Note 8)
X	r	—6	00 r 0110 (r = 0,3)	RAM(B) ↔ A Br ⊕ r → Br	None	Exchange RAM with A Exclusive OR Br with r
XAD	rd	23	0010 0011 1 r d	RAM(r,d) ↔ A	None	Exchange A with RAM pointed to directly by r d
XDS	r	—7	00 r 0111 (r = 0,3)	RAM(B) ↔ A Bd-1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd . Exclusive Or Br with r
XIS	r	—4	00 r 0100 (r = 0,3)	RAM(B) ↔ A Bd + 1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and increment Bd Exclusive Or Br with r

INSTRUCTION SET (continued)

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1 1 1 1 | 1 1 1 1	ROM($PC_{10:8}$ A,M) → $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6 -	0 1 1 0 | 0 | $a_{10:8}$	a → PC	None	Jump
		- -	$a_{7:0}$			
JP	a	- -	1 | $\overline{a_{6:0}}$ (pages 2, 3, only) or	a → $PC_{6:0}$	None	Jump within Page (Note 4)
		- -	1 1 | $a_{5:0}$ (all other pages)	a → $PC_{5:0}$		
JSRP	a	- -	1 0 | $a_{5:0}$	PC+1 → SA → SB → SC 00010 → $PC_{10:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6 -	0 1 1 0 | 1 | $a_{10:8}$	PC+1 → SA → SB → SC	None	Jump to Subroutine
			$a_{7:0}$	a → PC		
RET		48	0 1 0 0 | 1 0 0 0	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0 1 0 0 | 1 0 0 1	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0 1 0 1 | 0 0 0 0	A → Bd	None	Copy A to Bd
CBA		4E	0 1 0 0 | 1 1 1 0	Bd → A	None	Copy Bd to A
LBI	r,d	- -	0 0 | r | (d-1) (r=0:3) (d=0,9:15) or	r,d → B	Skip until not a LBI	Load B immediate with r,d (Note 6)
		33	0 0 1 1 | 0 0 1 1			
		- -	1 | r | d (any r, any d)			
LEI	y	33	0 0 1 1 | 0 0 1 1	y → EN	None	Load EN Immediate (Note 7)
		6 -	0 1 1 0 | y			
XABR		12	0 0 0 1 | 0 0 1 0	A↔ Br 0 → A_3	None	Exchange A with Br
TEST INSTRUCTIONS						
SKC		20	0 0 1 0 | 0 0 0 0		C="1"	Skip if C is True
SKE		21	0 0 1 0 | 0 0 0 1		A=RAM(B)	Skip if A Equals RAM
SKGZ		33	0 0 1 1 | 0 0 1 1		$G_{3:0}$=0	Skip if G is Zero
		21	0 0 1 0 | 0 0 0 1			(all 4 bits)
SKGBZ		33	0 0 1 1 | 0 0 1 1	1st byte		Skip if G Bit is Zero
	0	01	0 0 0 0 | 0 0 0 1	2nd byte	G_0=0	
	1	11	0 0 0 1 | 0 0 0 1		G_1=0	
	2	03	0 0 0 0 | 0 0 1 1		G_2=0	
	3	13	0 0 0 1 | 0 0 1 1		G_3=0	

INSTRUCTION SET (continued)

Mnemonic	Operand	Hx Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
SKMBZ	0	01	0 0 0 0 | 0 0 0 1		$RAM(B)_0 = 0$	Skip if RAM Bit is Zero
	1	11	0 0 0 1 | 0 0 0 1		$RAM(B)_1 = 0$	
	2	03	0 0 0 0 | 0 0 1 1		$RAM(B)_2 = 0$	
	3	13	0 0 0 1 | 0 0 1 1		$RAM(B)_3 = 0$	
SKT		41	0 1 0 0 | 0 0 0 1		A time-base counter carry has occured since last test	Skip on Timer (Note 3)
INPUT/OUTPUT INSTRUCTIONS						
ING		33	0 0 1 1 | 0 0 1 1	G → A	None	Input G Ports to A (Note 9)
		2A	0 0 1 0 | 1 0 1 0			
ININ		33	0 0 1 1 | 0 0 1 1	IN3, IN2, IN1, "0"→A	None	Input IN inputs to A
		28	0 0 1 0 | 1 0 0 0			
INIL		33	0 0 1 1 | 0 0 1 1	IL_3, CKO, "0", "0" → A	None	Input IL_3 Latch to A (Note 3)
		29	0 0 1 0 | 1 0 0 1			
INL		33	0 0 1 1 | 0 0 1 1	$L_{7:4}$→ RAM(B)	None	Input L Ports to RAM, A
		2E	0 0 1 0 | 1 1 1 0	$L_{3:0}$→ A		
OBD		33	0 0 1 1 | 0 0 1 1	Bd → D	None	Output Bd to D Outputs
		3E	0 0 1 1 | 1 1 1 0			
OGI	y	33	0 0 1 1 | 0 0 1 1	Y2→G2 Y3→G3	None	Output to G Ports
		5 -	0 1 0 1 | y			Immediate
OMG		33	0 0 1 1 | 0 0 1 1	$RAM(B)_2 \rightarrow G_2$ $RAM(B)_3 \rightarrow G_3$	None	Output RAM to G Ports
		3A	0 0 1 1 | 1 0 1 0			
XAS		4F	0 1 0 0 | 1 1 1 1	A ↔ SIO, C → SKL	None	Exchange A with SIO (Note 3)

Note 1 : All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 3 : For additional on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4 : The JP instruction allows a jump, while in subroutine page 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5 : A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6 : LBI is a single-byte instruction if d=0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the "d" data minus 1, e.g., to load the lower four bits of B (Bd) with the value $9(1001_2)$, the lower 4 bits of the LBI instruction equal $8\ (1000_2)$. To load 0, the lower 4 bits of the LBI instruction should equal $15\ (1111_2)$.

Note 7 : Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register).

Note 8: All transfer instructions (TRCA, TCRA, TRCB, TCRB) must be selected when $B_r3 = 1$. If $B_r3 = 0$, these transfer instructions will be decoded as XAD instruction.

Note 9: G0 and G1 can be used as inputs only with options 34.1 and 35.2.

DESCRIPTION OF SELECTED INSTRUCTIONS

XAS Instruction

XAS (Exchange A with SIO) copies C to the SKL latch and exchanges the accumulator with the 4-bit contents of the SIO serial-in/serial-out shift register. An XAS instruction can be performed once every 4 instruction cycles to effect a continuous data stream.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC_{10}: PC_8, A,M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction « pushes » the stack (PC + 1 → SA → SB → SC) and replaces the least significant 8 bits of the PC as follows: A → $PC_{7:4}$, $RAM_{(B)}$ → $PC_{3:0}$, leaving PC_{10}, PC_9 and PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is « popped » (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB into SC, the previous contents of SC are lost.

Note: LQID uses 2 instruction cycles if executed, one if skipped.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 11-bit word, $PC_{10:8}$, A,M. PC_{10}, PC_9 and PC_8 are not affected by JID.

Note: JID uses 2 instruction cycles if executed, one if skipped.

SKT Instruction

The SKT (Skip On Timer) instruction tests the state of the T counter overflow latch (see internal logic, above), executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction allow the processor to generate its own time-base for real-time processing, rather than relying on an external input signal.

SKT can be used (when the option selected for CPU interrupt source is the timer overflow) during the interrupt service routine to clear the overflow latch.

INIL Instruction

INIL (Input IL Latch to A) inputs latch IL3, CKO and 0 into A. The IL3 latch is set if a low-going pulse (« 1 » to « 0 ») has occured on the IN3 input since the last INIL instruction, provided the input pulse stays low for at least two instruction cycles. Execution of an INIL inputs IL 3 into A3, and resets this latch to allow it to respond to subsequent low-going pulses on the IN3. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a « 1 » will be placed in A2. A1 and A0 are cleared. IL latch is cleared on reset.

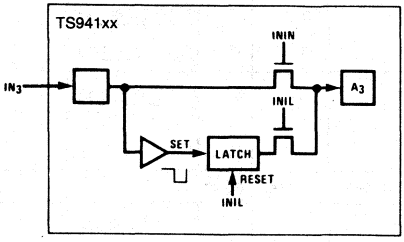


FIGURE 14: INIL HARDWARE IMPLEMENTATION

RET and RETSK Instructions

When a RET instruction is executed at the end of the interrupt subroutine, it restores the state of bit Br3 that was saved at the beginning of the interrupt subroutine. When used at the end of a software subroutine, a RET instruction will clear bit Br3. The RETSK instruction never modifies bit Br3.

Instruction set notes

- The first word of a program (ROM address 0) must be a CLRA (Clear A) instruction.
- Although skipped instructions are not executed, they are still fetched from the program memory. Thus program paths take the same number of cycles whether instructions are skipped or executed except for JID, and LQID.
- The ROM is organized into pages of 64 words each. The Program Counter is a 11-bit binary counter, and will count through page boundaries. If a JP is the last word of a page, it operates as if it were in the next page. For example, a JP Located in the last word of a page will jump to a location in the next page. JID or LQID located in the last word of every fourth page (i.e. hex address 0FF, 1FF, 2FF, 3FF, 4FF, etc.) will access data in the next group of four pages.

Note: TS94120 needs only 10 bits to address its ROM. Therefore, the eleventh bit (10) is ignored.

MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Input voltage IN0 SI	VI	— —0.8 to +10 —0.5 to +14	V
Voltage on any other Pin		—0.5 to +10	
Ambient operating temperature TS94100CP TS94100TP	T_A	 0 to +70 —40 to +85	 °C °C
Ambient storage temperature	T_{stg}	—65 to + 150	°C
Lead temperature (soldering 10s)		300	°C
Power dissipation T_A = +25°C T_A = +70°C	P_D	 1 550	 W mW
Total source current		36	mA
Total sink current		200	mA

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Unless otherwise specifed)

Characteristic	Symbol	Min	Typ	Max	Unit
Power supply ripple (peak to peak) - Note A	V_{ppl}	—	—	0.5	V
Operating supply current (all inputs set to 1) (all outputs set to 1) (all inputs set to 1) (all outputs set to 0)	I_{CC}	— —	— —	15 15.5	mA
INPUT					
CKI input level Crystal or RC Logic high Logic low External clock Logic high Logic low	 V_{IH} V_{IL} V_{IH} V_{IL}	 0.5V_{CC} — 0.7V_{CC} —	 — — — —	 — 1 — 0.2	 V V
$\overline{\text{RESET}}$ and WATCHDOG (D3) SCHMITT trigger input level Logic high Logic low	 V_{IH} V_{IL}	 0.7V_{CC} —	 — —	 — 0.6	 V
IN0 offset voltage (note B, Fig. 15)		—	—	150	mV
Input level on all other inputs With TTL option selected Logic high Logic low With high voltage option selected Logic high Logic low	 V_{IH} V_{IL} V_{IH} V_{IL}	 2 — 3.6 —	 — — — —	 — 0.8 — 1.2	 V V V V
Input capacitance	C_I	—	—	7	pF
High impedance input leakage	I_I	—2	—	+2	µA
OUTPUT					
TTL load Logic high (I_{OH} = —100µA) Logic low (I_{OL} = 1.6 mA)	 V_{OH} V_{OL}	 2.4 —	 — —	 — 0.4	 V V
CMOS load Logic high (I_{OH} = —10µA) Logic low (I_{OL} = +10µA)	V_{OH} V_{OL}	0.7V_{CC} —	— —	— 0.2	V V

OUPUT SINK CURRENT

Characteristic	Symbol	Min	Typ	Max	Unit
SO,SK and L0-7 outputs with TTL option					
(V_{CC} = 5.5V, V_{OL} = 0.4V)	I_{OL}	2	4.6	10	mA
(V_{CC} = 4.5V, V_{OL} = 0.4V)	I_{OL}	1.6	4	9	mA
G1-G3, D0-D3, L0-L7 outputs with very high current option					
(V_{CC} = 5.5V, V_{OL} = 1.0V)	I_{OL}	17	28	40	mA
(V_{CC} = 4.5V, V_{OL} = 1.0V)	I_{OL}	15	25	40	mA
G0 output (Triac driver)					
V_{CC} = 5.5V, V_{OL} = 2.0V	I_{OL}	50	70	90	mA
V_{CC} = 4.5V, V_{OL} = 1.0V	I_{OL}	28	40	46	mA
CKI (Single-pin RC oscillator)					
V_{CC} = 4.5V, V_{IH} = 3.5V	I_{IH}	2	4,6	10	mA

OUTPUT SOURCE CURRENT

G2, G3, D0-D3 standard output and SO, SK output with TTL option					
V_{CC} = 5.5V, V_{OH} = 2.0V	I_{OH}	−250	−700	−1900	µA
V_{CC} = 4.5V, V_{OH} = 2.0V	I_{OH}	−100	−350	−1000	µA
SO, SK outputs with high current option, G0, G1 and L0-L7 outputs					
V_{CC} = 5.5V, V_{OH} = 2.0V	I_{OH}	−1.2	−2.8	−7	mA
V_{CC} = 4.5V, V_{OH} = 1.0V	I_{OH}	−1.2	−2.8	−7	mA
Input load source current					
V_{CC} = 5.5V, V_{IL} = 0V	I_{IL}	−11	−45	−150	µA
V_{CC} = 4.5V, V_{IL} = 0V	I_{IL}	−10	−45	−150	µA

Characteristic	Symbol	Min	Typ	Max	Unit
3-State Output leakage current (Available on L only)	I_L	—	−5	+5	µA
Total Sink Current allowed					
All outputs combined	ΣI_{sink}	—	—	200	mA
D, G Ports		—	—	120	
L Port		—	—	160	
each L0-L7, G1-G3, D0-D3 pin		—	—	30	
G0 pin		—	—	60	
Each other pin		—	—	5	
Total Source Current allowed					
All I/O combined	ΣI_{source}	—	—	36	mA
Each L0-L7, G0, G1, SO, SK pin		—	—	4	
All other pins combined		—	—	4	

Note A: V_{CC} change must be less than 0.5V in a 1ms period to maintain proper operations.

Note B: IN0 Offset Voltage is the absolute value of the difference between the voltage at IN0 and GROUND.

MCU AND DUAL TIMER ELECTRICAL CHARACTERISTICS

$0°C \leqslant T_A \leqslant 70°C$; $4.5V \leqslant V_{CC} \leqslant 5.5V$ (Unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Instruction cycle time						
XTAL (Fig. 16)	÷ 20 (option 4.2)	t_c	4	—	11	µs
	÷ 10 (option 4.1)	t_c	4	—	11	µs
	÷ 5 (option 4.0)	t_c	5	—	11	µs
RC Oscillator	÷ 10 (option 4.1)	t_c	4	—	11	µs
External clock	÷ 10 (option 4.1)					
Rise time, fall time on CKI input (External waveform generator on CKI)	÷ 10 mode	t_r, t_f	—	—	50	ns
CKI duty cycle (Fig. 17)			0.4	—	0.6	
Input set up time	All inputs	$t_{set\ up}$	$t_c/10 + 1.3$	—	—	µs
Input hold time	All inputs	t_{hold}	100	—	—	ns
Output propagation delay (Load = one TTL load)						
SK (EN0 = 0, SK = 1)		t_{s1}, t_{s0}	—	—	2	µs
SK as an output (SK = 0)		t_{pd1}, t_{pd0}	$-t_c/10$	—	0.6	µs
SO as an output (EN0, EN3) = (00, 10, 11)		t_{pd1}, t_{pd0}	$-t_c/10$	—	0.6	µs
SO as SIO output (EN0, EN3) = 01		t_{pd1}, t_{pd0}	$t_c/10$	—	$t_c/5 + 0.6$	µs
All other outputs		t_{pd1}, t_{pd0}	$-t_c/10$	—	1.0	µs
G0, G1 rise time		t_{LH}	—	—	1.0	µs
G0, G1 fall time		t_{HL}	—	—	200	ns

Dual timer

System clock (Fig. 19)		f_{CLK}	450	—	1250	kHz
Timer A and timer B Prescaler	÷ 1	f_{CLKA}, f_{CLKB}	450	—	1250	kHz
Prescaler	÷ 5	f_{CLKA}, f_{CLKB}	90	—	250	kHz
Prescaler	÷ 20	f_{CLKA}, f_{CLKB}	22,5	—	62,5	kHz
Prescaler	÷ 40	f_{CLKA}, f_{CLKB}	11250	—	31250	Hz
IN0, IN3 INPUT						
All modes		f_{IN0}, f_{IN3}	0	—	$f_{CLK/2}$	—
IN0 in analog period counter mode			0	—	$1/2t_c$	—

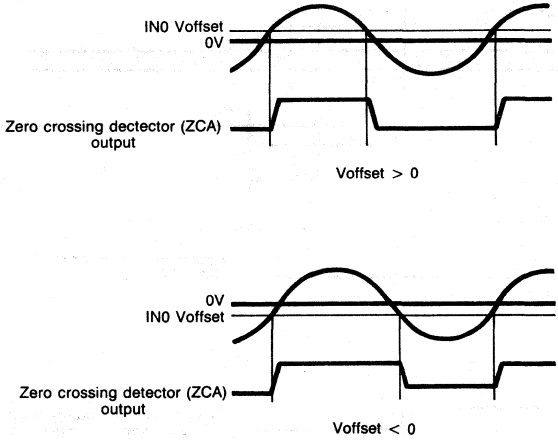


FIGURE 15: ZERO CROSSING DETECTOR OUTPUT

Characteristic	Symbol	Min	Typ	Max	Unit
External C value External R value (C = 250pF)	C R	250 4	—	— 8	pF kΩ
External C values f_{CKI} = 5 MHz	C1 C2	— —	15 15	— —	pF pF
f_{CKI} = 455 kHz	C1 C2	— —	30 30	— —	pF pF

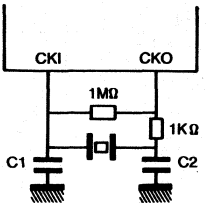


FIGURE 16

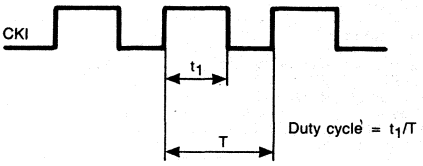
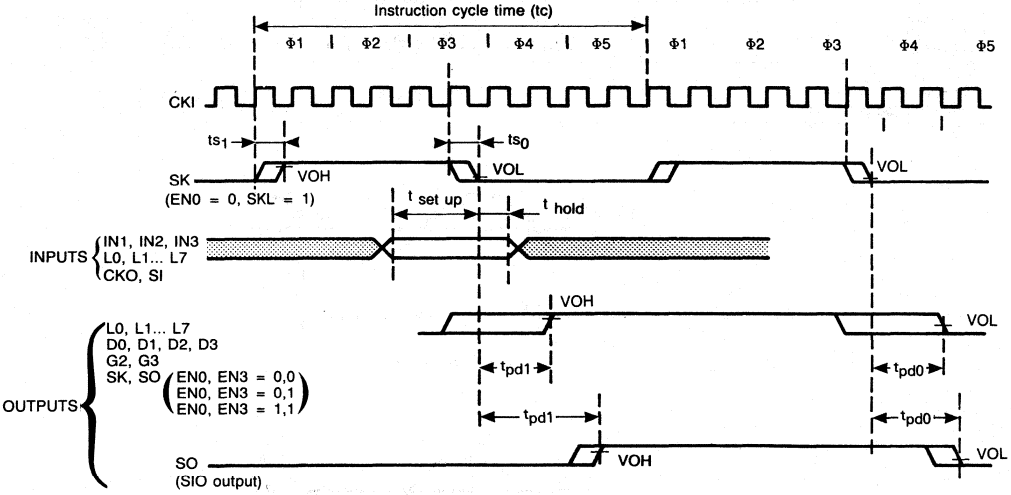
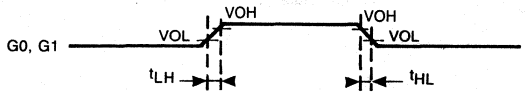


FIGURE 17





SK is a 0.5 duty cycle signal.
Inputs are sampled (by MCU) on the falling edge of SK.
Outputs may be sampled on the rising edge fo SK.

Note that Φ1, Φ2, Φ3, Φ4, Φ5 are MCU internal.

FIGURE 18: I/O TIMINGS (÷ 10 MODE)

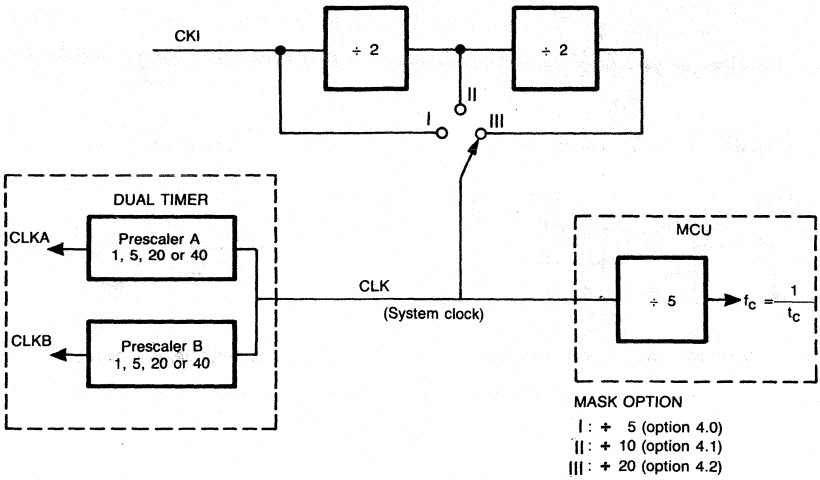


FIGURE 19: PRESCALERS MASK-OPTIONS

I/O OPTIONS

TS94100 outputs have the following optional configurations illustrated by figure 20:

a. General purpose - an enhancement-mode device to ground in conjunction with a depletion-mode paralleled by an enhancement-mode device to Vcc.
On G2-G3 and SO-SK with TTL option, this configuration is compatible with TTL and CMOS input requirements. On G1 and SO-SK with high current option, it allows fast rising and falling edges when driving capacitive loads. On G0, the enhancement-mode device to ground meets the typical current sinking requirements to directly trigger a triac.

b. Open-drain - an enhancement mode device to ground only, allowing external pull-up, as required by the user's application. Available on SO, SK, D, G2-G3 outputs.

c. 3-state general purpose - same as **a.**, but may be disabled.
The sinking devices meet the typical current sinking requirements of a LED display. These devices may be turned off under program control (see functional description, EN register) in a high-impedance state to provide required LED segments blanking for a multiplexed display. Available on L outputs only.

d. Open-drain L - same as **b.** but may be disabled - available on L only.

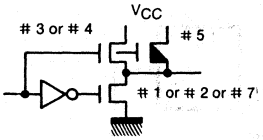
e. 3-state push-pull - an enhancement-mode device to ground and V_{CC}. Available on L outputs only.

TS94100 inputs have the following optional configurations:

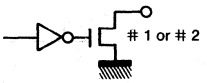
f. An on-chip depletion load device to Vcc.

g. A Hi-Z input which must be driven to a « 1 » or « 0 » by external components.

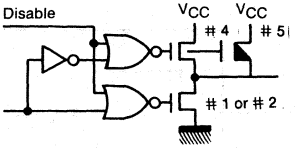
OUTPUT CONFIGURATIONS



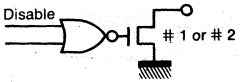
a. GENERAL PURPOSE OUPTUT



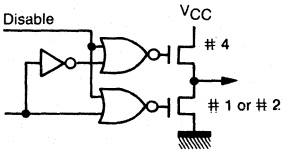
b. OPEN DRAIN OUTPUT



c. 3 STATE GENERAL PURPOSE L OUTPUT



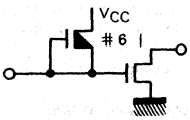
d. OPEN DRAIN L OUTPUT



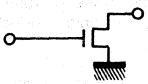
e. 3-STATE PUSH-PULL L OUTPUT

FIGURE 20

INPUT CONFIGURATIONS



f. INTPUT WITH LOAD



g. Hi-Z INPUT

FIGURE 21

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of 7 devices (numbered # 1 to # 7 respectively).

The SO, SK, D, G2-G3 outputs can be configured as shown in **a, b.**

The G0-G1 are configured as general purpose output, as shown in **a.**

Note that when inputing data to the G ports, the G outputs should be set to a « 1 ». The L outputs can be configured as shown in **c, d, e.**

An important point to remember if using configuration **c** with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current (see figure 20 device 5) ; however, when the L lines are used as inputs, the disabled depletion device cannot source a sufficient current to pull up an external input to a logic 1.

IN0 is configured as an Hi-Z input.

Output	Output scheme	Mask option	Transistor type 1	2	3	4	5	7
SO, SK	**a**	opt. 9-0	•		•		•	
	a	opt. 9-1	•			•	•	
	b	opt. 9-2	•					
G2, G3 D0, D1, D2, D3	**a**	opt. 20-0		•	•		•	
	b	opt. 20-1		•				
G0	**a**					•	•	•
G1	**a**			•		•	•	
L0, L1... L7	**c**	opt. 11-0	•			•	•	
	c	opt. 11-1		•		•	•	
	d	opt. 11-2	•					
	d	opt. 11-3		•				
	e	opt. 11-4	•			•		
	e	opt. 11-5		•		•		

OPTION LIST

OPTION 1: CKO Pin configuration
0: clock generator output to crystal/resonator
1: general purpose input, load device to Vcc
2: general purpose input, high-Z

OPTION 2: CKO intput levels
0: standard TTL input levels (0 = 0.8V, 1 = 2.0V)
1 : higher voltage input levels (0 = 1.2V, 1 = 3.6V)

OPTION 3: CKI input configuration
0: single pin RC controlled oscillator (option 4 must be ÷ 10)
1: crystal input
2: external clock (option 4 must be ÷ 10)

OPTION 4: CKI divider
0: CKI frequency divided by 5
1: CKI frequency divided by 10
2: CKI frequency divided by 20

OPTION 5: Reset pin configuration
0: load device to Vcc
1: high-Z input

OPTION 6: IN input configuration (IN1-IN3)
0: load device to Vcc
1: high-Z input

OPTION 7: IN input levels (IN1-IN3)
0: standard TTL input levels (0 = 0.8V, 1 = 2.0V)
1: higher voltage input levels (0 = 1.2V, 1 = 3.6V)

* **Note:** IN0 has no option

OPTION 8: SI input levels
0: standard TTL input levels (0 = 0.8V, 1 = 2.0V)
1: higher voltage input levels (0 = 1.2V, 1 = 3.6V)

OPTION 9: SO output configuration
0: general purpose TTL output
1: general purpose high current output
2: open drain output

OPTION 10: SK output configuration
same as OPTION 9

OPTION 11: L0 output driver
0: 3-state general purpose TTL output
1: 3-state general purpose very high current output
2: open drain TTL output
3: open drain very high current output
4: 3-state push-pull TTL output
5: 3-state push-pull very high current output

OPTION 12: L1 output driver
same as OPTION 11

OPTION 13: L2 output driver
same as OPTION 11

OPTION 14: L3 output driver
same as OPTION 11

OPTION 15: L4 output driver
same as OPTION 11

OPTION 16: L5 output driver
same as OPTION 11

OPTION 17: L6 output driver
same as OPTION 11

OPTION 18: L7 output driver
same as OPTION 11

OPTION 19: L input level L0-L7
0: standard TTL input levels (0 = 0.8V, 1 = 2.0V)
1: higher voltage input levels (0 = 1.2V, 1 = 3.6V)

OPTION 20: G2 output driver
0: general purpose output
1: open drain output

OPTION 21: G3 output driver
same as OPTION 20

OPTION 22: G input level (G0-G3)
0: standard TTL input levels (0 = 0.8V, 1 = 2V)
1: higher voltage input levels (0 = 1.2V, 1 = 3.6V)

OPTION 23: DO output configuration
same as OPTION 20

OPTION 24: D1 output configuration
same as OPTION 20

OPTION 25: D2 output configuration
same as OPTION 20

OPTION 26: D3 output configuration
same as OPTION 20

OPTION 27: CPU interrupt source
0: external interrupt
1: timer overflow

OPTION 28: timer input
0: prescaler output
1: event counter

OPTION 29: watchdog
0: no watchdog
1: D3 pin as watchdog input (OPTION 26 must be open drain)

OPTION 30: Dual timer block A clock (CLKA)
0: system clock (CLK) divided by 1
1: system clock (CLK) divided by 5
2: system clock (CLK) divided by 20
3: system clock (CLK) divided by 40

OPTION 31: Dual timer block B clock (CLKB)
0: system clock (CLK) divided by 1
1: system clock (CLK) divided by 5
2: system clock (CLK) divided by 20
3: system clock (CLK) divided by 40

OPTION 32: Dual timer interrupt source (block A)
0: zero crossing detector output falling edge (ZCA)
1: zero crossing detector output rising edge and falling edge (ZCA)

OPTION 33: Mode selection for MRB0 = 0 and MRB1 = 0
0: period measurement
1: duty cycle measurement

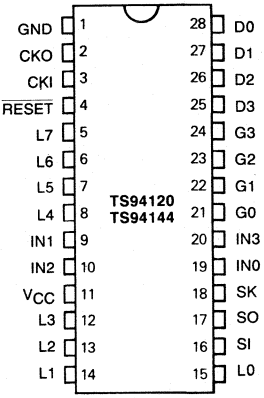
OPTION 34: G0 output for STA = 0
0: logical 0
1: logical 1

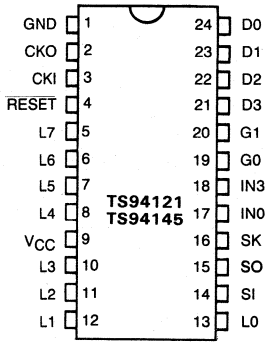
OPTION 35: G1 output for STB = 0 or when G1 is disabled (see CSB on fig. 14)
0: logical 0
1: logical 1

PIN ASSIGNMENTS

PIN NAMES

L7 - L0	8 bi-directionnal I/O ports with 3-state output
G3 - G2	2 bi-directionnal I/O ports
G0 - G1	2 dual timer peripheral outputs or 2 general purpose inputs
IN0	Dual timer peripheral analog input (Zero crossing detector input)
IN1-IN2	2 general purpose inputs
IN3	General purpose or dual timer peripheral input
SI	Serial input
SO	Serial output (or general purpose output)
D0 - D2	3 general purpose outputs
D3	General purpose output (or watch dog input)
SK	Logic controlled clock (or general purpose output)
CKI	Oscillator input
CKO	Oscillator output (or general purpose input)
$\overline{\text{RESET}}$	RESET input
Vcc	Power supply
GND	Ground





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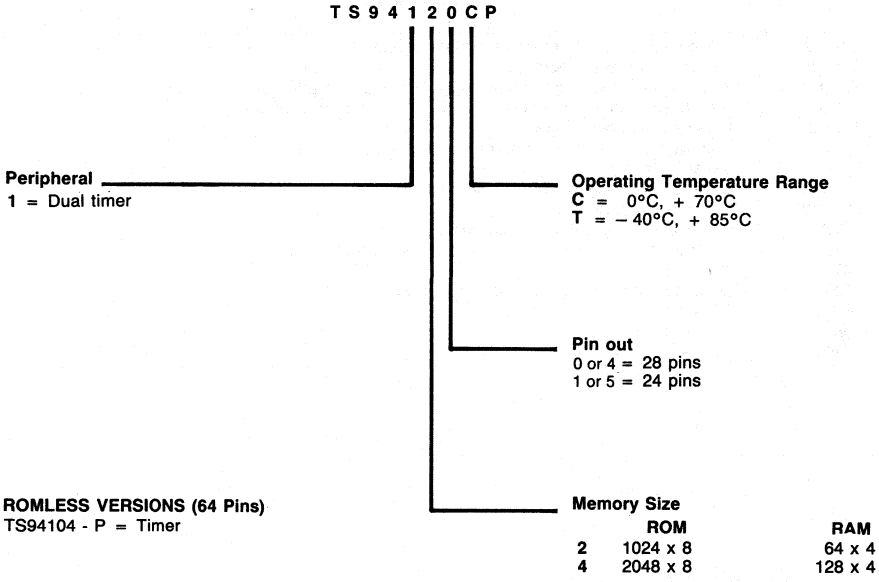

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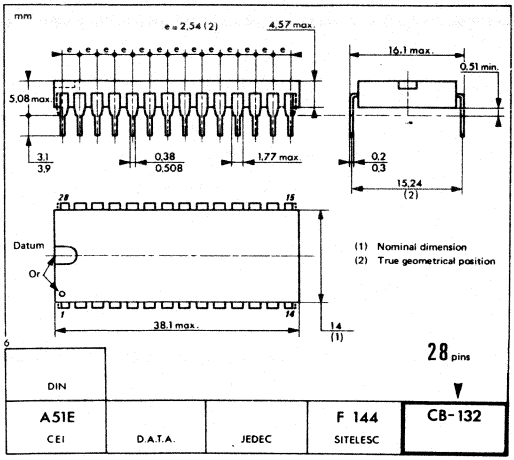

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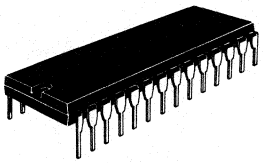

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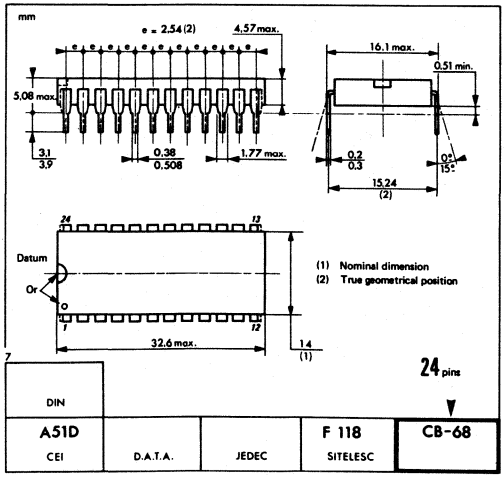

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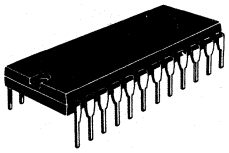

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EF6804J2

8 BIT MICROCOMPUTER

ADVANCE INFORMATION

The EF6804J2 microcomputer unit (MCU) is a member of the EF6804 Family of very low-cost single-chip microcomputers. This 8-bit microcomputer contains a CPU, on-chip CLOCK, ROM, RAM, I/O, and TIMER. It is designed for the user who needs an economical microcomputer with the proven capabilities of the EF6800-based instruction set.

The following are some of the hardware and software features of the EF6804J2 MCU.

HARDWARE FEATURES

- 5-Volt Single Supply
- 32 Bytes of RAM
- Memory Mapped I/O
- 1012 Bytes of Program ROM
- 64 Bytes of Data ROM
- 12 Bidirectional I/O Lines (Eight Lines with High Current Sink Capability)
- On-Chip Clock Generator
- Self-Test Mode
- Master Reset
- Complete Development System Support on DEVICE®
- Software Programmable 8-Bit Timer Control Register and Timer Prescaler (7 Bits, 2n)
- Timer Pin is Programmable as Input or Output
- On-Chip Circuit for ROM Verify.

SOFTWARE FEATURES

- Similar to EF6805 HMOS Family
- Byte Efficient Instruction Set
- Easy to Program
- True Bit Manipulation
- Bit Test and Branch Instruction
- Separate Flags for Interrupt and Normal Processing
- Versatile Indirect Registers
- Conditional Branches
- Single Instruction Memory Examine/Change
- True LIFO Stack Eliminates Stack Pointer
- Nine Powerful Addressing Modes
- Any Bit in Data Space Memory May be Tested
- Any Bit in Data Space Memory Capable of Being Written to May be Set or Cleared

USER SELECTABLE OPTIONS

- 12 Bidirectional I/O Lines with LSTTL, LSTTL/CMOS, or Open-Drain Interface
- Crystal or Low-Cost Resistor-Capacitor Oscillator
- Mask Selectable Edge- or Level- Sensitive Interrupt Pin.

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HMOS

HIGH DENSITY
N CHANNEL, SILICON-GATE
DEPLETION LOAD

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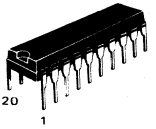

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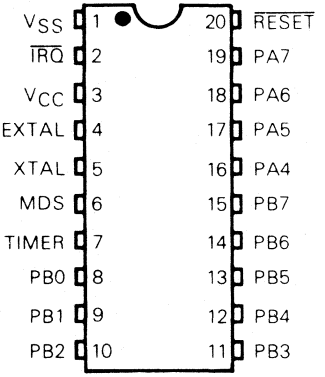
PIN ASSIGNMENT



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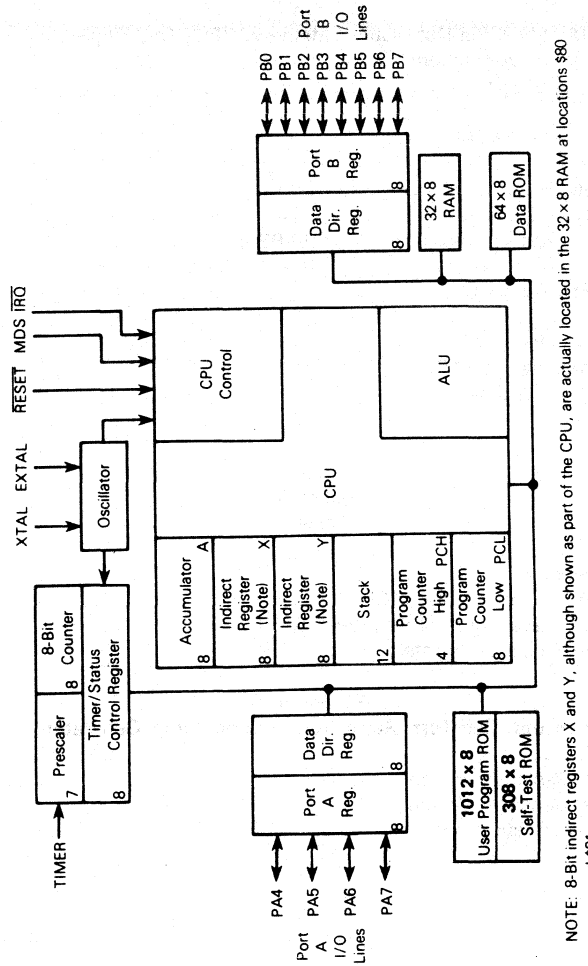

NOTE: 8-Bit indirect registers X and Y, although shown as part of the CPU, are actually located in the 32 x 8 RAM at locations $80 and $81.

Figure 1-1. EF6804J2 MCU Block Diagram

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SECTION 2
FUNCTIONAL PIN DESCRIPTION, MEMORY, CPU, AND REGISTERS

This section provides a description of the functional pins, memory spaces, the central processing unit (CPU), and the various registers and flags.

2.1 FUNCTIONAL PIN DESCRIPTION

2.1.1 V_{CC} and V_{SS}

Power is supplied to the MCU using these two pins. V_{CC} is power and V_{SS} is the ground connection.

2.1.2 $\overline{IRQ}$

This pin provides the capability for asynchronously applying an external interrupt to the MCU. Refer to **4.1 INTERRUPT** for additional information.

2.1.3 XTAL and EXTAL

These pins provide connections to the on-chip clock oscillator circuit. A crystal, a resistor and capacitor, or an external signal, depending on the user selectable manufacturing mask option, can be connected to these pins to provide a system clock source with various stability/cost tradeoffs. Lead lengths and stray capacitance on these two pins should be minimized. Refer to **4.4 INTERNAL CLOCK GENERATOR OPTIONS** for recommendations concerning these inputs.

2.1.4 TIMER

In the input mode, the timer pin is connected to the prescaler input and serves as the timer clock. In the output mode, the timer pin signals that a time out of the timer has occurred. Refer to **SECTION 3 TIMER** for additional information.

2.1.5 $\overline{RESET}$

The $\overline{RESET}$ pin is used to restart the processor of the EF6804J2 to the beginning of a program. This pin, together with the MDS pin, is also used to select the operating mode of the EF6804J2. If the MDS pin is at zero volts, the normal mode is selected and the program counter is loaded with the user restart vector. However, if the MDS pin is at +5 volts, then pins PA6 and PA7 are decoded to allow selection of the operating mode. Refer to **4.3 RESET** for additional information.

2.1.6 MDS

The MDS (mode select) pin is used to place the MCU into special operating modes. If MDS is held at +5 volts at the exit of the reset state, the decoded state of PA6 and PA7 is latched to determine the operating mode (single-chip, self-test, or ROM verify). However, if MDS is held at zero volts at the exit of the reset state, the single-chip operating mode is automatically selected (regardless of PA6 and PA7 state).

For those users familiar with the EF6801 microcomputer, mode selection is similar but much less complex in the EF6804J2. No special external diodes, switches, transistors, etc. are required in the EF6804J2.

2.1.7 Input/Output Lines (PA4-PA7, PB0-PB7)

These 12 lines are arranged into one 4-bit port (A) and one 8-bit port (B). All lines are programmable as either inputs or outputs under software control of the data direction registers. Refer to **SECTION 5 INPUT/OUTPUT PORTS** for additional information.

2.2 MEMORY

The MCU operates in three different memory spaces: program space, data space, and stack space. A representation of these memory spaces is shown in Figure 2-1. The program space (Figure 2-1a) contains all of the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, and the self-test and user vectors. The data space (Figure 2-1b) contains all of the RAM locations, plus I/O locations and some ROM used for storage of tables and constants. The stack space (Figure 2-1c) contains RAM which is used for stacking subroutine and interrupt return addresses.

The MCU is capable of addressing 4096 bytes of program space memory with its program counter and 256 bytes of data space memory with its instructions. The data space memory contains three bytes for port data registers, three bytes for port data direction registers, one byte for timer status/control, 64 bytes ROM, 32 bytes RAM (which includes two bytes for X and Y indirect registers), two bytes for timer prescaler and count registers, and one byte for the accumulator. The program space section includes 304 bytes of self-test ROM, 1008 bytes program ROM, and eight bytes of vectors for self-test and user programs.

2.3 CENTRAL PROCESSING UNIT

The CPU of the EF6804 Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control buses.

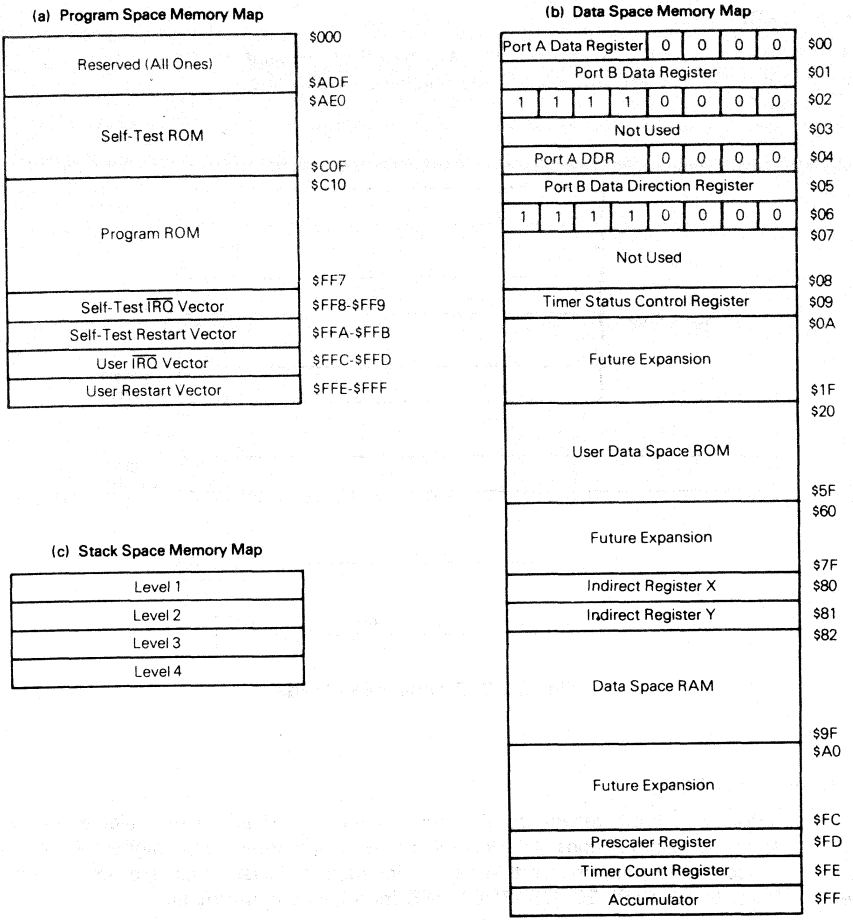


Figure 2-1. EF6804J2 MCU Address Map

2.4 REGISTERS

The EF6804 Family CPU has four registers and two flags available to the programmer. They are shown in Figure 2-2 and are explained in the following paragraphs.

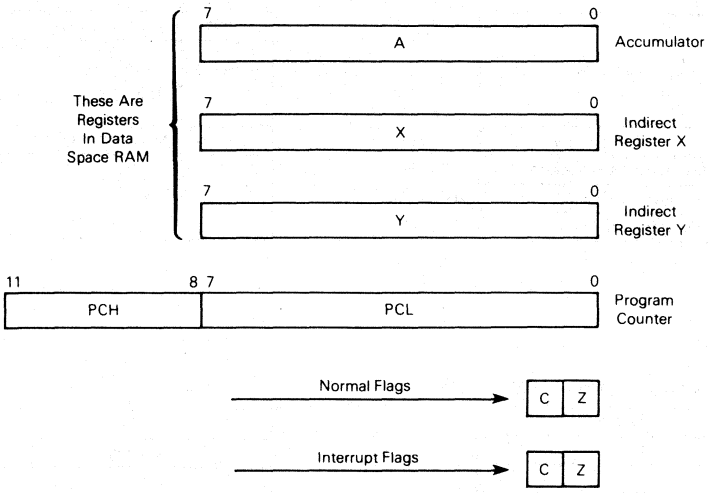


Figure 2-2. Programming Model

2.4.1 Accumulator (A)

The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator is implemented as the highest RAM location ($FF) in data space and thus implies that several instructions exist which are not explicitly implemented. Refer to **6.3 IMPLIED INSTRUCTIONS** for additional information.

2.4.2 Indirect Registers (X, Y)

These two indirect registers are used to maintain pointers to other memory locations in data space. They are used in the register-indirect addressing mode, and can be accessed with the direct, indirect, short direct, or bit set/clear addressing modes. These registers are implemented as two of the 32 RAM locations ($80, $81) and as such generate implied instructions and may be manipulated in a manner similar to any RAM memory location in data space. Refer to **6.3 IMPLIED INSTRUCTIONS** for additional information.

2.4.3 Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next ROM word to be used (may be opcode, operand, or address-of operand). The 12-bit program counter is contained in PCL (low byte) and PCH (high nibble).

2.4.4 Flags (C, Z)

The carry (C) bit is set on a carry or a borrow out of the ALU. It is cleared if the result of an arithmetic operation does not result in a carry or a borrow. The (C) bit is also set to the value of the bit tested in a bit test instruction, and participates in the rotate left instruction.

The zero (Z) bit is set if the result of the last arithmetic or logical operation was equal to zero, otherwise it is cleared.

There are two sets of these flags, one set is for interrupt processing, the other for all other routines. When an interrupt occurs, a context switch is made from the program flags to the interrupt flags (interrupt mode). An RTI forces the context switch back to the program flags (program mode). While in either mode, only the flags for that mode are available. Further, the interrupt flags will not be cleared upon entering the interrupt mode. Instead, the flags will be as they were at the exit of the last interrupt mode. Both sets of flags are cleared by reset.

2.4.5 Stack

There is a true LIFO stack incorporated in the EF6804J2 which eliminates the need for a stack pointer. Stack space is implemented in separate RAM (12-bits wide) shown in Figure 2-1c. Whenever a subroutine call (or interrupt) occurs, the contents of the PC are shifted into the top register of the stack. At the same time (same cycle), the top register is shifted to the next level deeper. This happens to all registers with the bottom register falling out the bottom of the stack.

Whenever a subroutine or interrupt return occurs, the top register is shifted into the PC and all lower registers are shifted up one level higher. The stack RAM is four levels deep. If the stack is pulled more than four times without any pushes, the address that was stored in the bottom level will be shifted into the PC.

SECTION 3
TIMER

3.1 INTRODUCTION

A block diagram of the EF6804J2 timer circuitry is shown in Figure 3-1. The timer logic in the MCU is comprised of a simple 8-bit counter (timer count register, TCR) with a 7-bit prescaler, and a timer status/control register (TSCR). The timer count register, which may be loaded under program control, is decremented towards zero by a clock input (prescaler output). The prescaler is used to extend the maximum interval of the overall timer. The prescaler tap is selected by bits 0-2 (PS0-PS2) of the timer status/control register. Bits PS0-PS2 control the actual division of the prescaler within the range of divide-by-1 (2^0) to divide-by-128 (2^7). The timer count register (TCR) and prescaler are decremented on rising clock edges. The coding of the TCSR PS0-PS2 bits produce a division in the prescaler as shown in Table 3-1.

Table 3-1. Prescaler Coding Table

PS2	PS1	PS0	Divide By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8

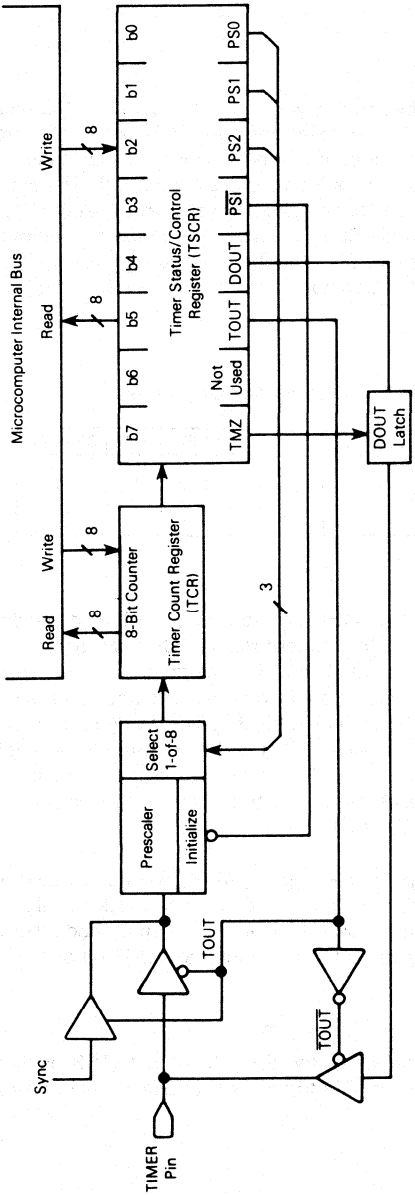
PS2	PS1	PS0	Divide By
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The TIMER pin may be programmed as either an input or an output depending on the status of TOUT (TSCR bit 5). Refer to Figure 3-1. In the input mode, TOUT is a logic zero and the TIMER pin is connected directly to the prescaler input. Therefore, the timer prescaler is clocked by the signal applied from the TIMER pin. The prescaler then divides its clock input by a value determined by the coding of the TSCR bits PS0-PS2 as shown in Table 3-1. The divided prescaler output then clocks the 8-bit timer count register (TCR). When the TCR is decremented to zero, it sets the TMZ bit in the timer status/control register (TSCR). The TMZ bit can be tested under program control to perform a timer function whenever it goes high. The frequency of the external clock applied to the TIMER pin must be less than t_{byte} ($f_{osc}/48$).

In the output mode, TOUT is a logic one and the TIMER pin is connected to the DOUT latch. Therefore, the timer prescaler is clocked by the internal sync pulse (divide-by-48 of the internal oscillator). Operation is similar to that described above for the input mode. However, in the output mode, the low-to-high TMZ bit transition is used to latch the DOUT bit of the TSCR and provide it as output for the TIMER pin.

NOTE

TMZ is normally set to logic one when the timer times out (TCR decrements to $00); however, it may be set by a write of $00 to the TCR or by a write to bit 7 of the TSCR.



TIMER Pin Status

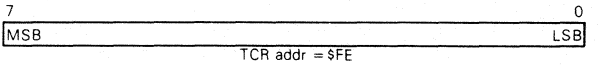
TOUT	Prescaler Clock	TIMER Pin
0	TIMER Pin Sync	Input Mode
1		Output Mode

Figure 3-1. Timer Block Diagram

During reset, the timer count register and prescaler are set to $FF, while the timer status/control register is cleared to $00 and the DOUT LATCH (TIMER pin is in the high-impedance input mode) is forced to a logic high. The prescaler and timer count register are implemented in data space RAM locations ($FD, $FE); therefore, they are both readable and writeable. A write to either will predominate over the TCR decrement-to-$00 function; i.e., if a write and a TCR decrement-to-$00 occur simultaneously, the write will take precedence, and the TMZ bit is not set until the next timer time out.

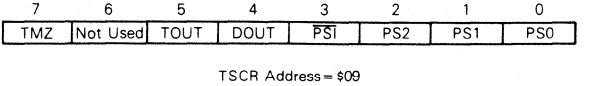
3.2 TIMER REGISTERS

3.2.1 Timer Count Register (TCR)



The timer count register indicates the state of the internal 8-bit counter.

3.2.2 Timer Status/Control Register (TSCR)



b7, TMZ — Low-to-high transition indicates the timer count register has decremented to zero since the timer status/control register was last read. Cleared by a read of TSCR register if TMZ was read as a logic one.

b6 — Not used.

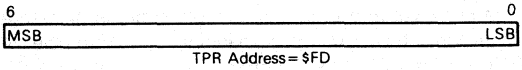
b5, TOUT — When low, this bit selects the input mode for the timer. When high, the output mode is selected.

b4, DOUT — Data sent to the timer output pin when TMZ is set high (output mode only).

b3, $\overline{PSI}$ — Used to initialize the prescaler and inhibit its counting while $\overline{PSI} = 0$. The initialized value is set to $FF. The timer count register will also be inhibited (contents unchanged). When PSI = 1 the prescaler begins to count downward.

b0, b1, b2 PS0-PS1-PS2 — **These bits are used to select the prescaler divide-by ratio; therefore, effecting the clock input frequency to the timer count register.**

3.2.3 Timer Prescaler Register



The timer prescaler register indicates the state of the internal 7-bit prescaler. This 7-bit prescaler divide ratio is normally determined by bits PS0-PS2 of the timer status/control register (see Table 3-1).

SECTION 4
INTERRUPT, SELF-TEST, RESET, AND INTERNAL CLOCK GENERATOR

4.1 INTERRUPT

The EF6804J2 can be interrupted by applying a logic low signal to the $\overline{IRQ}$ pin ; however, a mask option selected at the time of manufacture determines whether the negative-going edge or the actual low level is sensed to indicate an interrupt.

4.1.1 Edge-Sensitive Option

When the $\overline{IRQ}$ pin is pulled low, the internal interrupt request latch is set. Prior to each instruction fetch, the interrupt request latch is tested and, if its output is high, an interrupt sequence is initiated at the end of the current instruction (provided the interrupt mask is cleared). Figure 4-1 contains a flowchart which illustrates both the reset and interrupt sequence. The interrupt sequence consists of one cycle during which: the interrupt request latch is cleared, the interrupt mode flags are selected, the PC is saved on the stack, the interrupt mask is set, and the $\overline{IRQ}$ vector (single chip mode = $FFC/$FFD, self-test mode = $FF8/$FF9) is loaded into the PC. Internal processing of the interrupt continues until an RTI (return from interrupt) instruction is processed. During the RTI instruction, the interrupt mask is cleared and the program mode flags are selected. The next instruction of the program is then fetched and executed. Once the interrupt was initially detected and the interrupt sequence started, the interrupt request latch is cleared so that the next (second) interrupt may be detected even while the previous (first) one is being serviced. However, even though the second interrupt sets the interrupt request latch during processing of the first interrupt, the second interrupt sequence will not be initiated until completion of the interrupt service routine for the first interrupt. Completion of an interrupt service routine is always accomplished using an RTI instruction to return to the main program. The interrupt mask (which is not directly available to the programmer) is cleared during the last cycle of the RTI instruction.

4.1.2 Level-Sensitive Option

The actual operation of the level-sensitive and edge-sensitive options are similar except that the level-sensitive option does not have an interrupt request latch. With no interrupt request latch, the logic level of the $\overline{IRQ}$ pin is checked for detection of the interrupt. Also, in the interrupt sequence, there is no need to clear the interrupt request latch. These differences are illustrated in the flowchart of Figure 4-1.

4.1.3 Power Up and Timing

During the power-up sequence the interrupt mask is set to preclude any false or "ghost" interrupts from occurring. To clear the interrupt mask, the programmer should write a JSR (instead of a JMP) instruction to an initialization routine as the first instruction in a program. The initialization routine

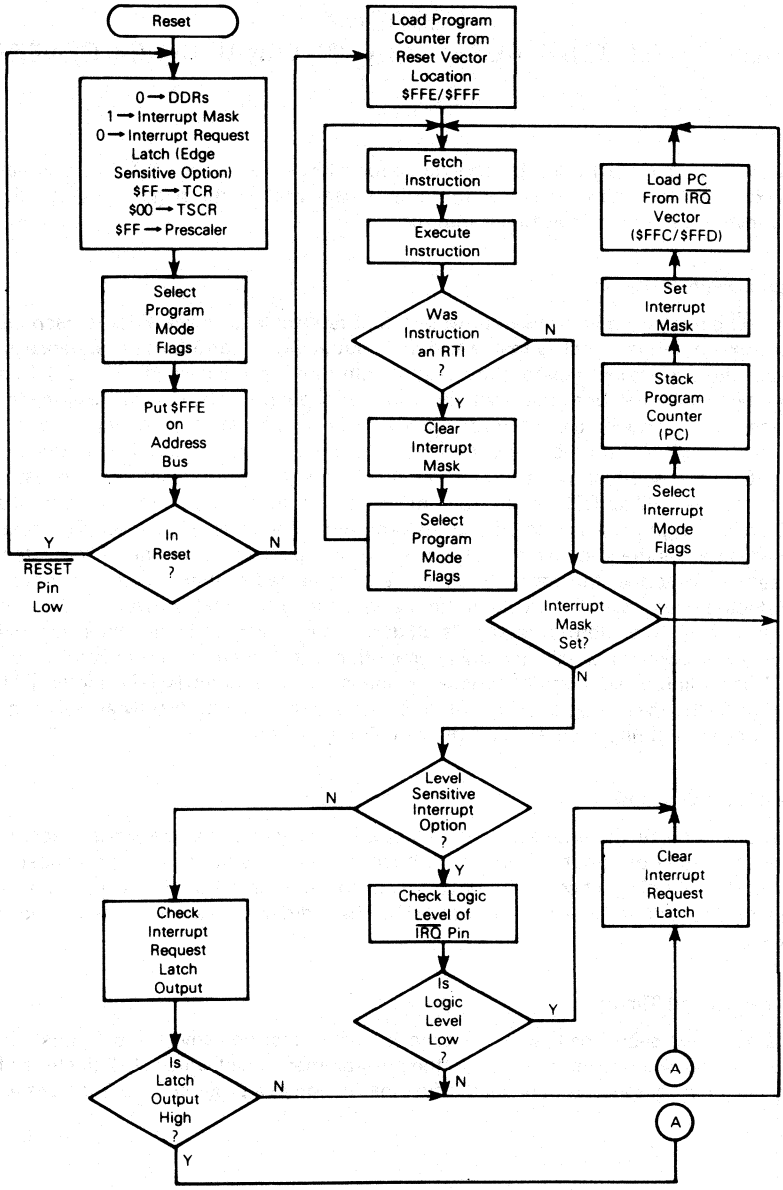


Figure 4-1. Reset and Interrupt Processing Flowchart

should end with an RTI (instead of RTS). Maximum interrupt response time is eight machine (t_{byte}) cycles (see 4.4 INTERNAL CLOCK GENERATOR OPTIONS). This includes five machine cycles for the longest instruction, plus one machine cycle for stacking the PC and switching flags, plus two machine cycles for synchronization of the $\overline{IRQ}$ input with the internal clock. Minimum response time is one machine cycle for stacking PC and switching flags (see 2.4.4 Flags (C, Z)).

4.2 SELF-TEST

The EF6804J2 MCU has a unique internal ROM-based off-line self-test capability using signature analysis techniques. A test program stored in the on-chip ROM is initiated by configuring pins PA6 and PA7 during reset. The test results are sampled on a cycle-by-cycle basis by a 16-bit on-chip signature analysis register configured as a linear feedback shift register (LFSR) using the standard CCITT CRC16 polynomial. A schematic diagram of the self-test connections is shown in Figure 4-2. To perform a test of the MCU, connect it as shown in Figure 4-2a and monitor the LEDs for a 1101 ($D) pattern.

A special ROM self-test utilizing the signature analysis circuitry is also included. To initiate a test of the ROM, connect the circuit as shown in Figure 4-2b. This mode also uses the on-chip signature analysis register to verify the contents of the custom ROM by monitoring an internal bus. The "Good" LED indicates that all ROM words have been read and that the result was the correct signature.

The on-chip self-test and the ROM test are the basis of THOMSON SEMICONDUCTEURS production testing for the EF6804J2. These tests have been fault graded using statistical methods and have been found to provide high fault coverage using automatic test equipment (ATE) or the circuit of Figure 4-2.

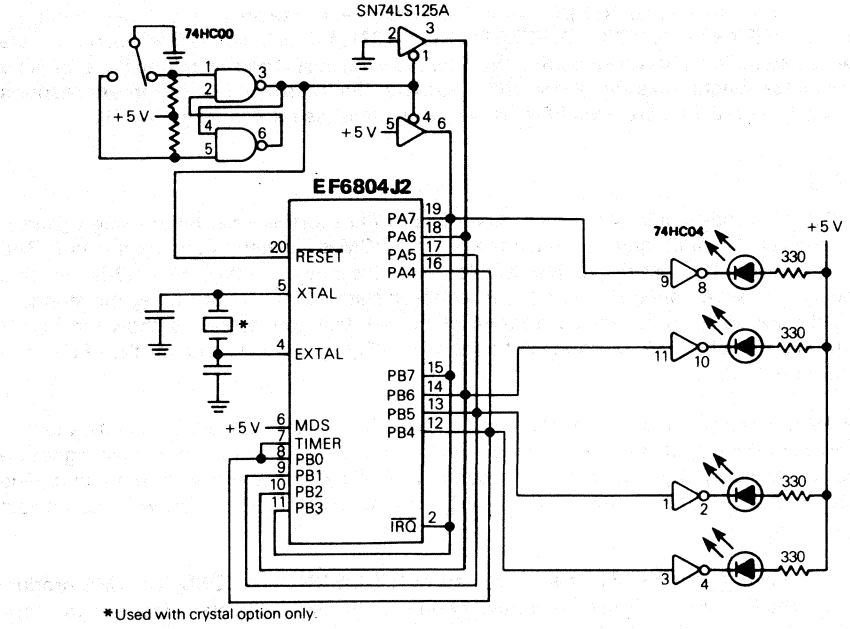
4.3 RESET

The MCU can be reset in two ways: by initial power up (see Figure 4-1) and by the external reset input ($\overline{RESET}$). During power up, a delay of t_{RHL} is needed before allowing the $\overline{RESET}$ input to go high. This time delay allows the internal clock generator to stabilize. Connecting a capacitor and resistor to the $\overline{RESET}$ input, as shown in Figure 4-3, typically provides sufficient delay.

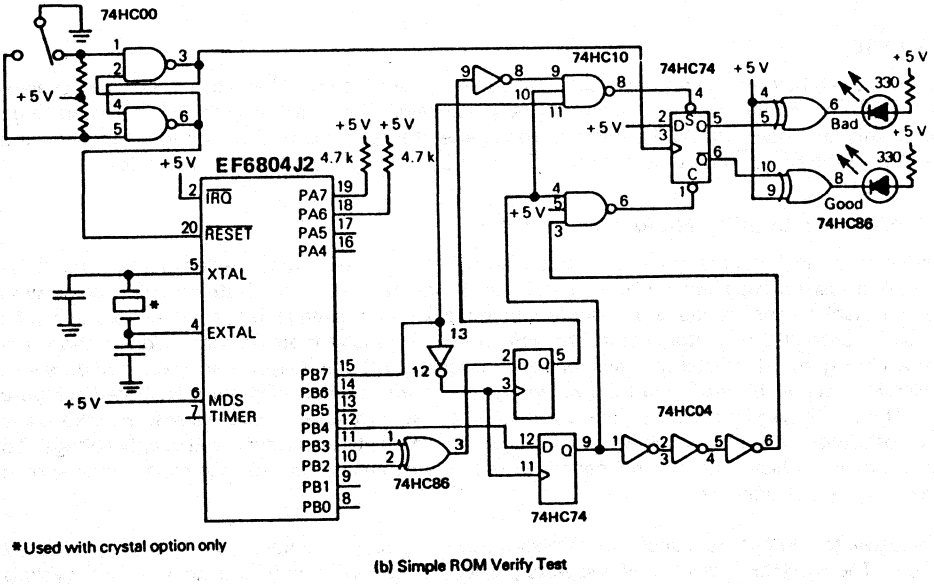
4.4 INTERNAL CLOCK GENERATOR OPTIONS

The internal clock generator circuit is designed to require a minimum of external components. A crystal, a resistor-capacitor, or an external signal may be used to generate a system clock with various stability/cost tradeoffs. A manufacturing mask option is required to select either the crystal oscillator or the RC oscillator circuit. The different clock generator option connection methods are shown in Figure 4-4, crystal specifications and suggested PC board layouts are given in Figure 4-5, resistor-capacitor selection graph is given in Figure 4-6, and a timing diagram is illustrated in Figure 4-7. The crystal oscillator startup time is a function of many variables: crystal parameters (especially R_S), oscillator load capacitance (C_L), IC parameters, ambient temperature, and supply voltage. To ensure rapid oscillator startup, neither the crystal characteristics nor the load capacitance should exceed recommendations.

The oscillator output frequency is internally divided by four to produce the internal $\phi 1$ and $\phi 2$ clocks. The $\phi 1$ clock is divided by twelve to produce a machine byte (cycle) clock. A byte cycle is the smallest unit needed to execute any operation (i.e., increment the program counter). An instruction may need two, four, or five byte cycles to execute.



(a) Functional Test



(b) Simple ROM Verify Test

Figure 4-2. Self-Test Circuit

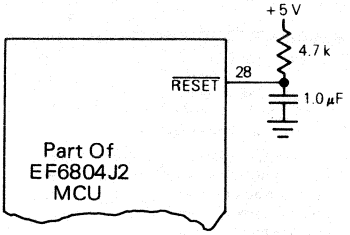
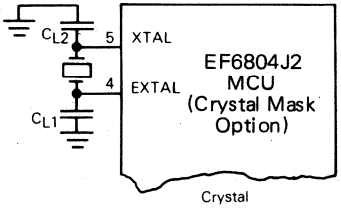


Figure 4-3. Power-Up Reset Delay Circuit



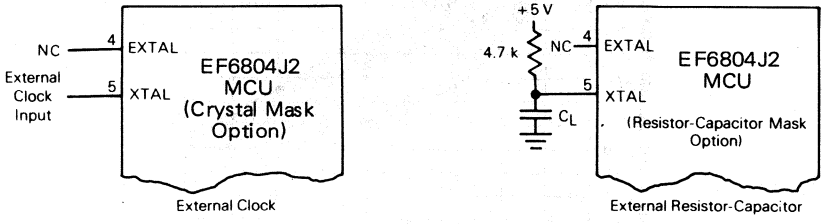


Figure 4-4. Clock Generator Options

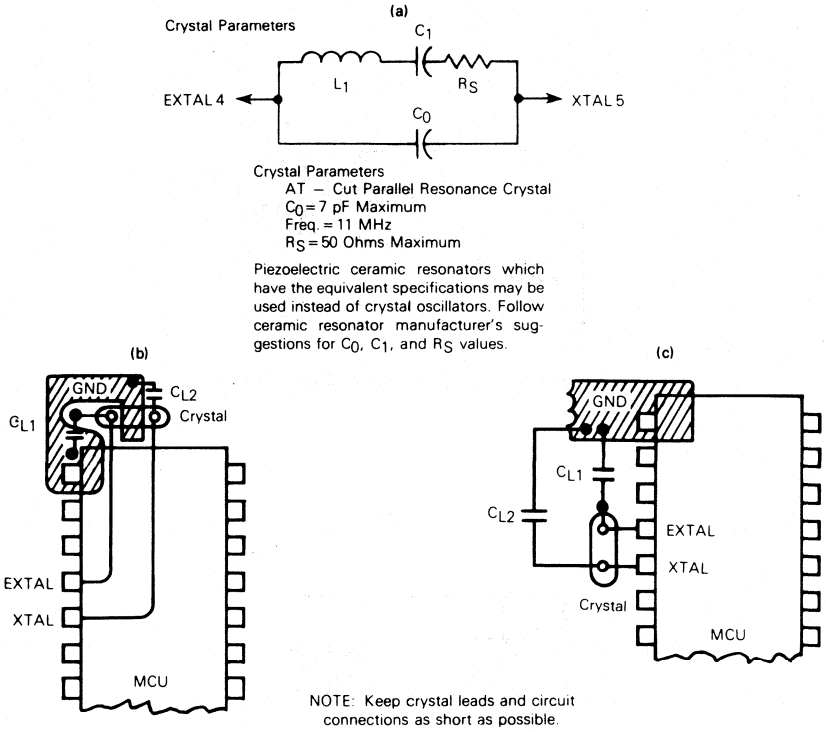


Figure 4-5. Crystal Motional Arm Parameters and Suggested PC Board Layout

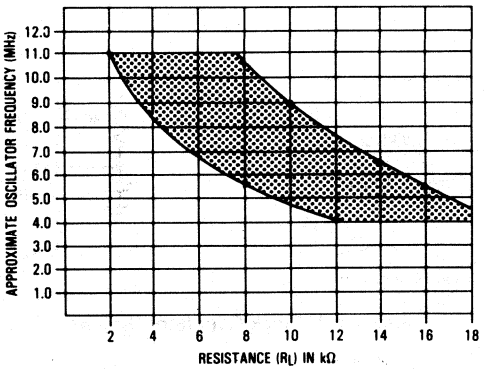


Figure 4-6. Typical Frequency Selection For Resistor-Capacitor Oscillator Option (C_L = 17 pF)

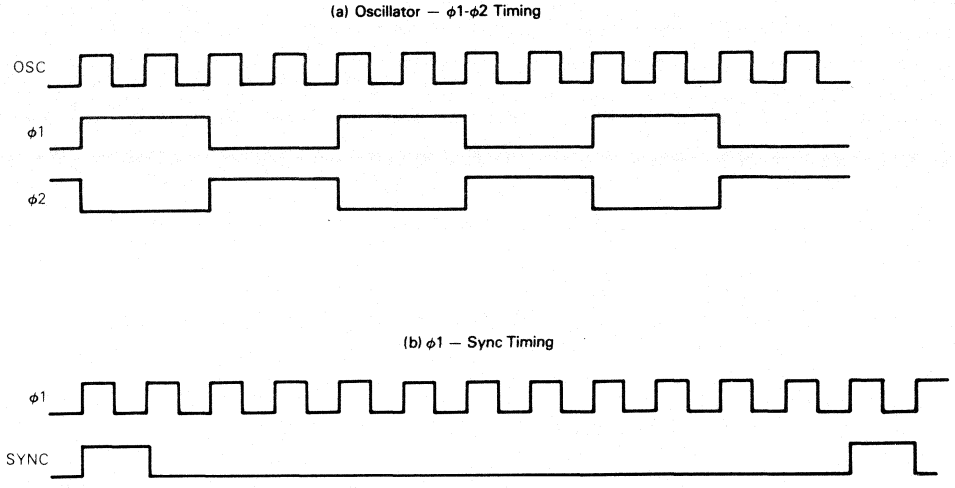
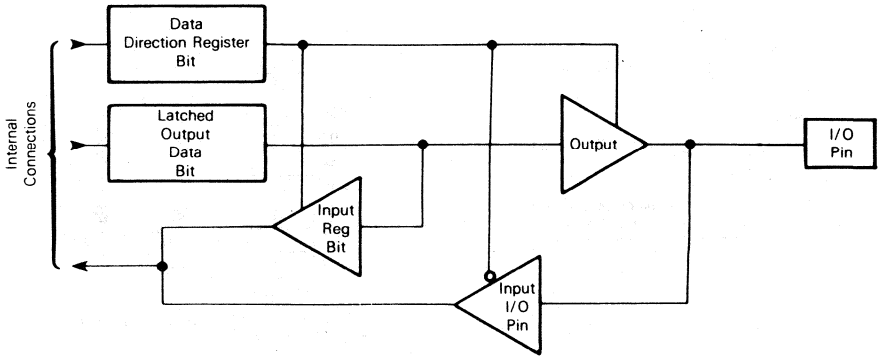


Figure 4-7. Clock Generator Timing Diagram

SECTION 5
INPUT/OUTPUT PORTS

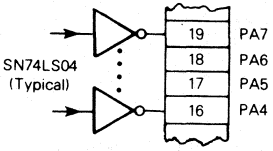
5.1 INPUT/OUTPUT

There are 12 input/output pins. All pins (port A and B) are programmable as either inputs or outputs under software control of the corresponding data direction register (DDR). The port I/O programming is accomplished by writing the corresponding bit in the port DDR to a logic one for output or a logic zero for input. On reset, all the DDRs are initialized to a logic zero state to put the ports in the input mode. The port output registers are not initialized on reset but should be initialized before changing the DDR bits to avoid undefined levels. When programmed as outputs, the latched output data is readable as input data, regardless of the logic levels at the output pin due to output loading; see Figure 5-1. All input/output pins are LSTTL compatible as both inputs and outputs. In addition, both ports may have one of two mask options: 1) internal pullup resistor for CMOS output compatibility, or 2) open drain output. The address map in Figure 2-1 gives the address of data registers and DDRs. The register configuration is discussed under the registers paragraph below and Figure 5-2 provides some examples of port connections.

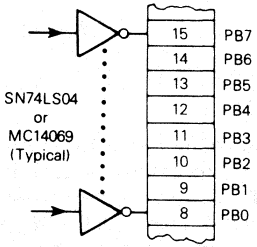


Data Direction Register Bit	Output Data Bit	Output State	Input To MCU
1	0	0	0
1	1	1	1
0	X	Hi-Z	Pin

Figure 5-1. Typical I/O Port Circuitry

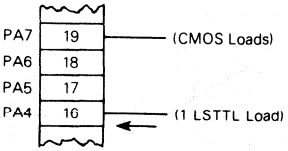


LSTTL Driving Port A Directly

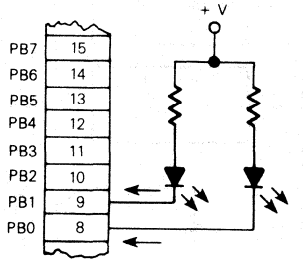


CMOS or LSTTL Driving Port B Directly

(a) Input Mode



Port A, bit 7 programmed as output, driving CMOS loads and bit 4 driving one LSTTL load directly (using CMOS output option).



Port B, bit 0, and bit 1 programmed as output, driving LEDs directly.

(b) Output Mode

Figure 5-2. Typical Port Connections

The latched output data bit (see Figure 5-1) may always be written. Therefore, any write to a port writes to all of its data bits even though the port DDR is set to input. This may be used to initialize the data registers and avoid undefined outputs; however, care must be exercised when using read-modify-write instructions since the data read corresponds to the pin level if the DDR is an input (0) and corresponds to the latched output data when the DDR is an output (1). The 12 bidirectional lines may be configured by port to be LSTTL (standard configuration), LSTTL/CMOS (mask option), or open drain (mask option). Port B outputs are LED compatible.

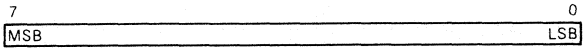
NOTE

The mask option only allows changes by port. For example, if the customer wishes PA7 to be open drain, then PA4-PA7 must all be open drain.

5.2 REGISTERS

The registers described below are implemented as RAM locations and thus may be read or written.

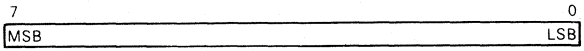
5.2.1 Port Data Register



Port A Address = $00
Port B Address = $01

The source of data read from the port data register will be the port I/O pin or previously latched output data depending upon the contents of the corresponding data direction register (DDR). The destination of data written to the port data register will be an output data latch. If the corresponding data direction register (DDR) for the port I/O pin is programmed as an output, the data will then appear on the port pin.

5.2.2 Port Data Direction Register



Port A Address = $04
Port B Address = $05

The port DDRs configure the port pins as either inputs or outputs. Each port pin can be programmed individually to act as an input or an output. A zero in the pins corresponding bit position will program that pin as an input while a one in the pins corresponding bit position will program that pin as an output.

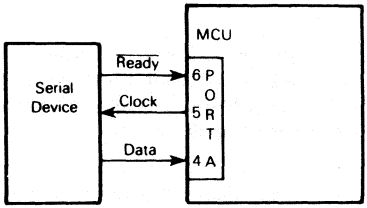
SECTION 6
SOFTWARE AND INSTRUCTION SET

6.1 SOFTWARE

6.1.1 Bit Manipulation

The EF6804J2 MCU has the ability to set or clear any register or single random access memory (RAM) writable bit with a single instruction (BSET, BCLR). Any bit in data space, including ROM, can be tested, using the BRSET and BRCLR instructions, and the program may branch as a result of its state. The carry bit is set to the value of the bit referenced by BRSET or BRCLR. A rotate instruction may then be used to accumulate serial input data in a RAM location or register. The capability to work with any bit in RAM, ROM, or I/O allows the user to have individual flags in RAM or to handle I/O bits as control lines.

The coding example in Figure 6-1 illustrates the usefulness of the bit manipulation and test instructions. Assume that the MCU is to communicate with an external serial device. The external device has a data ready signal, a data output line, and a clock line (to clock data one bit at a time, MSB first, out of the device). The MCU waits until the data is ready, clocks the external device, picks up the data in the carry flag (C bit), clears the clock line, and finally accumulates the data bit in the accumulator.




```
                .
                .
                .
SELF    BRSET   6,PORTA,SELF
                .
                .
                .
        BSET    5,PORTA
        BRCLR   4,PORTA,CONT
CONT    BCLR    5,PORTA
        ROLA    .
                .
                .
                .
```

Figure 6-1. Bit Manipulation Example

6.1.2 Addressing Modes

The EF6804J2 MCU has nine addressing modes which are explained briefly in the following paragraphs. The EF6804J2 deals with objects in three different address spaces : program space, data space, and stack space. Program space contains the instructions which are to be executed, plus the data for immediate mode instructions. Data space contains all of the RAM locations, X and Y registers, accumulator, timer, I/O locations, and some ROM (for storage of tables and constants). Stack space contains RAM for use in stacking the return addresses for subroutines and interrupts.

The term "Effective Address" (EA) is used in describing the address modes. EA is defined as the address from which the argument for an instruction is fetched or stored.

6.1.2.1 IMMEDIATE. In the immediate addressing mode, the operand is located in program ROM and is contained in a byte following the opcode. The immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

6.1.2.2 DIRECT. In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the 256 bytes in data space memory with a single two-byte instruction.

6.1.2.3 SHORT DIRECT. The MCU also has four locations in data space RAM ($80, $81, $82, $83) which may be used in a short-direct addressing mode. In this mode the lower two bits of the opcode determine the data space. RAM location, and the instruction is only one byte. Short direct addressing is a subset of the direct addressing mode. (The X and Y registers are at locations $80 or $81 respectively.)

6.1.2.4 EXTENDED. In the extended addressing mode, the effective address is obtained by concatenating the four least significant bits of the opcode with the byte following the opcode (12-bit address). Instructions using the extended addressing mode (JMP, JSR) are capable of branching anywhere in program space. An extended addressing mode instruction is two bytes long.

6.1.2.5 RELATIVE. The relative addressing mode is only used in conditional branch instructions. In relative addressing, the address is formed by adding the sign extended lower five bits of the opcode (the offset) to the program counter if and only if the condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from − 15 to + 16 from the opcode address. The programmer need not worry about calculating the correct offset when using the Motorola assembler since it calculates the proper offset and checks to see if it is within the span of the branch.

6.1.2.6 BIT SET/CLEAR. In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode specifies the direct address of the byte in which the specified bit is to be set or cleared. Thus, any bit in the 256 locations of data space memory, which can be written to, can be set or cleared.

6.1.2.7 BIT TEST AND BRANCH. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit which is to be tested is included in the opcode, and the data space address of the byte to be tested is in the single byte immediately following the opcode byte. The third byte is sign extended to twelve bits and becomes the offset added to the program counter if the condition is true. The single three-byte instruction allows the program to branch based on the condition of any bit in data space memory. The span of branching is from −125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry flag.

6.1.2.8 REGISTER-INDIRECT. In the register-indirect addressing mode, the operand is at the address (in data space) pointed to by the contents of one of the indirect registers (X or Y). The particular X or Y register is selected by bit 4 of the opcode. Bit 4 of the opcode is then decoded into an address which selects the desired X or Y register ($80 or $81). A register-indirect instruction is one byte long.

6.1.2.9 INHERENT. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

6.2 INSTRUCTION SET

The EF6804J2 MCU has a set of 42 basic instructions, which when combined with nine addressing modes produce 242 usable opcodes. They can be divided into five different types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

6.2.1 Register/Memory Instructions

Most of these instructions use two operands. One operand is the accumulator and the other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operands. Refer to Table 6-1.

6.2.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. There are ten instructions which utilize read-modify-write cycles. All INC and DEC forms along with all bit manipulation instructions use this method. Refer to Table 6-2.

6.2.3 Branch Instructions

The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 6-3.

6.2.4 Bit Manipulation Instructions

These instructions are used on any bit in data space memory. One group either sets or clears. The other group performs the bit test branch operations. Refer to Table 6-4.

Table 6-1. Register/Memory Instructions

		Addressing Modes																			
		Indirect				Immediate			Direct			Inherent			Extended			Short-Direct			
Function	Mnem	Opcode X	Opcode Y	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Special Notes
Load A from Memory	LDA	E0	F0	1	4	E8	2	4	F8	2	4	–	–	–	–	–	–	AC-AF	1	4	1
Load XP from Memory	LDXI	–	–	–	–	B0	3	4	–	–	–	–	–	–	–	–	–	–	–	–	4
Load YP from Memory	LDYI	–	–	–	–	B0	3	4	–	–	–	–	–	–	–	–	–	–	–	–	4
Store A in Memory	STA	E1	F1	1	4	–	–	–	F9	2	4	–	–	–	–	–	–	BC-BF	1	4	2
Add to A	ADD	E2	F2	1	4	EA	2	4	FA	2	4	–	–	–	–	–	–	–	–	–	–
Subtract from A	SUB	E3	F3	1	4	EB	2	4	FB	2	4	–	–	–	–	–	–	–	–	–	–
Arithmetic Compare with Memory	CMP	E4	F4	1	4	EC	2	4	FC	2	4	–	–	–	–	–	–	–	–	–	–
AND Memory to A	AND	E5	F5	1	4	ED	2	4	FD	2	4	–	–	–	–	–	–	–	–	–	–
Jump to Subroutine	JSR	–	–	–	–	–	–	–	–	–	–	–	–	–	8 (TAR)	2	4	–	–	–	3
Jump Unconditional	JMP	–	–	–	–	–	–	–	–	–	–	–	–	–	9 (TAR)	2	4	–	–	–	3
Clear A	CLRA	–	–	–	–	–	–	–	FB	2	4	–	–	–	–	–	–	–	–	–	–
Clear XP	CLRX	–	–	–	–	–	–	–	FB	2	4	–	–	–	–	–	–	–	–	–	–
Clear YP	CLRY	–	–	–	–	–	–	–	FB	2	4	–			–	–	–	–	–	–	–
Complement A	COMA	–	–	–	–	–	–	–	–	–	–	B4	1	4	–	–	–	–	–	–	–
Move Immediate Value to Memory	MVI	–	–	–	–	B0	3	4	B0	3	4	–	–	–	–	–	–	–	–	–	5
Rotate A Left and Carry	ROLA	–	–	–	–	–	–	–	–	–	–	B5	1	4	–	–	–	–	–	–	–
Arithmetic Left Shift of A	ASLA	–	–	–	–	–	–	–	FA	2	4	–	–	–	–	–	–	–	–	–	–

SPECIAL NOTES

1. In Short-Direct addressing, the LDA mnemonic represents opcode AC, AD, AE, and AF. This is equivalent to RAM locations $80 (AC), $81 (AD), $82 (AE), and $83 (AF)
2. In Short-Direct addressing, the STA mnemonic represents opcode BC, BD, BE, and BF. This is equivalent to RAM locations $80 (BC), $81 (BD), $82 (BE), and $83 (BF).
3. In Extended addressing, the four LSBs of the opcode (Mnemonic JSR and JMP) are formed by the four MSBs of the target address. (TAR)
4. In Immediate addressing, the LDXI and LDYI are mnemonics which are recognized as follows:
   LDXI = MVI $80,data
   LDYI = MVI $81,data Where data is a one-byte hexadecimal number.
5. The MVI instruction refers to both Immediate and Direct addressing.

Table 6-2. Read-Modify-Write Instructions

Function	Mnem	Addressing Modes										Special Notes
		Indirect				Direct			Short-Direct			
		Opcode		# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	
		X	Y									
Increment Memory Location	INC	E6	F6	1	4	FE	2	4	A8-AB	1	4	1, 3
Increment A	INCA	–	–	–	–	FE	2	4	–	–	–	–
Increment XP	INCX	–	–	–	–	–	–	–	A8	1	4	–
Increment YP	INCY	–	–	–	–	–	–	–	A9	1	4	–
Decrement Memory Location	DEC	E7	F7	1	4	FF	2	4	B8-BB	1	4	2, 4
Decrement A	DECA	–	–	–	–	FF	2	4	–	–	–	–
Decrement XP	DECX	–	–	–	–	–	–	–	B8	1	4	–
Decrement YP	DECY	–	–	–	–	–	–	–	B9	1	4	–

SPECIAL NOTES

1. In Short-Direct addressing, the INC mnemonic represents opcode A8, A9, AA, and AB. These are equivalent to RAM locations $80 (A8), $81 (A9), $82 (AA), and $83 (AB).
2. In Short-Direct addressing, the DEC mnemonic represents opcode B8, B9, BA, and BB. These are equivalent to RAM locations $80 (B8), $81 (B9), $82 (BA), and $83 (BB).
3. In Indirect addressing, the INC mnemonic represents opcode E6 or F6, and causes the location pointed to by X (E6 opcode) or Y (F6 opcode) to be incremented.
4. In Indirect addressing, the INC mnemonic represents opcode E7 or F7, and causes the location pointed to by X (E7 opcode) or Y (F7 opcode) to be incremented.

Table 6-3. Branch Instructions

Function	Mnem	Relative Addressing Mode			
		Opcode	# Bytes	# Cycles	Special Notes
Branch if Carry Clear	BCC	40-5F	1	2	1
Branch if Higher or Same	(BHS)	40-5F	1	2	1, 2
Branch if Carry Set	BCS	60-7F	1	2	1
Branch if Lower	(BLO)	60-7F	1	2	1, 3
Branch if Not Equal	BNE	00-1F	1	2	1
Branch if Equal	BEQ	20-3F	1	2	1

SPECIAL NOTES

1. Each mnemonic of the Branch Instructions covers a range of 32 opcodes; e.g., BCC ranges from 40 through 5F. The actual memory location (target address) to which the branch is made is formed by adding the sign extended lower five bits of the opcode to the contents of the program counter.
2. The BHS instruction (shown in parentheses) is identical to the BCC instruction. The C bit is clear if the register was higher or the same as the location in the memory to which it was compared.
3. The BLO instruction (shown in parentheses) is identical to the BCS instruction. The C bit is set if the register was lower than the location in memory to which it was compared.

Table 6-4. Bit Manipulation Instructions

Function	Mnem	Addressing Modes						
		Bit Set/Clear			Bit Test and Branch			Special Note
		Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	
Branch IFF Bit n is set	BRSET n (n=0 . . . 7)	–	–	–	C8+n	3	5	1
Branch IFF Bit n is clear	BRCLR n (n=0 . . . 7)	–	–	–	C0+n	3	5	1
Set Bit n	BSET n (n=0 . . . 7)	D8+n	2	4	–	–	–	1
Clear Bit n	BCLR n (n=0 . . . 7)	D0+n	2	4	–	–	–	1

SPECIAL NOTE

1. The opcode is formed by adding the bit number (0-7) to the basic opcode. For example: to clear bit six using the BSET6 instruction the opcode becomes DE (D8+6); BCLR5 becomes (C0+5); etc.

6.2.5 Control Instructions

The control instructions control the MCU operations during program execution. Refer to Table 6-5.

6.2.6 Alphabetical Listing

The complete instruction set is given in alphabetical order in Table 6-6. There are certain mnemonics recognized by the assembler and converted to other instructions. The fact that all registers and accumulator are in RAM allows many implied instructions to exist. The implied instructions recognized by the assembler are identified in Table 6-6.

6.2.7 Opcode Map Summary

Table 6-7 contains an opcode map for the instructions used on the MCU.

6.3 IMPLIED INSTRUCTIONS

Since the accumulator and all other registers are located in RAM many implied instructions exist. The assembler-recognized implied instructions are given in Table 6-6. Some examples not recognized by the assembler are shown below.

BCLR,7 $FF	Ensures accumulator is plus
BSET,7 $FF	Ensures accumulator is minus
BRCLR,7 $FF	Branch iff accumulator is plus
BRSET,7 $FF	Branch iff accumulator is minus
BRCLR,7 $80	Branch iff X is plus (BXPL)
BRSET,7 $80	Branch iff X is minus (BXMI)
BRCLR,7 $81	Branch iff Y is plus (BYPL)
BRSET,7 $81	Branch iff Y is minus (BYMI)

Table 6-5. Control Instructions

		Addressing Modes									
		Short-Direct			Inherent			Relative			
Function	Mnem	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Special Notes
Transfer A to X	TAX	BC	1	4	–	–	–	–	–	–	–
Transfer A to Y	TAY	BD	1	4	–	–	–	–	–	–	–
Transfer X to A	TXA	AC	1	4	–	–	–	–	–	–	–
Transfer Y to A	TYA	AD	1	4	–	–	–	–	–	–	–
Return from Subroutine	RTS	–	–	–	B3	1	2	–	–	–	–
Return from Interrupt	RTI	–	–	–	B2	1	2	–	–	–	–
No-Operation	NOP	–	–	–	–	–	–	–	–	–	1

SPECIAL NOTE

1 . The NOP instruction is equivalent to a branch if equal (BEQ) to the location designated by PC + 1.

Table 6-6. Instruction Set

Mnemonic	Addressing Modes									Flags	
	Inherent	Immediate	Direct	Short Direct	Bit/Set Clear	Bit-Test-Branch	Register Indirect	Extended	Relative	Z	C
ADD		X	X				X			Λ	Λ
AND		X	X				X			Λ	•
ASLA	Assembler converts this to "ADD $FF"									•	•
BCC									X	Λ	Λ
BCLR					X					•	•
BCS									X	•	•
BEQ									X	•	•
BHS	Assembler converts this to "BCC"									•	•
BLO	Assembler converts this to "BCS"									•	•
BNE									X	•	•
BRCLR						X				•	Λ
BRSET						X				•	Λ
BSET					X					•	•
CLRA	Assembler converts this to "SUB $FF"									Λ	Λ
CLRX	Assembler converts this to "MVI = 0, $80"									•	•
CLRY	Assembler converts this to "MVI = 0, $81"									•	•
CMP		X	X				X			Λ	Λ
COMA	X									Λ	Λ
DEC			X	X			X			Λ	•
DECA	Assembler converts this to "DEC $FF"									Λ	•
DECX	Assembler converts this to "DEC $80"									Λ	•
DECY	Assembler converts this to "DEC $81"									Λ	•
INC			X	X			X			Λ	•
INCA	Assembler converts this to "INC $FF"									Λ	•
INCX	Assembler converts this to "INC $80"									Λ	•
INCY	Assembler converts this to "INC $81"									Λ	•
JMP								X		•	•
JSR								X		•	•
LDA		X	X	X			X			Λ	•
LDXI	Assembler converts this to "MVI DATA, $80"									•	•
LDYI	Assembler converts this to "MVI DATA, $81"									•	•
MVI		X	X							•	•
NOP	Assembler converts this to "BEQ (PC) + 1"									•	•
ROLA	X									Λ	Λ
RTI	X									Λ	Λ
RTS	X									•	•
STA			X	X			X			Λ	•
SUB		X	X				X			Λ	Λ
TAX	Assembler converts this to "STA $80"									Λ	•
TAY	Assembler converts this to "STA $81"									Λ	•
TXA	Assembler converts this to "LDA $80"									Λ	•
TYA	Assembler converts this to "LDA $81"									Λ	•

Flag Symbols: Z = Zero, C = Carry/Borrow, Λ = Test and Set if True, Cleared Otherwise, • = Not Affected

Table 6-7 – EF6804P2 Microcomputer Instruction Set Opcode Map

	Branch Instructions							
Hi / Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111
0 0000	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
1 0001	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
2 0010	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
3 0011	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
4 0100	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
5 0101	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
6 0110	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
7 0111	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
8 1000	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
9 1001	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
A 1010	2 BNE 1 REL	2 BNE 2 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
B 1011	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
C 1100	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
D 1101	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
E 1110	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
F 1111	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL

Abbreviations for Address Modes

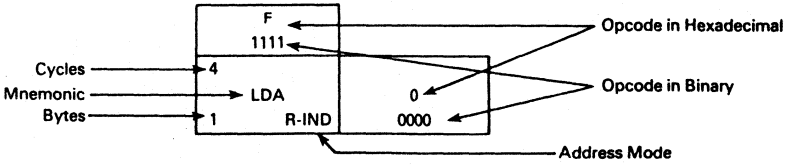
INH	Inherent
S-D	Short Direct
B-T-B	Bit Test and Branch
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
R-IND	Register Indirect

*	Indicates Instruction Reserved for Future Use
#	Indicates Illegal Instruction

Instruction Set Opcode Map

Register/Memory, Control, and Read/Modify/Write Instructions				Bit Manipulation Instructions		Register/Memory and Read/Modify/Write		
8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Hi / Low
4 JSRn 2 EXT	4 JMPn 2 EXT	*	4 MVI 3 IMM	5 BRCLR0 3 B-T-B	4 BCLR0 2 BSC	4 LDA 1 R-IND	4 LDA 1 R-IND	0 0000
4 JSRn 2 EXT	4 JMPn 2 EXT	*	*	5 BRCLR1 3 B-T-B	4 BCLR1 2 BSC	4 STA 1 R-IND	4 STA 1 R-IND	1 0001
4 JSRn 2 EXT	4 JMPn 2 EXT	*	2 RTI 1 INH	5 BRCLR2 3 BT-B	4 BCLR2 2 BSC	4 ADD 1 R-IND	4 ADD 1 R-IND	2 0010
4 JSRn 2 EXT	4 JMPn 2 EXT	*	2 RTS 1 INH	5 BRCLR3 3 B-T-B	4 BCLR3 2 BSC	4 SUB 1 R-IND	4 SUB 1 R-IND	3 0011
4 JSRn 2 EXT	4 JMPn 2 EXT	*	4 COMA 1 INH	5 BRCLR4 3 B-T-B	4 BCLR4 2 BSC	4 CMP 1 R-IND	4 CMP 1 R-IND	4 0100
4 JSRn 2 EXT	4 JMPn 2 EXT	*	4 ROLA 1 INH	5 BRCLR5 3 B-T-B	4 BCLR5 2 BSC	4 AND 1 R-IND	4 AND 1 R-IND	5 0101
4 JSRn 2 EXT	4 JMPn 2 EXT	*	*	5 BRCLR6 3 B-T-B	4 BCLR6 2 BSC	4 INC 1 R-IND	4 INC 1 R-IND	6 0110
4 JSRn 2 EXT	4 JMPn 2 EXT	*	*	5 BRCLR7 3 B-T-B	4 BCLR7 2 BSC	4 DEC 1 R-IND	4 DEC 1 R-IND	7 0111
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 S-D	4 DEC 1 S-D	5 BRSET0 3 B-T-B	4 BSET0 2 BSC	4 LDA 2 IMM	4 LDA 2 DIR	8 1000
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 S-D	4 DEC 1 S-D	5 BRSET1 3 B-T-B	4 BSET1 2 BSC	#	4 STA 2 DIR	9 1001
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 S-D	4 DEC 1 S-D	5 BRSET2 3 B-T-B	4 BSET2 2 BSC	4 ADD 2 IMM	4 ADD 2 DIR	A 1010
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 S-D	4 DEC 1 S-D	5 BRSET3 3 B-T-B	4 BSET3 2 BSC	4 SUB 2 IMM	4 SUB 2 DIR	B 1011
4 JSRn 2 EXT	4 JMPn 2 EXT	4 LDA 1 S-D	4 STA 1 S-D	5 BRSET4 3 B-T-B	4 BSET4 2 BSC	4 CMP 2 IMM	4 CMP 2 DIR	C 1100
4 JSRn 2 EXT	4 JMPn 2 EXT	4 LDA 1 S-D	4 STA 1 S-D	5 BRSET5 3 B-T-B	4 BSET5 2 BSC	4 AND 2 IMM	4 AND 2 DIR	D 1101
4 JRSn 2 EXT	4 JMPn 2 EXT	4 LDA 1 S-D	4 STA 1 S-D	5 BRSET6 3 B-T-B	4 BSET6 2 BSC	#	4 INC 2 DIR	E 1110
4 JSRn 2 EXT	4 JMPn 2 EXT	4 LDA 1 S-D	4 STA 1 S-D	5 BRSET7 3 B-T-B	4 BSET7 2 BSC	#	4 DEC 2 DIR	F 1111

LEGEND



SECTION 7
ELECTRICAL SPECIFICATIONS

7.1 INTRODUCTION

This section contains the electrical specifications and associated timing for the EF6804J2.

7.2 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to / 7.0	V
Operating Temperature Range Standard or L suffix V suffix T suffix	T_A	TL to TH 0 to 70 -40 to 85 -40 to 105	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C
Junction Temperature Range Plastic	T_J	150	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$. Reliability of operation is enhanced if unused inputs except EXTAL are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

7.3 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic	θ_{JA}	90	°C/W

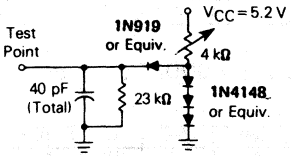


Figure 7-1. LSTTL Equivalent Test Load (Port B)

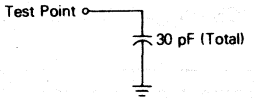


Figure 7-2. CMOS Equivalent Test Load (Ports A and B)

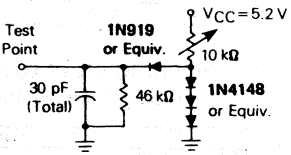


Figure 7-3. LSTTL Equivalent Test Load (Port A and TIMER)

7.4 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts – Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts – User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

7.5 ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc ± 0.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Power Dissipation – No Port Loading T_A = 0°C	P_{INT}	–	135	170	mV
T_A = -40°C		–	–	210	
Input High Voltage	V_{IH}	4.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Input Capacitance	C_{in}	–	10	–	pF
Input Current ($\overline{IRQ}$, $\overline{RESET}$)	I_{in}	–	2	20	µA

7.6 SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc ± 0.5 Vdc, V_{SS} = GND, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency	f_{OSC}	4.0	–	11.0	MHz
Bit Time	t_{bit}	0.364	–	1.0	µs
Byte Cycle Time	t_{byte}	4.36	–	12.0	µs
$\overline{IRQ}$ and TIMER Pulse Width	t_{WL}, t_{WH}	$2xt_{byte}$	–	–	–
$\overline{RESET}$ Pulse Width	t_{RWL}	$2xt_{byte}$	–	–	–
$\overline{RESET}$ Delay Time (External Capacitance = 1.0 µF)	t_{RHL}	100	–	–	ms

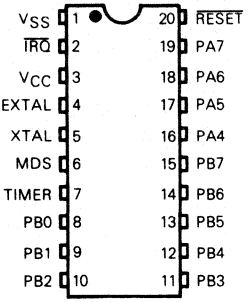
7.7 PORT DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc ± 0.5 Vdc, V_{SS} = GND $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Timer and Ports A (Standard)					
Output Low Voltage, I_{Load} = 0.4 mA	V_{OL}	–	–	0.5	V
Output High Voltage, I_{Load} = – 50 µA	V_{OH}	2.3	–	–	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	4	40	µA
Timer and Ports A (Open Drain)					
Output Low Voltage, I_{Load} = 0.4 mA	V_{OL}	–	–	0.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	4	40	µA
Open Drain Leakage (V_{out} = V_{CC})	I_{LOD}	–	4	40	µA
Timer and Ports A (CMOS Drive)					
Output Low Voltage, I_{Load} = 0.4 mA (Sink)	V_{OL}	–	–	0.5	V
Output High Voltage, I_{Load} = – 10 µA	V_{OH}	V_{CC} – 1.0	–	–	V
Output High Voltage, I_{Load} = – 50 µA	V_{OH}	2.3	–	–	V
Input High Voltage, I_{Load} = – 300 µA Max	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage, I_{Load} = – 300 µA Max	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current (V_{in} = 0.4 V to V_{CC})	I_{TSI}	–	–	– 300	µA
Port B (Standard)					
Output Low Voltage, I_{Load} = 1.0 mA	V_{OL}	–	–	0.5	V
Output Low Voltage, I_{Load} = 10 mA (Sink)	V_{OL}	–	–	1.5	V
Output High Voltage, I_{Load} = – 100 µA	V_{OH}	2.3	–	–	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	8	80	µA
Port B (Open Drain)					
Output Low Voltage, I_{Load} = 1.0 mA	V_{OL}	–	–	0.5	V
Output Low Voltage, I_{Load} = 10 mA (Sink)	V_{OL}	–	–	1.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	8	80	µA
Open Drain Leakage (V_{out} = V_{CC})	I_{LOD}	–	8	80	µA
Port B (CMOS Drive)					
Output Low Voltage, I_{Load} = 1.0 mA	V_{OL}	–	–	0.5	V
Output High Voltage, I_{Load} = 10 mA (Sink)	V_{OL}	–	–	1.5	V
Output High Voltage, I_{Load} = – 10 µA	V_{OH}	V_{CC} – 1.0	–	–	V
Output High Voltage, I_{Load} = – 100 µA	V_{OH}	2.3	–	–	V
Input High Voltage, I_{Load} = – 300 µA Max	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage, I_{Load} = – 300 µA Max	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current (V_{in} = 0.4 V to V_{CC})	I_{TSI}	–	–	– 300	µA

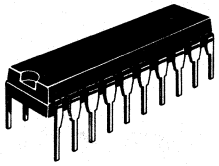
SECTION 8
MECHANICAL DATA

This section contains the pin assignment and package dimension diagrams for the EF6804J2 microcomputer.

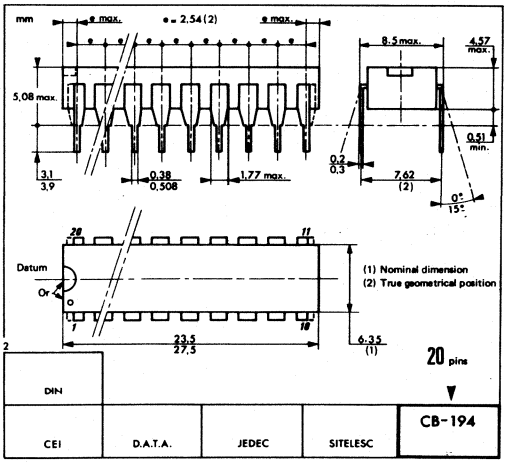
8.1 PIN ASSIGNMENT



CASE CB-194



P SUFFIX
PLASTIC PACKAGE



SECTION 9
ORDERING INFORMATION

9.1 INTRODUCTION

The following information is required when ordering a custom MCU. The information may be transmitted to THOMSON SEMICONDUCTEURS in the following media:

EPROM(s), 2716 or 2732
EFDOS/MDOS*, disk file

To initiate a ROM pattern for the MCU, it is necessary to first contact your local field service office, local sales person, or your local THOMSON SEMICONDUCTEURS representative.

9.1.1 EPROMs

One 2716 or one 2732 type EPROM, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. Since all program and data space information will fit on one 2716 or 2732 EPROM, the EPROM must be programmed as follows in order to emulate the EF6804J2 MCU. **For a 2716, start the data space ROM at EPROM address $020 and start program space ROM at EPROM address $410 and continue to memory space $7FF. Memory spaces $7F8 through $7FB are reserved for THOMSON SEMICONDUCTEURS self-test vectors. For a 2732, the memory map shown in Figure 2-1 can be used. All unused bytes, including the user's space, must be set to zero.** For shipment to THOMSON SEMICONDUCTEURS the EPROMs should be placed in a conductive IC carrier and packed securely. Do not use styrofoam.

9.1.2 EFDOS/MDOS* Disk File

An EFDOS/MDOS* disk, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. **When using the EFDOS/MDOS* disk, include the entire memory image of both data and program space. All unused bytes, including the user's space, must be set to zero.**

9.2 VERIFICATION MEDIA

All original pattern media (EPROMs or floppy disk) are filed for contractual purposes and are not returned. A computer listing of the ROM code will be generated and returned along with a listing verification form. The listing should be thoroughly checked and the verification form completed, signed, and returned to THOMSON SEMICONDUCTEURS. The signed verification form constitutes the contractural agreement for creation of the customer mask. If desired, THOMSON SEMICONDUCTEURS will program a blank 2716, 2732, or EFDOS/MDOS* disk **(supplied by the customer)** from the data file used to create the custom mask to aid in the verification process.

* Requires prior factory approval

9.3 ROM VERIFICATION UNITS (RVUs)

Ten MCUs containing the customer's ROM pattern will be sent for program verification. These units will have been made using the custom mask but are for the purpose of ROM verification only. For expediency they are usually tested only at room temperature, five volts and may be unmarked and packaged in ceramic. These RVUs are included in the mask charge and are not production parts.

These RVUs are not backed nor guaranteed by THOMSON SEMICONDUCTEURS Quality Assurance.

9.4 FLEXIBLE DISKS

The disk media submitted must be single-sided single density, 8-inch, EFDOS/MDOS* compatible floppies. The customer must clearly label the disk with the ROM pattern file name. The minimum EFDOS/MDOS* system files as well as the absolute binary object file (file name. LO type of file) from the 6804 cross assembler must be on the disk. An object file made from a memory dump, using the ROLLOUT command is also admissable. Consider submitting a source listing as well as: file name, .LX (DEVICE/EXORciser loadable format). This file will of course be kept confidential and is used 1) to speed up the process in house if any problems arise, and 2) to speed up our customer to factory interface if a user finds any software errors and needs assistance quickly from THOMSON SEMICONDUCTEURS factory representatives.

EFDOS is THOMSON SEMICONDUCTEURS Disk Operating System available on development systems such as DEVICE.
MDOS is MOTOROLA's Disk Operating System available on development systems such as EXORciser . .
*Requires prior factory approval.

Whenever ordering a custom MCU is required, please contact your local THOMSON SEMICONDUCTEURS distributor and/or complete and send the attached "MCU customer ordering sheet SEMICONDUCTEURS representative.

ORDERING INFORMATION

EF6804J2 | P | V | ___

- EF6804J2 — Device
- P — Package
- V — Oper. temp.
- ___ — Screening level

The table below horizontally shows all available suffix combinations for package, operating temperature and screening level. Other possibilities on request.

DEVICE	PACKAGE					OPER. TEMP			SCREENING LEVEL			
	C	J	P	E	FN	L*	V	T	Std	D		
EF6804J2			●			●	●		●	●		

Examples : EF6804J2P, EF6804J2PV, EF6804J2PLD, EF6804J2PVD.

Package : C : Ceramic DIL, **P** : Plastic DIL, **FN** : PLCC.
Oper. temp. : L* : 0°C to +70°C, **V** : -40°C to +85°C, **T** : -40°C to +105°C, * : may be omitted.
Screening level : Std : (no-end suffix), **D** : NFC 96883 level D.

EXORciser is a registered trademark of Motorola Inc.

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

NOTES

EF6804 FAMILY – MCU CUSTOMER ORDERING SHEET

Commercial reference : E F 6 8 0 4 J 2 _ _ _

Customer's marking : _ _ _ _ _ _ _ _ _ _ _
11 characters max.

Application : .....
.....

ROM capacity required : _ _ _ _ bytes

Temperature range :
☐ 0°C/ +70°C
☐ −40°C/ +85°C
☐ -40°C/+105°C

Package :
☐ Plastic

Customer name : .....
Company : .....
Address : .....
Phone : .....

Specification reference :
☐ THOMSON SEMICONDUCTEURS reference .....
☐ Special customer data reference* .....

Number of interrupt vector : _ _

Quality level :
☐ STD
☐ D
☐ Other* (customer's quality specification ref.) :
.....

Software developed by :
☐ THOMSON SEMICONDUCTEURS application lab.
☐ External lab.
☐ Customer

PATTERN MEDIA (a listing may be supplied in addition for checking purposes) :

☐ EPROM Reference :

☐ EFDOS/MDOS* disk file (DEVICE/EXORciser)
☐ 8" floppy
☐ 5" 1/4 floppy

☐ Other*

OPTION LIST :
– Oscillator input :
☐ Xtal
☐ RC

– Interrupt Trigger
☐ Edge-sensitive
☐ Level-and edge-sensitive

– Port A output drive (4 I/Os)
☐ CMOS and TTL
☐ TTL only
☐ Open drain

– Port B output drive
☐ CMOS and TTL
☐ TTL only
☐ Open drain

* Requires prior factory approval

Yearly quantity forecast :

- start of production date :
- for a shipment period of :

CUSTOMER CONTACT NAME : DATE : SIGNATURE :

THOMSON SEMICONDUCTEURS
43 - 45, Avenue de l'Europe 78140 VELIZY-FRANCE Tel. (1) 39. 46.97.19 Telex : 240780F

THOMSON COMPONENTS SEMICONDUCTEURS

EF6804P2

8 BIT MICROCOMPUTER

ADVANCE INFORMATION

The EF6804P2 Microcomputer Unit (MCU) is a member of the EF6804 Family of very low-cost single-chip microcomputers. This 8-bit microcomputer contains a CPU, on-chip CLOCK, ROM, RAM, I/O, and TIMER. It is designed for the user who needs an economical microcomputer with the proven capabilities of the EF6800-based instruction set. The following are some of the hardware and software highlights of the EF6804P2 MCU.

HARDWARE FEATURES

- 8-Bit Architecture
- Pin Compatible with the EF6805P2 and EF68HC04P3
- 32 Bytes of RAM
- Memory Mapped I/O
- 1020 Bytes of User ROM
- 64 Bytes of ROM for Look-Up Tables
- 20 TTL/CMOS Compatible Bidirectional I/O Lines (Eight Lines are LED Compatible)
- 8-Bit Timer with 7-Bit Software Programmable Prescaler
- On-Chip Clock Generator
- Self-Check Mode and ROM Verify Mode
- Master Reset
- Complete Development System Support on DEVICE®
- 5 Volt Single Supply
- TIMER Pin is Programmable as Input or Output

SOFTWARE FEATURES

- Similar to EF6805 HMOS Family
- Byte Efficient Instruction Set
- Easy to Program
- True Bit Manipulation
- Bit Test and Branch Instruction
- Separate Flags for Interrupt and Normal Processing
- Versatile Indirect Registers
- Conditional Branches
- Single Instruction Memory Examine/Change
- True LIFO Stack Eliminates Stack Pointer
- Eight Powerful Addressing Modes
- Any Bit in Data Space Memory May be Tested
- Any Bit in Data Space Memory Capable of Being Written to May be Set or Cleared.

USER SELECTABLE OPTIONS

- 20 Bidirectional I/O Lines with LSTTL, LSTTL/CMOS, or Open-Drain Interface
- Crystal or Low-Cost Resistor-Capacitor Oscillator
- Mask Selectable Edge- or Level-Sensitive Interrupt Pin

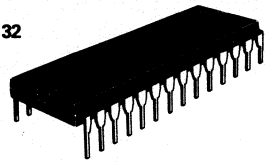
DEVICE® is THOMSON SEMICONDUCTEURS' development/emulation tool.

HMOS
(HIGH DENSITY
N-CHANNEL, SILICON-GATE
DEPLETION LOAD)

8-BIT MICROCOMPUTER

CASES

CB-132

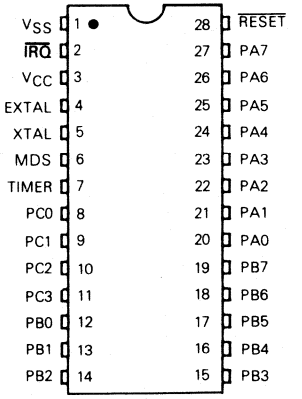


P SUFFIX
PLASTIC PACKAGE

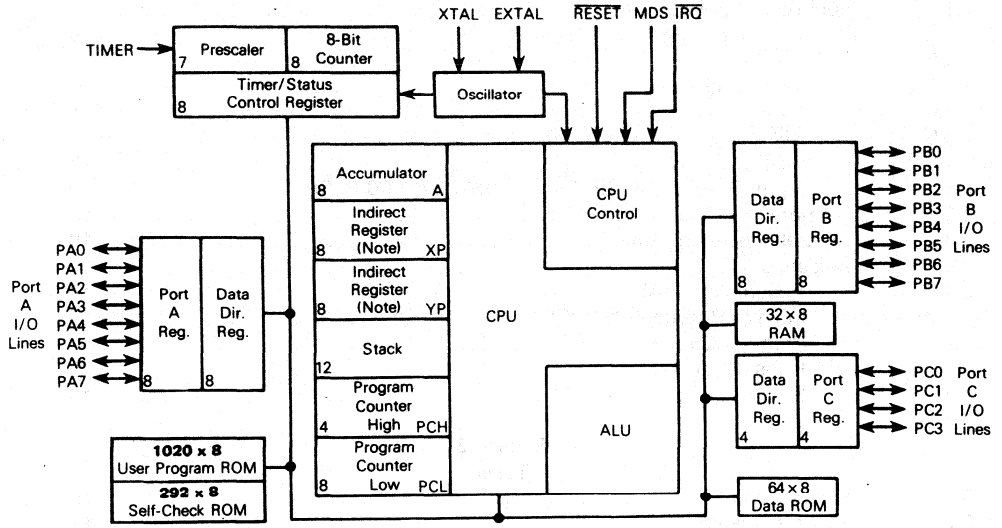
CB-520

FN SUFFIX
PLCC-28

PIN ASSIGNMENT



43, Avenue de l'Europe - 78140 VÉLIZY-VILLACOUBLAY/FRANCE - Tel.: (1) 39.46.97.19 - Telex TCSF 204780F - Telecopie: (1) 39.46.52.64



NOTE: 8-Bit indirect registers XP and YP, although shown as part of the CPU, are actually located in the 32 x 8 RAM at locations $80 and $81.

Figure 1-1. EF6804P2 MCU Block Diagram

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SECTION 2
FUNCTIONAL PIN DESCRIPTION, MEMORY, CPU, AND REGISTERS

This section provides a description of the functional pins, memory spaces, the central processing unit (CPU), and the various registers and flags.

2.1 FUNCTIONAL PIN DESCRIPTION

2.1.1 V_{CC} and V_{SS}

Power is supplied to the MCU using these two pins. V_{CC} is power and V_{SS} is the ground connection.

2.1.2 $\overline{IRQ}$

This pin provides the capability for asynchronously applying an external interrupt to the MCU. Refer to **4.1 INTERRUPT** for additional information.

2.1.3 XTAL and EXTAL

These pins provide connections to the on-chip clock oscillator circuit. A crystal, a resistor and capacitor, or an external signal, depending on the user selectable manufacturing mask option, can be connected to these pins to provide a system clock source with various stability/cost tradeoffs. Lead lengths and stray capacitance on these two pins should be minimized. Refer to **4.4 INTERNAL CLOCK GENERATOR OPTIONS** for recommendations concerning these inputs.

2.1.4 TIMER

In the input mode, the timer pin is connected to the prescaler input and serves as the timer clock. In the output mode, the timer pin signals that a time out of the timer has occurred. Refer to **SECTION 3 TIMER** for additional information.

2.1.5 $\overline{RESET}$

The $\overline{RESET}$ pin is used to restart the processor of the EF6804P2 to the beginning of a program. This pin, together with the MDS pin is also used to select the operating mode of the EF6804P2. If the MDS pin is at zero volts, the normal mode is selected and the program counter is loaded with the user restart vector. However, if the MDS pin is at +5 volts, then pins PA6 and PA7 are decoded to allow selection of the operating mode. Refer to **4.3 RESET** for additional information.

2.1.6 MDS

The MDS (mode select) pin is used to place the MCU into special operating modes. If MDS is held at +5 volts at the exit of the reset state, the decoded state of PA6 and PA7 is latched to determine the operating mode (single-chip, self-check, or ROM verify). However, if MDS is held at zero volts at the exit of the reset state, the single-chip operating mode is automatically selected (regardless of PA6 and PA7 state).

For those users familiar with the EF6801 microcomputer, mode selection is similar but much less complex in the EF6804P2. No special external diodes, switches, transistors, etc. are required in the EF6804P2.

2.1.7 Input/Output Lines (PA0-PA7, PB0-PB7, PC0-PC3)

These 20 lines are arranged into two 8-bit ports (A and B) and one 4-bit port (C). All lines are programmable as either inputs or outputs under software control of the data direction registers. Refer to **SECTION 5 INPUT/OUTPUT PORTS** for additional information.

2.2 MEMORY

The MCU operates in three different memory spaces: program space, data space, and stack space. A representation of these memory spaces is shown in Figure 2-1. The program space (Figure 2-1a) contains all of the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, and the self-check and user vectors. The data space (Figure 2-1b) contains all of the RAM locations, plus I/O locations and some ROM used for storage of tables and constants. The stack space (Figure 2-1c) contains RAM which is used for stacking subroutine and interrupt return addresses.

The MCU is capable of addressing 4096 bytes of program space memory with its program counter and 256 bytes of data space memory with its instructions. The data space memory contains three bytes for port data registers, three bytes for port data direction registers, one byte for timer status/control, 64 bytes ROM, 32 bytes RAM (which includes two bytes for XP and YP indirect registers), two bytes for timer prescaler and count registers, and one byte for the accumulator. The program space section includes 288 bytes of self-check ROM, 1016 bytes program ROM, and eight bytes of vectors for self-check and user programs.

2.3 CENTRAL PROCESSING UNIT

The CPU of the EF6804 Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control buses.

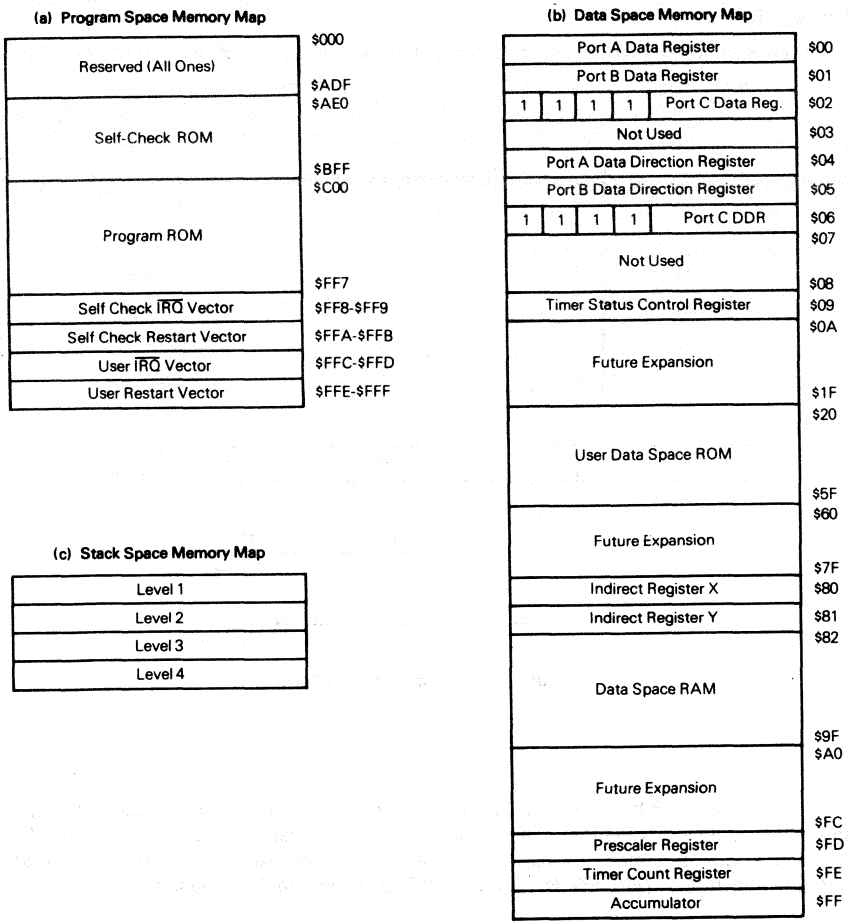


Figure 2-1. EF6804P2 MCU Address Map

2.4 REGISTERS

The EF6804 Family CPU has four registers and two flags available to the programmer. They are shown in Figure 2-2 and are explained in the following paragraphs.

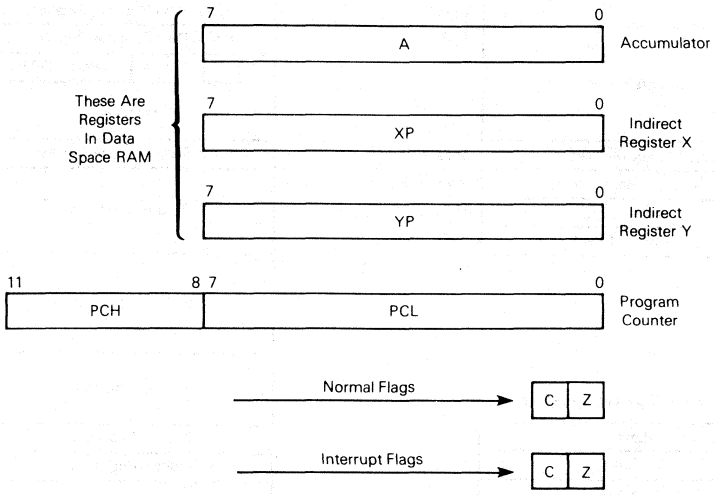


Figure 2-2. Programming Model

2.4.1 Accumulator (A)

The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator is implemented as the highest RAM location ($FF) in data space and thus implies that several instructions exist which are not explicitly implemented. Refer to **6.3 IMPLIED INSTRUCTIONS** for additional information.

2.4.2 Indirect Registers (XP, YP)

These two indirect registers are used to maintain pointers to other memory locations in data space. They are used in the register-indirect addressing mode, and can be accessed with the direct, indirect, short direct, or bit set/clear addressing modes. These registers are implemented as two of the 32 RAM locations ($80, $81) and as such generate implied instructions and may be manipulated in a manner similar to any RAM memory location in data space. Refer to **6.3 IMPLIED INSTRUCTIONS** for additional information.

2.4.3 Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next ROM word to be used (may be opcode, operand, or address of operand). The 12-bit program counter is contained in PCL (low byte) and PCH (high nibble).

2.4.4 Flags (C, Z)

The carry (C) bit is set on a carry or a borrow out of the ALU. It is cleared if the result of an arithmetic operation does not result in a carry or a borrow. The (C) bit is also set to the value of the bit tested in a bit test instruction, and participates in the rotate left instruction.

The zero (Z) bit is set if the result of the last arithmetic or logical operation was equal to zero, otherwise it is cleared.

There are two sets of these flags, one set is for interrupt processing, the other for all other routines. When an interrupt occurs, a context switch is made from the program flags to the interrupt flags (interrupt mode). An RTI forces the context switch back to the program flags (program mode). While in either mode, only the flags for that mode are available. Further, the interrupt flags will not be cleared upon entering the interrupt mode. Instead, the flags will be as they were at the exit of the last interrupt mode. Both sets of flags are cleared by reset.

2.4.5 Stack

There is a true LIFO stack incorporated in the EF6804P2 which eliminates the need for a stack pointer. Stack space is implemented in separate RAM (12-bits wide) shown in Figure 2-1c. Whenever a subroutine call (or interrupt) occurs, the contents of the PC are shifted into the top register of the stack. At the same time (same cycle), the top register is shifted to the next level deeper. This happens to all registers with the bottom register falling out the bottom of the stack.

Whenever a subroutine or interrupt return occurs, the top register is shifted into the PC and all lower registers are shifted up one level higher. The stack RAM is four levels deep. If the stack is pulled more than four times without any pushes, the address that was stored in the bottom level will be shifted into the PC.

SECTION 3
TIMER

3.1 INTRODUCTION

A block diagram of the EF6804P2 timer circuitry is shown in Figure 3-1. The timer logic in the MCU is comprised of a simple 8-bit counter (timer count register, TCR) with a 7-bit prescaler, and a timer status/control register (TSCR). The timer count register, which may be loaded under program control, is decremented towards zero by a clock input (prescaler output). The prescaler is used to extend the maximum interval of the overall timer. The prescaler tap is selected by bits 0-2 (PS0-PS2) of the timer status/control register. Bits PS0-PS2 control the actual division of the prescaler within the range of divide-by-1 (2^0) to divide-by-128 (2^7). The timer count register (TCR) and prescaler are decremented on rising clock edges. The coding of the TCSR PS0-PS2 bits produce a division in the prescaler as shown in Table 3-1.

Table 3-1. Prescaler Coding Table

PS2	PS1	PS0	Divide By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8

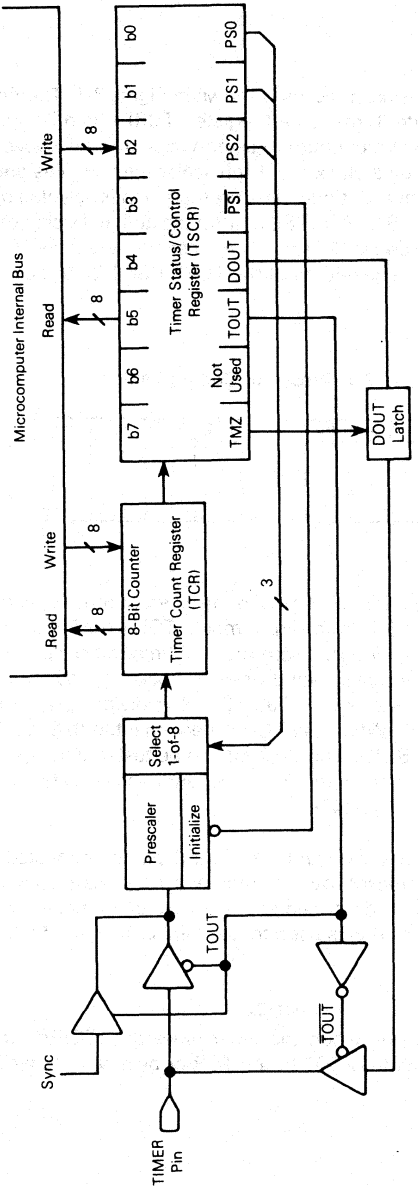
PS2	PS1	PS0	Divide By
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The TIMER pin may be programmed as either an input or an output depending on the status of TOUT (TSCR bit 5). Refer to Figure 3-1. In the input mode, TOUT is a logic zero and the TIMER pin is connected directly to the prescaler input. Therefore, the timer prescaler is clocked by the signal applied from the TIMER pin. The prescaler then divides its clock input by a value determined by the coding of the TSCR bits PS0-PS2 as shown in Table 3-1. The divided prescaler output then clocks the 8-bit timer count register (TCR). When the TCR is decremented to zero, it sets the TMZ bit in the timer status/control register (TSCR). The TMZ bit can be tested under program control to perform a timer function whenever it goes high. The frequency of the external clock applied to the TIMER pin must be less than t_{byte} ($f_{osc}/48$).

In the output mode, TOUT is a logic one and the TIMER pin is connected to the DOUT latch. Therefore, the timer prescaler is clocked by the internal sync pulse (divide-by-48 of the internal oscillator). Operation is similar to that described above for the input mode. However, in the output mode, the low-to-high TMZ bit transition is used to latch the DOUT bit of the TSCR and provide it as output for the TIMER pin.

NOTE

TMZ is normally set to logic one when the timer times out (TCR decrements to $00); however, it may be set by a write of $00 to the TCR or by a write to bit 7 of the TSCR.



TIMER Pin Status

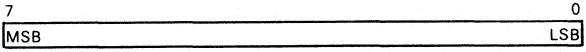
TOUT	Prescaler Clock	TIMER Pin
0	TIMER Pin Sync	Input Mode
1		Output Mode

Figure 3-1. Timer Block Diagram

During reset, the timer count register and prescaler are set to $FF, while the timer status/control register is cleared to $00 and the DOUT LATCH (TIMER pin is in the high-impedance input mode) is forced to a logic high. The prescaler and timer count register are implemented in data space RAM locations ($FD, $FE); therefore, they are both readable and writeable. A write to either will predominate over the TCR decrement-to-$00 function; i.e., if a write and a TCR decrement-to-$00 occur simultaneously, the write will take precedence, and the TMZ bit is not set until the next timer time out.

3.2 TIMER REGISTERS

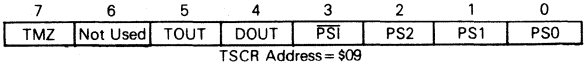
3.2.1 Timer Count Register (TCR)



TCR Address = $FE

The timer count register indicates the state of the internal 8-bit counter.

3.2.2 Timer Status/Control Register (TSCR)



TSCR Address = $09

b7, TMZ — Low-to-high transition indicates the timer count register has decremented to zero since the timer status/control register was last read. Cleared by a read of TSCR register if TMZ was read as a logic one.

b6 — Not used.

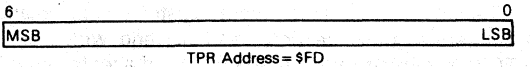
b5, TOUT — When low, this bit selects the input mode for the timer. When high, the output mode is selected.

b4, DOUT — Data sent to the timer output pin when TMZ is set high (output mode only).

b3, $\overline{PSI}$ — Used to initialize the prescaler and inhibit its counting while $\overline{PSI} = 0$. The initialized value is set to $FF. The timer count register will also be inhibited (contents unchanged). When $\overline{PSI} = 1$ the prescaler begins to count downward.

b0, b1, b2 **PS0-PS1-PS2** — These bits are used to select the prescaler divide-by ratio; therefore, effecting the clock input frequency to the timer count register.

3.2.3 Timer Prescaler Register



TPR Address = $FD

The timer prescaler register indicates the state of the internal 7-bit prescaler. This 7-bit prescaler divide ratio is normally determined by bits PS0-PS2 of the timer status/control register (see Table 3-1).

SECTION 4
INTERRUPT, SELF-CHECK, RESET, AND INTERNAL CLOCK GENERATOR

4.1 INTERRUPT

The EF6804P2 can be interrupted by applying a logic low signal to the $\overline{IRQ}$ pin ; however, a mask option selected at the time of manufacture determines whether the negative-going edge or the actual low level is sensed to indicate an interrupt.

4.1.1 Edge-Sensitive Option

When the $\overline{IRQ}$ pin is pulled low, the internal interrupt request latch is set. Prior to each instruction fetch, the interrupt request latch is tested and, if its output is high, an interrupt sequence is initiated at the end of the current instruction (provided the interrupt mask is cleared). Figure 4-1 contains a flowchart which illustrates both the reset and interrupt sequence. The interrupt sequence consists of one cycle during which: the interrupt request latch is cleared, the interrupt mode flags are selected, the PC is saved on the stack, the interrupt mask is set, and the $\overline{IRQ}$ vector (single chip mode= $FFC/$FFD, self-check mode= $FF8/$FF9) is loaded into the PC. Internal processing of the interrupt continues until an RTI (return from interrupt) instruction is processed. During the RTI instruction, the interrupt mask is cleared and the program mode flags are selected. The next instruction of the program is then fetched and executed. Once the interrupt was initially detected and the interrupt sequence started, the interrupt request latch is cleared so that the next (second) interrupt may be detected even while the previous (first) one is being serviced. However, even though the second interrupt sets the interrupt request latch during processing of the first interrupt, the second interrupt sequence will not be initiated until completion of the interrupt service routine for the first interrupt. Completion of an interrupt service routine is always accomplished using an RTI instruction to return to the main program. The interrupt mask (which is not directly available to the programmer) is cleared during the last cycle of the RTI instruction.

4.1.2 Level-Sensitive Option

The actual operation of the level-sensitive and edge-sensitive options are similar except that the level-sensitive option does not have an interrupt request latch. With no interrupt request latch, the logic level of the $\overline{IRQ}$ pin is checked for detection of the interrupt. Also, in the interrupt sequence, there is no need to clear the interrupt request latch. These differences are illustrated in the flowchart of Figure 4-1.

4.1.3 Power Up and Timing

During the power-up sequence the interrupt mask is set to preclude any false or "ghost" interrupts from occurring. To clear the interrupt mask, the programmer should write a JSR (instead of a JMP) instruction to an initialization routine as the first instruction in a program. The initialization routine

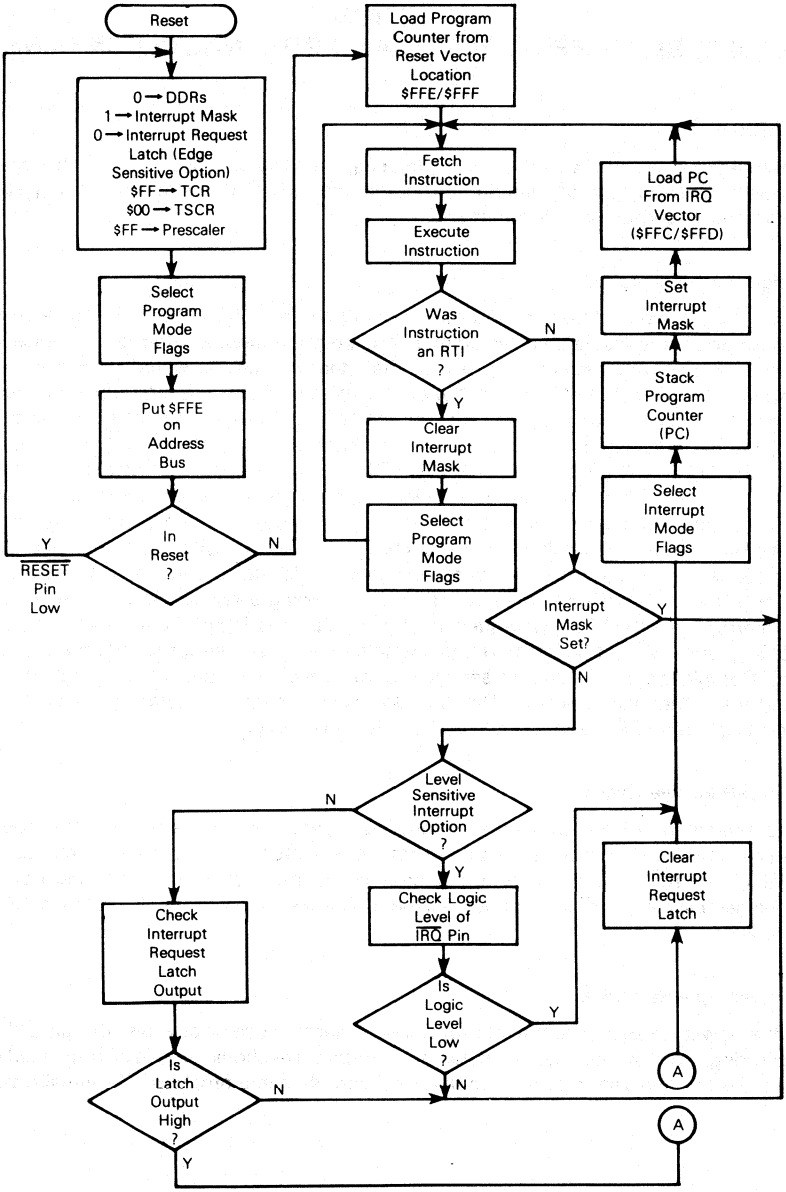


Figure 4-1. Reset and Interrupt Processing Flowchart

should end with an RTI (instead of RTS). Maximum interrupt response time is eight machine (t_{byte}) cycles (see **4.4 INTERNAL CLOCK GENERATOR OPTIONS**). This includes five machine cycles for the longest instruction, plus one machine cycle for stacking the PC and switching flags, plus two machine cycles for synchronization of the $\overline{IRQ}$ input with the internal clock. Minimum response time is one machine cycle for stacking PC and switching flags (see **2.4.4 Flags (C, Z)**).

4.2 SELF-CHECK

The self check capability of the EF6804P2 MCU provides an internal check to determine if the part is functional. A schematic diagram of the self-check connections is shown in Figure 4-2. To perform a functional check of the MCU, connect it as shown in Figure 4-2a and monitor the LEDs for a 00100 ($04) pattern on port A. To initiate a ROM self-check of the memory simply connect the circuit as shown in Figure 4-2b and check that the "good" LED turns on to indicate a good memory. The ROM verify uses a cyclical redundancy check (CRC) to conduct a ROM check by means of signature analysis circuit. This circuit consists of two 8-bit shift registers configured to perform the check using the CCITT polynominal.

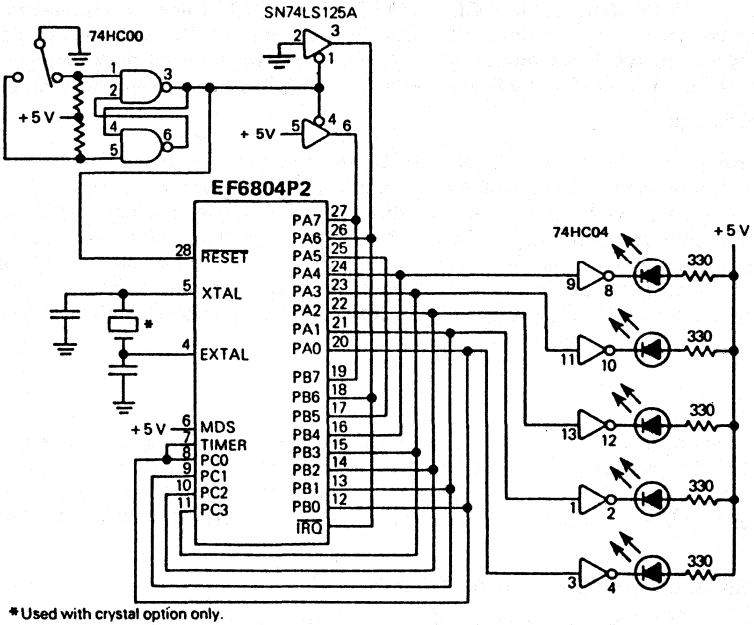
4.3 RESET

The MCU can be reset in two ways: by initial power up (see Figure 4-1) and by the external reset input ($\overline{RESET}$). During power up, a delay of t_{RHL} is needed before allowing the $\overline{RESET}$ input to go high. This time delay allows the internal clock generator to stabilize. Connecting a capacitor and resistor to the $\overline{RESET}$ input, as shown in Figure 4-3, typically provides sufficient delay.

4.4 INTERNAL CLOCK GENERATOR OPTIONS

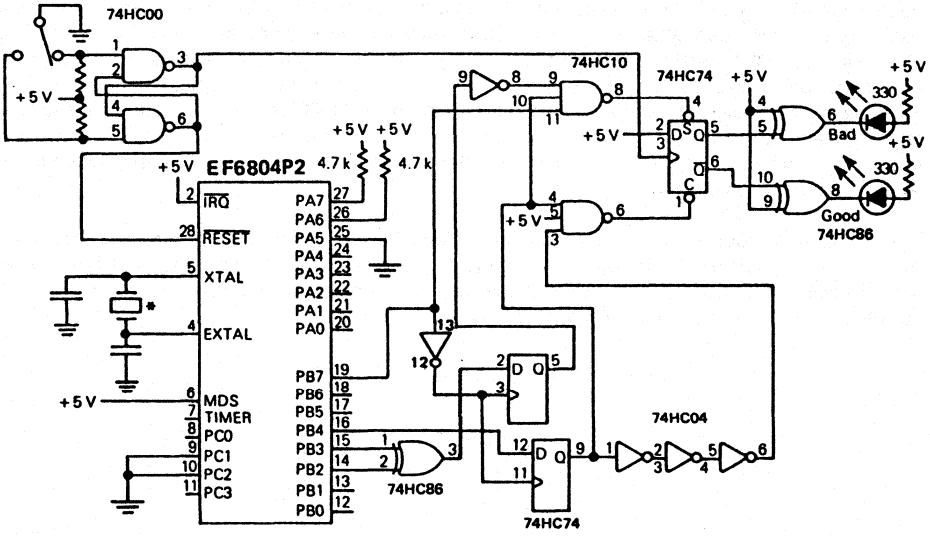
The internal clock generator circuit is designed to require a minimum of external components. A crystal, a resistor-capacitor, or an external signal may be used to generate a system clock with various stability/cost tradeoffs. A manufacturing mask option is required to select either the crystal oscillator or the RC oscillator circuit. The different clock generator option connection methods are shown in Figure 4-4, crystal specifications and suggested PC board layouts are given in Figure 4-5, resistor-capacitor selection graph is given in Figure 4-6, and a timing diagram is illustrated in Figure 4-7. The crystal oscillator startup time is a function of many variables: crystal parameters (especially R_S), oscillator load capacitance (C_L), IC parameters, ambient temperature, and supply voltage. To ensure rapid oscillator startup, neither the crystal characteristics nor the load capacitance should exceed recommendations.

The oscillator output frequency is internally divided by four to produce the internal $\phi 1$ and $\phi 2$ clocks. The $\phi 1$ clock is divided by twelve to produce a machine byte (cycle) clock. A byte cycle is the smallest unit needed to execute any operation (i.e., increment the program counter). An instruction may need two, four, or five byte cycles to execute.



*Used with crystal option only.

(a) Functional Check



*Used with crystal option only.

(b) Simple ROM Verify Check

Figure 4-2. Self-Check Circuit

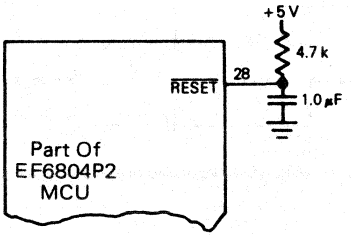
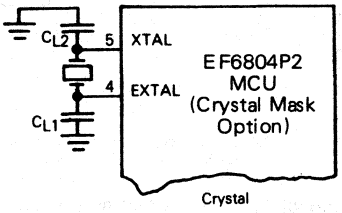


Figure 4-3. Power-Up Reset Delay Circuit



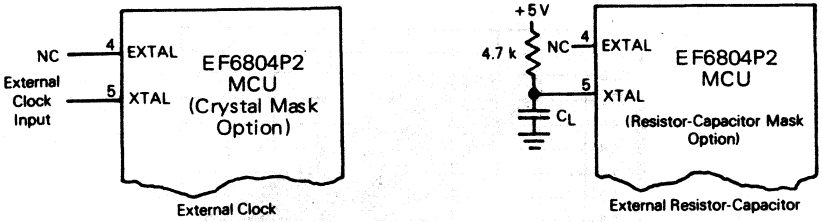


Figure 4-4. Clock Generator Options

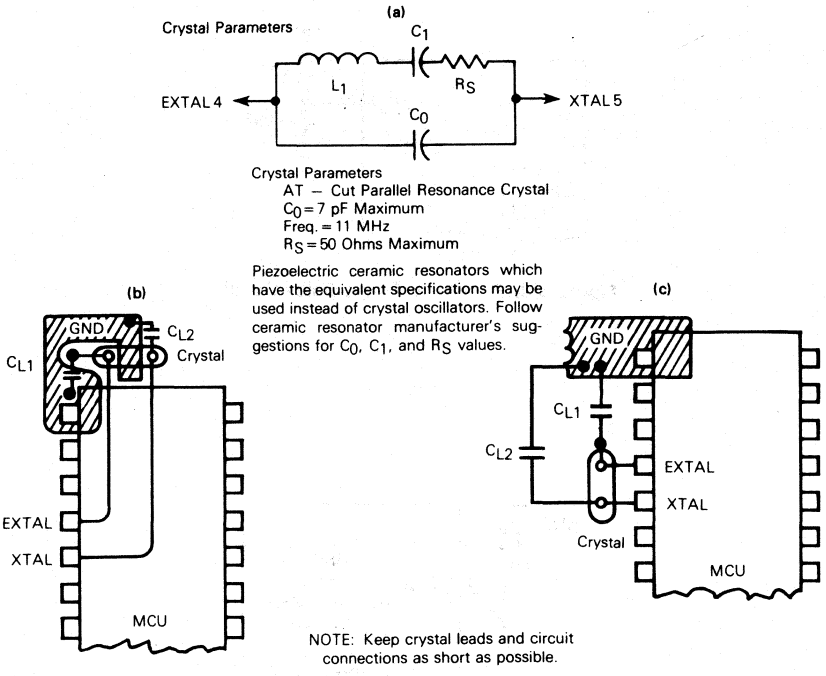


Figure 4-5. Crystal Motional Arm Parameters and Suggested PC Board Layout

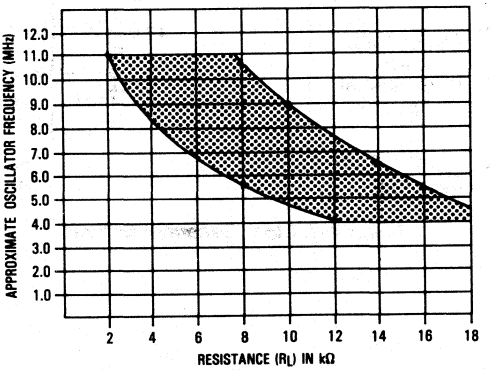


Figure 4-6. Typical Frequency Selection For Resistor-Capacitor Oscillator Option (C_L = 17 pF)

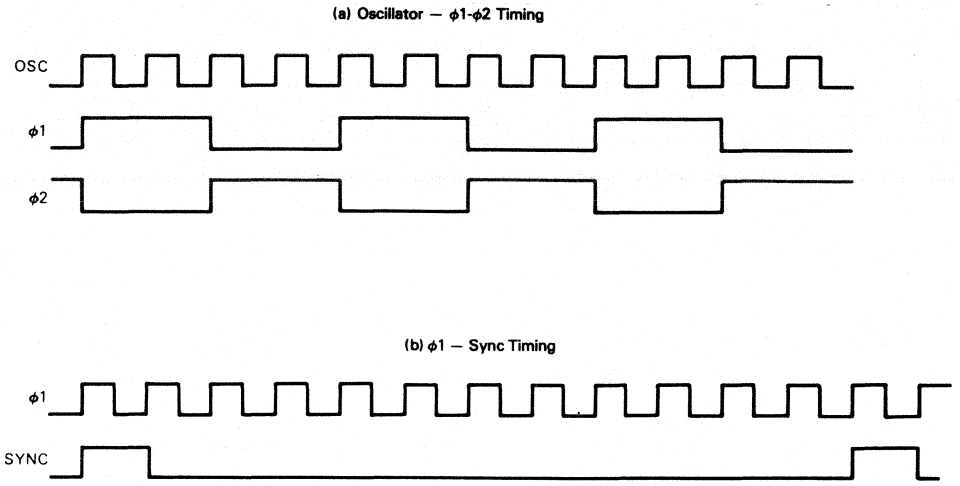
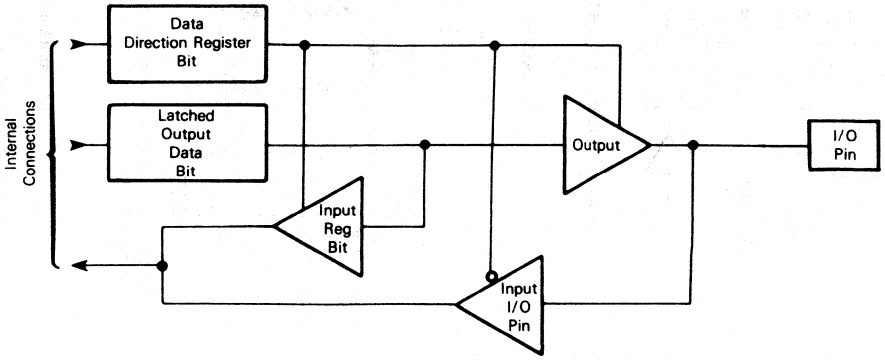


Figure 4-7. Clock Generator Timing Diagram

SECTION 5
INPUT/OUTPUT PORTS

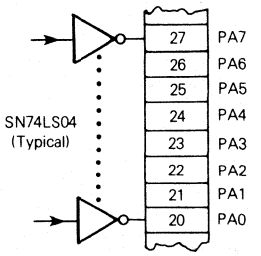
5.1 INPUT/OUTPUT

There are 20 input/output pins. All pins (port A, B, and C) are programmable as either inputs or outputs under software control of the corresponding data direction register (DDR). The port I/O programming is accomplished by writing the corresponding bit in the port DDR to a logic one for output or a logic zero for input. On reset, all the DDRs are initialized to a logic zero state to put the ports in the input mode. The port output registers are not initialized on reset but should be initialized before changing the DDR bits to avoid undefined levels. When programmed as outputs, the latched output data is readable as input data, regardless of the logic levels at the output pin due to output loading; see Figure 5-1. All input/output pins are LSTTL compatible as both inputs and outputs. In addition, all three ports may have one of two mask options: 1) internal pullup resistor for CMOS output compatibility, or 2) open drain output. The address map in Figure 2-1 gives the address of data registers and DDRs. The register configuration is discussed under the registers paragraph below and Figure 5-2 provides some examples of port connections.

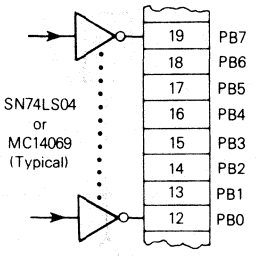


Data Direction Register Bit	Output Data Bit	Output State	Input To MCU
1	0	0	0
1	1	1	1
0	X	Hi-Z	Pin

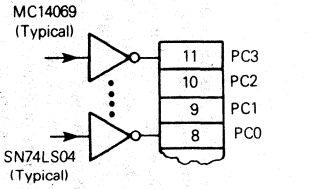
Figure 5-1. Typical I/O Port Circuitry



LSTTL Driving Port A Directly

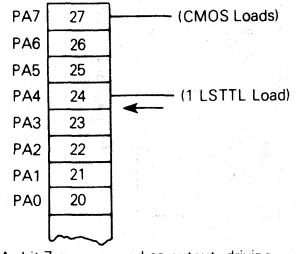


CMOS or LSTTL Driving Port B Directly

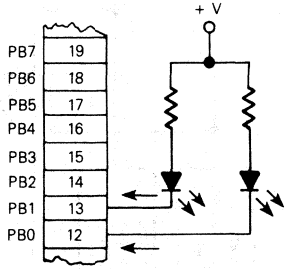


CMOS and LSTTL Driving Port C Directly

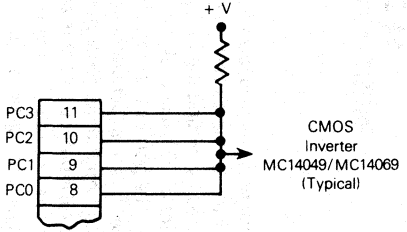
(a) Input Mode



Port A, bit 7 programmed as output, driving CMOS loads and bit 4 driving one LSTTL load directly (using CMOS output option).



Port B, bit 0, and bit 1 programmed as output, driving LEDs directly.



Port C open drain option, with bits 0-3 programmed as output, driving CMOS load via wired-ORed configuration.

(b) Output Mode

Figure 5-2. Typical Port Connections

The latched output data bit (see Figure 5-1) may always be written. Therefore, any write to a port writes to all of its data bits even though the port DDR is set to input. This may be used to initialize the data registers and avoid undefined outputs; however, care must be exercised when using read-modify-write instructions since the data read corresponds to the pin level if the DDR is an input (0) and corresponds to the latched output data when the DDR is an output (1). The 20 bidirectional lines may be configured by port to be LSTTL (standard configuration), LSTTL/CMOS (mask option), or open drain (mask option). Port B outputs are LED compatible.

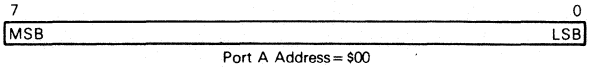
NOTE

The mask option only allows changes by port. For example, if the customer wishes PA7 to be open drain, then PA0-PA7 must all be open drain.

5.2 REGISTERS

The registers described below are implemented as RAM locations and thus may be read or written.

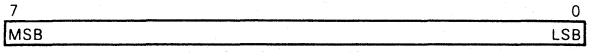
5.2.1 Port Data Register



Port A Address = $00
Port B Address = $01
Port C Address = $02 (Bits 0-3)

The source of data read from the port data register will be the port I/O pin or previously latched output data depending upon the contents of the corresponding data direction register (DDR). The destination of data written to the port data register will be an output data latch. If the corresponding data direction register (DDR) for the port I/O pin is programmed as an output, the data will then appear on the port pin.

5.2.2 Port Data Direction Register



Port A Address = $04
Port B Address = $05
Port C Address = $06 (Bits 0-3)

The port DDRs configure the port pins as either inputs or outputs. Each port pin can be programmed individually to act as an input or an output. A zero in the pins corresponding bit position will program that pin as an input while a one in the pins corresponding bit position will program that pin as an output.

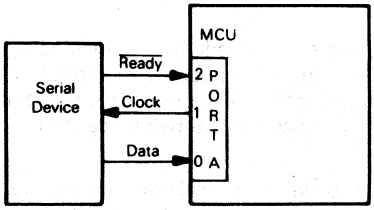
SECTION 6
SOFTWARE AND INSTRUCTION SET

6.1 SOFTWARE

6.1.1 Bit Manipulation

The EF6804P2 MCU has the ability to set or clear any register or single random access memory (RAM) writable bit with a single instruction (BSET, BCLR). Any bit in data space, including ROM, can be tested, using the BRSET and BRCLR instructions, and the program may branch as a result of its state. The carry bit equals the value of the bit referenced by BRSET or BRCLR. A rotate instruction may then be used to accumulate serial input data in a RAM location or register. The capability to work with any bit in RAM, ROM, or I/O allows the user to have individual flags in RAM or to handle I/O bits as control lines.

The coding example in Figure 6-1 illustrates the usefulness of the bit manipulation and test instructions. Assume that the MCU is to communicate with an external serial device. The external device has a data ready signal, a data output line, and a clock line (to clock data one bit at a time, MSB first, out of the device). The MCU waits until the data is ready, clocks the external device, picks up the data in the carry flag (C bit), clears the clock line, and finally accumulates the data bit in the accumulator.




```
                .
                .
                .
SELF    BRSET   2,PORTA,SELF
                .
                .
                .
        BSET    1,PORTA
        BRCLR   0,PORTA,CONT
CONT    BCLR    1,PORTA
        ROLA    .
                .
                .
                .
```

Figure 6-1. Bit Manipulation Example

6.1.2 Addressing Modes

The EF6804P2 MCU has nine addressing modes which are explained briefly in the following paragraphs. The EF6804P2 deals with objects in three different address spaces : program space, data space, and stack space. Program space contains the instructions which are to be executed, plus the data for immediate mode instructions. Data space contains all of the RAM locations, XP and YP registers, accumulator, timer, I/O locations, and some ROM (for storage of tables and constants). Stack space contains RAM for use in stacking the return addresses for subroutines and interrupts.

The term "Effective Address" (EA) is used in describing the address modes. EA is defined as the address from which the argument for an instruction is fetched or stored.

6.1.2.1 IMMEDIATE. In the immediate addressing mode, the operand is located in program ROM and is contained in a byte following the opcode. The immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

6.1.2.2 DIRECT. In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the 256 bytes in data space memory with a single two-byte instruction.

6.1.2.3 SHORT DIRECT. The MCU also has four locations in data space RAM ($80, $81, $82, $83) which may be used in a short-direct addressing mode. In this mode the opcode determines the data space RAM location, and the instruction is only one byte. Short direct addressing is a subset of the direct addressing mode. (The XP and YP registers are at locations $80 and $81 respectively.)

6.1.2.4 EXTENDED. In the extended addressing mode, the effective address is obtained by concatenating the four least significant bits of the opcode with the byte following the opcode (12-bit address). Instructions using the extended addressing mode (JMP, JSR) are capable of branching anywhere in program space. An extended addressing mode instruction is two bytes long.

6.1.2.5 RELATIVE. The relative addressing mode is only used in conditional branch instructions. In relative addressing, that address is formed by adding the sign extended lower five bits of the opcode (the offset) to the program counter if and only if the condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from -15 to $+16$ from the opcode address. The programmer need not worry about calculating the correct offset when using the assembler since it calculates the proper offset and checks to see if it is within the span of the branch.

6.1.2.6 BIT SET/CLEAR. In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode specifies the direct address of the byte in which the specified bit is to be set or cleared. Thus, any bit in the 256 locations of data space memory, which can be written to, can be set or cleared.

6.1.2.7 BIT TEST AND BRANCH. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit and condition (set or clear) which is to be tested is included in the opcode, and the data space address of the byte to be tested is in the single byte immediately following the opcode byte. The third byte is sign extended to twelve bits and becomes the offset added to the program counter if the condition is true. The single three-byte instruction allows the program to branch based on the condition of any bit in data space memory. The span of branching is from −125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry flag.

6.1.2.8 REGISTER-INDIRECT. In the register-indirect addressing mode, the operand is at the address (in data space) pointed to by the contents of one of the indirect registers (X or Y). The particular X or Y register is selected by bit 4 of the opcode. Bit 4 of the opcode is then decoded into an address which selects the desired X or Y register ($80 or $81). A register-indirect instruction is one byte long.

6.1.2.9 INHERENT. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

6.2 INSTRUCTION SET

The EF6804P2 MCU has a set of 42 basic instructions which when combined with nine addressing modes produce 242 usable opcodes. They can be divided into five different types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

6.2.1 Register/Memory Instructions

Most of these instructions use two operands. One operand is the accumulator and the other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operands. Refer to Table 6-1.

6.2.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. There are ten instructions which utilize read-modify-write cycles. All INC and DEC forms along with all bit manipulation instructions use this method. Refer to Table 6-2.

6.2.3 Branch Instructions

The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 6-3.

6.2.4 Bit Manipulation Instructions

These instructions are used on any bit in data space memory. One group either sets or clears. The other group performs the bit test branch operations. Refer to Table 6-4.

Table 6-1. Register/Memory Instructions

		Addressing Modes																			
		Indirect				Immediate			Direct			Inherent			Extended			Short-Direct			
Function	Mnem	Opcode XP	Opcode YP	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Special Notes
Load A from Memory	LDA	E0	F0	1	4	E8	2	4	F8	2	4	–	–	–	–	–	–	AC-AF	1	4	1
Load XP from Memory	LDXI	–	–	–	–	B0	3	4	–	–	–	–	–	–	–	–	–	–	–	–	4
Load YP from Memory	LDYI	–	–	–	–	B0	3	4	–	–	–	–	–	–	–	–	–	–	–	–	4
Store A in Memory	STA	E1	F1	1	4	–	–	–	F9	2	4	–	–	–	–	–	–	BC-BF	1	4	2
Add to A	ADD	E2	F2	1	4	EA	2	4	FA	2	4	–	–	–	–	–	–	–	–	–	–
Subtract from A	SUB	E3	F3	1	4	EB	2	4	FB	2	4	–	–	–	–	–	–	–	–	–	–
Arithmetic Compare with Memory	CMP	E4	F4	1	4	EC	2	4	FC	2	4	–	–	–	–	–	–	–	–	–	–
AND Memory to A	AND	E5	F5	1	4	ED	2	4	FD	2	4	–	–	–	–	–	–	–	–	–	–
Jump to Subroutine	JSR	–	–	–	–	–	–	–	–	–	–	–	–	–	8 (TAR)	2	4	–	–	–	3
Jump Unconditional	JMP	–	–	–	–	–	–	–	–	–	–	–	–	–	9 (TAR)	2	4	–	–	–	3
Clear A	CLRA	–	–	–	–	–	–	–	FB	2	4	–	–	–	–	–	–	–	–	–	–
Clear XP	CLRX	–	–	–	–	–	–	–	FB	2	4	–	–	–	–	–	–	–	–	–	–
Clear YP	CLRY	–	–	–	–	–	–	–	FB	2	4	–			–	–	–	–	–	–	–
Complement A	COMA	–	–	–	–	–	–	–	–	–	–	B4	1	4	–	–	–	–	–	–	–
Move Immediate Value to Memory	MVI	–	–	–	–	B0	3	4	B0	3	4	–	–	–	–	–	–	–	–	–	5
Rotate A Left and Carry	ROLA	–	–	–	–	–	–	–	–	–	–	B5	1	4	–	–	–	–	–	–	–
Arithmetic Left Shift of A	ASLA	–	–	–	–	–	–	–	FA	2	4	–	–	–	–	–	–	–	–	–	–

SPECIAL NOTES

1. In Short-Direct addressing, the LDA mnemonic represents opcode AC, AD, AE, and AF. This is equivalent to RAM locations $80 (AC), $81 (AD), $82 (AE), and $83 (AF)
2. In Short-Direct addressing, the STA mnemonic represents opcode BC, BD, BE, and BF. This is equivalent to RAM locations $80 (BC), $81 (BD), $82 (BE), and $83 (BF).
3. In Extended addressing, the four LSBs of the opcode (Mnemonic JSR and JMP) are formed by the four MSBs of the target address. (TAR)
4. In Immediate addressing, the LDXI and LDYI are mnemonics which are recognized as follows:
   LDXI = MVI $80,data
   LDYI = MVI $81,data Where data is a one-byte hexadecimal number.
5. The MVI instruction refers to both Immediate and Direct addressing.

Table 6-2. Read-Modify-Write Instructions

		Addressing Modes										
		Indirect				Direct			Short-Direct			
Function	Mnem	Opcode XP	Opcode YP	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Special Notes
Increment Memory Location	INC	E6	F6	1	4	FE	2	4	A8-AB	1	4	1, 3
Increment A	INCA	—	—	—	—	FE	2	4	—	—	—	—
Increment XP	INCX	—	—	—	—	—	—	—	A8	1	4	—
Increment YP	INCY	—	—	—	—	—	—	—	A9	1	4	—
Decrement Memory Location	DEC	E7	F7	1	4	FF	2	4	B8-BB	1	4	2, 4
Decrement A	DECA	—	—	—	—	FF	2	4	—	—	—	—
Decrement XP	DECX	—	—	—	—	—	—	—	B8	1	4	—
Decrement YP	DECY	—	—	—	—	—	—	—	B9	1	4	—

SPECIAL NOTES

1. In Short-Direct addressing, the INC mnemonic represents opcode A8, A9, AA, and AB. These are equivalent to RAM locations $80 (A8), $81 (A9), $82 (AA), and $83 (AB).
2. In Short-Direct addressing, the DEC mnemonic represents opcode B8, B9, BA, and BB. These are equivalent to RAM locations $80 (B8), $81 (B9), $82 (BA), and $83 (BB).
3. In Indirect addressing, the INC mnemonic represents opcode E6 or F6, and causes the location pointed to by XP (E6 opcode) or YP (F6 opcode) to be incremented.
4. In Indirect addressing, the INC mnemonic represents opcode E7 or F7, and causes the location pointed to by XP (E7 opcode) or YP (F7 opcode) to be incremented.

Table 6-3. Branch Instructions

Function	Mnem	Relative Addressing Mode			Special Notes
		Opcode	# Bytes	# Cycles	
Branch if Carry Clear	BCC	40-5F	1	2	1
Branch if Higher or Same	(BHS)	40-5F	1	2	1, 2
Branch if Carry Set	BCS	60-7F	1	2	1
Branch if Lower	(BLO)	60-7F	1	2	1, 3
Branch if Not Equal	BNE	00-1F	1	2	1
Branch if Equal	BEQ	20-3F	1	2	1

SPECIAL NOTES

1. Each mnemonic of the Branch Instructions covers a range of 32 opcodes; e.g., BCC ranges from 40 through 5F. The actual memory location (target address) to which the branch is made is formed by adding the sign extended lower five bits of the opcode to the contents of the program counter.
2. The BHS instruction (shown in parentheses) is identical to the BCC instruction. The C bit is clear if the register was higher or the same as the location in the memory to which it was compared.
3. The BLO instruction (shown in parentheses) is identical to the BCS instruction. The C bit is set if the register was lower than the location in memory to which it was compared.

Table 6-4. Bit Manipulation Instructions

Function	Mnem	Addressing Modes						Special Note
		Bit Set/Clear			Bit Test and Branch			
		Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	
Branch IFF Bit n is set	BRSET n (n=0 . . . . 7)	–	–	–	C8+n	3	5	1
Branch IFF Bit n is clear	BRCLR n (n=0 . . . . 7)	–	–	–	C0+n	3	5	1
Set Bit n	BSET n (n=0 . . . .7)	D8+n	2	4	–	–	–	1
Clear Bit n	BCLR n (n=0 . . . . 7)	D0+n	2	4	–	–	–	1

SPECIAL NOTE

1. The opcode is formed by adding the bit number (0-7) to the basic opcode. For example: to clear bit six using the BSET6 instruction the opcode becomes DE (D8+6); BCLR5 becomes (C0+5); etc.

6.2.5 Control Instructions

The control instructions control the MCU operations during program execution. Refer to Table 6-5.

6.2.6 Alphabetical Listing

The complete instruction set is given in alphabetical order in Table 6-6. There are certain mnemonics recognized by the assember and converted to other instructions. The fact that all registers and accumulator are in RAM allows many implied instructions to exist. The implied instructions recognized by the assembler are identified in Table 6-6.

6.2.7 Opcode Map Summary

Table 6-7 contains an opcode map for the instructions used on the MCU.

6.3 IMPLIED INSTRUCTIONS

Since the accumulator and all other registers are located in RAM many implied instructions exist. The assembler-recognized implied instructions are given in Table 6-6. Some examples not recognized by the assembler are shown below.

BCLR,7 $FF	Ensures accumulator is plus
BSET,7 $FF	Ensures accumulator is minus
BRCLR,7 $FF	Branch iff accumulator is plus
BRSET,7 $FF	Branch iff accumulator is minus
BRCLR,7 $80	Branch iff X is plus (BXPL)
BRSET,7 $80	Branch iff X is minus (BXMI)
BRCLR,7 $81	Branch iff Y is plus (BYPL)
BRSET,7 $81	Branch iff Y is minus (BYMI)

Table 6-5. Control Instructions

		Addressing Modes									
		Short-Direct			Inherent			Relative			
Function	Mnem	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Special Notes
Transfer A to XP	TAX	BC	1	4	–	–	–	–	–	–	–
Transfer A to YP	TAY	BD	1	4	–	–	–	–	–	–	–
Transfer XP to A	TXA	AC	1	4	–	–	–	–	–	–	–
Transfer YP to A	TYA	AD	1	4	–	–	–	–	–	–	–
Return from Subroutine	RTS	–	–	–	B3	1	2	–	–	–	–
Return from Interrupt	RTI	–	–	–	B2	1	2	–	–	–	–
No-Operation	NOP	–	–	–	–	–	–	–	–	–	1

SPECIAL NOTE

1 . The NOP instruction is equivalent to a branch if equal (BEQ) to the location designated by PC + 1.

Table 6-6. Instruction Set

Mnemonic	Addressing Modes									Flags	
	Inherent	Immediate	Direct	Short Direct	Bit/Set Clear	Bit-Test-Branch	Register Indirect	Extended	Relative	Z	C
ADD		X	X				X			Λ	Λ
AND		X	X				X			Λ	•
ASLA	Assembler converts this to "ADD $FF"									•	•
BCC									X	Λ	Λ
BCLR					X					•	•
BCS									X	•	•
BEQ									X	•	•
BHS	Assembler converts this to "BCC"									•	•
BLO	Assembler converts this to "BCS"									•	•
BNE									X	•	•
BRCLR						X				•	Λ
BRSET						X				•	Λ
BSET					X					•	•
CLRA	Assembler converts this to "SUB $FF"									Λ	Λ
CLRX	Assembler converts this to "MVI # 0, $80"									•	•
CLRY	Assembler converts this to "MVI # 0, $81"									•	•
CMP		X	X				X			Λ	Λ
COMA	X									Λ	Λ
DEC			X	X			X			Λ	•
DECA	Assembler converts this to "DEC $FF"									Λ	•
DECX	Assembler converts this to "DEC $80"									Λ	•
DECY	Assembler converts this to "DEC $81"									Λ	•
INC			X	X			X			Λ	•
INCA	Assembler converts this to "INC $FF"									Λ	•
INCX	Assembler converts this to "INC $80"									Λ	•
INCY	Assembler converts this to "INC $81"									Λ	•
JMP								X		•	•
JSR								X		•	•
LDA		X	X	X			X			Λ	•
LDXI	Assembler converts this to "MVI DATA, $80"									•	•
LDYI	Assembler converts this to "MVI DATA, $81"									•	•
MVI		X	X							•	•
NOP	Assembler converts this to "BEQ (PC) + 1"									•	•
ROLA	X									Λ	Λ
RTI	X									Λ	Λ
RTS	X									•	•
STA			X	X			X			Λ	•
SUB		X	X				X			Λ	Λ
TAX	Assembler converts this to "STA $80"									Λ	•
TAY	Assembler converts this to "STA $81"									Λ	•
TXA	Assembler converts this to "LDA $80"									Λ	•
TYA	Assembler converts this to "LDA $81"									Λ	•

Flag Symbols: Z = Zero, C = Carry/Borrow, Λ = Test and Set if True, Cleared Otherwise, • = Not Affected

Table 6-7 . EF6804P2 Microcomputer

	Branch Instructions							
Hi / Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111
0 0000	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
1 0001	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
2 0010	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
3 0011	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
4 0100	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
5 0101	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
6 0110	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
7 0111	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
8 1000	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
9 1001	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
A 1010	2 BNE 1 REL	2 BNE 2 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
B 1011	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
C 1100	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
D 1101	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
E 1110	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
F 1111	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL

Abbreviations for Address Modes

INH	Inherent
S-D	Short Direct
B-T-B	Bit Test and Branch
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
R-IND	Register Indirect

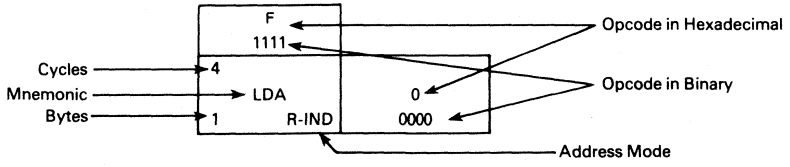
* Indicates Instruction Reserved for Future Use

\# Indicates Illegal Instruction

Instruction Set Opcode Map

Register/Memory, Control, and Read/Modify/Write Instructions				Bit Manipulation Instructions		Register/Memory and Read/Modify/Write		
8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Hi / Low
4 JSRn 2 EXT	4 JMPn 2 EXT	*	4 MVI 3 IMM	5 BRCLR0 3 B-T-B	4 BCLR0 2 BSC	4 LDA 1 R-IND	4 LDA 1 R-IND	0 0000
4 JSRn 2 EXT	4 JMPn 2 EXT	*	*	5 BRCLR1 3 B-T-B	4 BCLR1 2 BSC	4 STA 1 R-IND	4 STA 1 R-IND	1 0001
4 JSRn 2 EXT	4 JMPn 2 EXT	*	2 RTI 1 INH	5 BRCLR2 3 BT-B	4 BCLR2 2 BSC	4 ADD 1 R-IND	4 ADD 1 R-IND	2 0010
4 JSRn 2 EXT	4 JMPn 2 EXT	*	2 RTS 1 INH	5 BRCLR3 3 B-T-B	4 BCLR3 2 BSC	4 SUB 1 R-IND	4 SUB 1 R-IND	3 0011
4 JSRn 2 EXT	4 JMPn 2 EXT	*	4 COMA 1 INH	5 BRCLR4 3 B-T-B	4 BCLR4 2 BSC	4 CMP 1 R-IND	4 CMP 1 R-IND	4 0100
4 JSRn 2 EXT	4 JMPn 2 EXT	*	4 ROLA 1 INH	5 BRCLR5 3 B-T-B	4 BCLR5 2 BSC	4 AND 1 R-IND	4 AND 1 R-IND	5 0101
4 JSRn 2 EXT	4 JMPn 2 EXT	*	*	5 BRCLR6 3 B-T-B	4 BCLR6 2 BSC	4 INC 1 R-IND	4 INC 1 R-IND	6 0110
4 JSRn 2 EXT	4 JMPn 2 EXT	*	*	5 BRCLR7 3 B-T-B	4 BCLR7 2 BSC	4 DEC 1 R-IND	4 DEC 1 R-IND	7 0111
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 S-D	4 DEC 1 S-D	5 BRSET0 3 B-T-B	4 BSET0 2 BSC	4 LDA 2 IMM	4 LDA 2 DIR	8 1000
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 S-D	4 DEC 1 S-D	5 BRSET1 3 B-T-B	4 BSET1 2 BSC	#	4 STA 2 DIR	9 1001
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 S-D	4 DEC 1 S-D	5 BRSET2 3 B-T-B	4 BSET2 2 BSC	4 ADD 2 IMM	4 ADD 2 DIR	A 1010
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 S-D	4 DEC 1 S-D	5 BRSET3 3 B-T-B	4 BSET3 2 BSC	4 SUB 2 IMM	4 SUB 2 DIR	B 1011
4 JSRn 2 EXT	4 JMPn 2 EXT	4 LDA 1 S-D	4 STA 1 S-D	5 BRSET4 3 B-T-B	4 BSET4 2 BSC	4 CMP 2 IMM	4 CMP 2 DIR	C 1100
4 JSRn 2 EXT	4 JMPn 2 EXT	4 LDA 1 S-D	4 STA 1 S-D	5 BRSET5 3 B-T-B	4 BSET5 2 BSC	4 AND 2 IMM	4 AND 2 DIR	D 1101
4 JRSn 2 EXT	4 JMPn 2 EXT	4 LDA 1 S-D	4 STA 1 S-D	5 BRSET6 3 B-T-B	4 BSET6 2 BSC	#	4 INC 2 DIR	E 1110
4 JSRn 2 EXT	4 JMPn 2 EXT	4 LDA 1 S-D	4 STA 1 S-D	5 BRSET7 3 B-T-B	4 BSET7 2 BSC	#	4 DEC 2 DIR	F 1111

LEGEND



SECTION 7
ELECTRICAL SPECIFICATIONS

7.1 INTRODUCTION

This section contains the electrical specifications and associated timing for the EF6804P2

7.2 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	TL to TH	°C
Standard or L suffix		0 to 70	
V suffix		-40 to 85	
T suffix		-40 to 105	
Storage Temperature Range	T_{stg}	−55 to 150	°C
Junction Temperature Range	Tj		°C
Plastic		150	
PLCC		150	

This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$. Reliability of operation is enhanced if unused inputs except EXTAL are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

7.3 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance	θ JA		°C/W
Plastic		70	
PLCC		90	

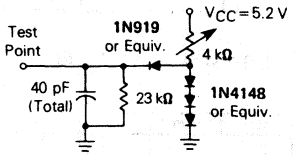


Figure 7-1. LSTTL Equivalent Test Load (Port B)

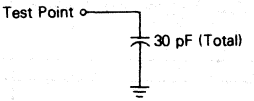


Figure 7-2. CMOS Equivalent Test Load (Ports A, B, C)

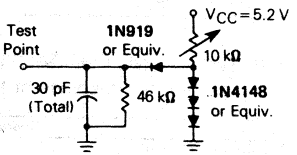


Figure 7-3. LSTTL Equivalent Test Load (Ports A, C, and TIMER)

7.4 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts – Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts – User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

7.5 ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc ± 0.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Power Dissipation – No Port Loading T_A = 0°C	P_{INT}	–	135	170	mV
T_A = -40°C		–	–	210	
Input High Voltage	V_{IH}	4.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Input Capacitance	C_{in}	–	10	–	pF
Input Current ($\overline{IRQ}$, $\overline{RESET}$)	I_{in}	–	2	20	µA

7.6 SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc ± 0.5 Vdc, V_{SS} = GND, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency	f_{OSC}	4.0	–	11.0	MHz
Bit Time	t_{bit}	0.364	–	1.0	µs
Byte Cycle Time	t_{byte}	4.36	–	12.0	µs
$\overline{IRQ}$ and TIMER Pulse Width	t_{WL}, t_{WH}	$2xt_{byte}$	–	–	–
$\overline{RESET}$ Pulse Width	t_{RWL}	$2xt_{byte}$	–	–	–
$\overline{RESET}$ Delay Time (External Capacitance = 1.0 µF)	t_{RHL}	100	–	–	ms

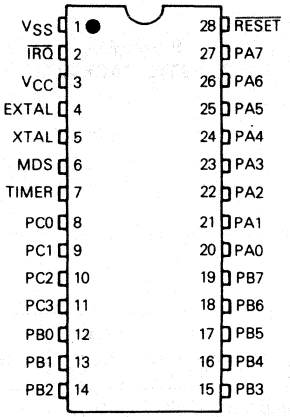
7.7 PORT DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc ± 0.5 Vdc, V_{SS} = GND, $T_A = T_L$ to T_H unless otherwise noted)

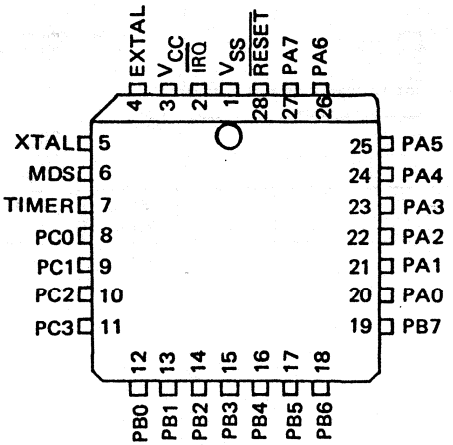
Characteristic	Symbol	Min	Typ	Max	Unit
Timer and Ports A and C (Standard)					
Output Low Voltage, I_{Load} = 0.4 mA	V_{OL}	–	–	0.5	V
Output High Voltage, I_{Load} = – 50 µA	V_{OH}	2.3	–	–	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	4	40	µA
Ports A and C (Open Drain)					
Output Low Voltage, I_{Load} = 0.4 mA	V_{OL}	–	–	0.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	4	40	µA
Open Drain Leakage ($V_{out} = V_{CC}$)	I_{LOD}	–	4	40	µA
Ports A and C (CMOS Drive)					
Output Low Voltage, I_{Load} = 0.4 mA (Sink)	V_{OL}	–	–	0.5	V
Output High Voltage, I_{Load} = – 10 µA	V_{OH}	V_{CC} – 1.0	–	–	V
Output High Voltage, I_{Load} = – **50 µA**	V_{OH}	2.3	–	–	V
Input High Voltage, I_{Load} = – 300 µA Max	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage, I_{Load} = – 300 µA Max	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current (V_{in} = 0.4 V to V_{CC})	I_{TSI}	–	–	– 300	µA
Port B (Standard)					
Output Low Voltage, I_{Load} = 1.0 mA	V_{OL}	–	–	0.5	V
Output Low Voltage, I_{Load} = 10 mA (Sink)	V_{OL}	–	–	1.5	V
Output High Voltage, I_{Load} = – 100 µA	V_{OH}	2.3	–	–	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	8	80	µA
Port B (Open Drain)					
Output Low Voltage, I_{Load} = 1.0 mA	V_{OL}	–	–	0.5	V
Output Low Voltage, I_{Load} = 10 mA (Sink)	V_{OL}	–	–	1.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	8	80	µA
Open Drain Leakage ($V_{out} = V_{CC}$)	I_{LOD}	–	8	80	µA
Port B (CMOS Drive)					
Output Low Voltage, I_{Load} = 1.0 mA	V_{OL}	–	–	0.5	V
Output High Voltage, I_{Load} = 10 mA (Sink)	V_{OL}	–	–	1.5	V
Output High Voltage, I_{Load} = – 10 µA	V_{OH}	V_{CC} – 1.0	–	–	V
Output High Voltage, I_{Load} = – **100 µA**	V_{OH}	2.3	–	–	V
Input High Voltage, I_{Load} = – 300 µA Max	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage, I_{Load} = – 300 µA Max	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current (V_{in} = 0.4 V to V_{CC})	I_{TSI}	–	–	– 300	µA

SECTION 8
MECHANICAL DATA

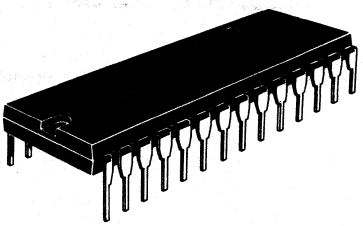
This section contains the pin assignment and package dimension diagrams for the EF6804P2 microcomputer.

8.1 PIN ASSIGNMENTS

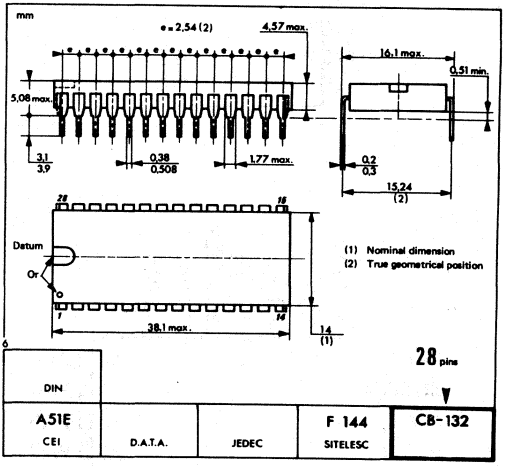




CASE CB-132

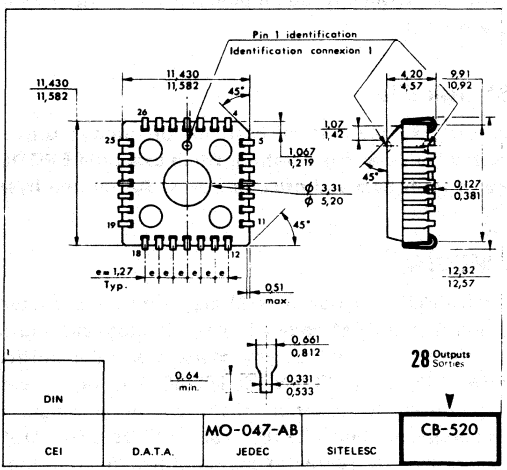


P SUFFIX
PLASTIC PACKAGE



CASE CB-520

FN SUFFIX
PLCC 28



SECTION 9
ORDERING INFORMATION

9.1 INTRODUCTION

The following information is required when ordering a custom MCU. The information may be transmitted to THOMSON SEMICONDUCTEURS in the following media:

EPROM(s), 2716 or 2732
EFDOS/MDOS* disk file

To initiate a ROM pattern for the MCU, it is necessary to first contact your local field service office, local sales person, or your local THOMSON SEMICONDUCTEURS representative.

9.1.1 EPROMs

One 2716 or one 2732 type EPROM, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. Since all program and data space information will fit on one 2716 EPROM, the EPROM must be programmed as follows in order to emulate the EF6804P2 MCU: **start the data space ROM at EPROM address $020 and start program space ROM at EPROM address $400 and continue to memory space $7FF. All unused bytes, including the user's space, must be set to zero, memory space $7F8 to $7FB is reserved for self-check vectors.** When using one 2732 EPROM, the memory map shown in Figure 2-1 can be used. For shipment to THOMSON SEMICONDUCTEURS the EPROMs should be placed in a conductive IC carrier and packed securely. Do not use styrofoam.

9.1.2 EFDOS/MDOS* Disk File

An EFDOS/MDOS* disk, programmed with the customer program (positive logic sense for address and data) may be submitted for pattern generation. **When using the EFDOS/MDOS* disk, include the entire memory image of both data and program space. All unused bytes, including the user's space, must be set to zero.**

9.2 VERIFICATION MEDIA

All original pattern media (EPROMs or floppy disk) are filed for contractual purposes and are not returned. A computer listing of the ROM code will be generated and returned along with a listing verification form. The listing should be thoroughly checked and the verification form completed, signed, and returned to THOMSON SEMICONDUCTEURS. The signed verification form constitutes the contractural agreement for creation of the customer mask. If desired, THOMSON SEMICONDUCTEURS will program a blank 2716, 2732, or EFDOS/MDOS* disk **(supplied by the customer)** from the data file used to create the custom mask to aid in the verification process.

* Requires prior factory approval

9.3 ROM VERIFICATION UNITS (RVUs)

Ten MCUs containing the customer's ROM pattern will be sent for program verification. These units will have been made using the custom mask but are for the purpose of ROM verification only. For expediency they are usually unmarked, packaged in ceramic, and tested only at room temperature and five volts. These RVUs are included in the mask charge and are not production parts. These RVUs are not backed nor guaranteed by THOMSON SEMICONDUCTEURS Quality Assurance.

9.4 FLEXIBLE DISKS

The disk media submitted must be single-sided, single density, 8-inch, EFDOS/MDOS* compatible floppies. The customer must clearly label the disk with the ROM pattern file name. The minimum EFDOS/MDOS* system files as well as the absolute binary object file (file name. LO type of file) from the 6804 cross-assembler must be on the disk. An object file made from a memory dump, using the ROLLOUT command is also admissable. Consider submitting a source listing as well as: file name, .LX (DEVICE/EXORciser loadable format). This file will of course be kept confidential and is used 1) to speed up the process in house if any problems arises, and 2) to speed up our customer to factory interface if an user finds any software errors and needs assistance quickly from THOMSON SEMICONDUCTEURS factory representatives.

MDOS* (fully compatible with EFDOS) is Motorola's Disk Operating System available on development systems Such as EXORcisers, EXORsets, etc.

EFDOS is THOMSON SEMICONDUCTEURS Disk Operating System available on development systems such as DEVICE/EXOR...

Whenever ordering a custom MCU is required, please contact your local THOMSON-SEMICONDUCTEURS representative or THOMSON-SEMICONDUCTEURS distributor and/or complete and send the attached "MCU customer ordering sheet" to your local THOMSON-SEMICONDUCTEURS representative.

* Requires prior factory approval

ORDERING INFORMATION

EF6804P2 | P | V | ____

- EF6804P2: Device
- P: Package
- V: Oper. temp.
- ____: Screening level

The table below horizontally shows all available suffix combinations for package, operating temperature and screening level. Other possibilities on request.

DEVICE	PACKAGE					OPER. TEMP			SCREENING LEVEL			
	C	J	P	E	FN	L*	V	T	Std	D		
EF6804P2			●		●	●	●		●	●		

Examples : EF6804P2P, EF6804P2FN, EF6804P2PV, EF6804P2FNV.

Package : C : Ceramic DIL, **P** : Plastic DIL, **FN** : PLCC.
Oper. temp. : L* : 0°C to +70°C, **V** : -40°C to +85°C, **T** : -40°C to +105°C, * : may be omitted.
Screening level : Std : (no-end suffix), **D** : NFC 96883 level D.

EXORciser is a registered trademark to Motorola Inc.

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

EF6804 FAMILY — MCU CUSTOMER ORDERING SHEET

Commercial reference : E F 6 8 0 4 P 2 _ _ _

Customer's marking : _ _ _ _ _ _ _ _ _ _ _
11 characters max.

Application : .....
.....

ROM capacity required : _ _ _ _ bytes

Temperature range :
☐ 0°C/+70°C
☐ −40°C/+85°C
☐ −40°C/+105°C

Package :
☐ Plastic
☐ PLCC

Customer name : .....
Company : .....
Address : .....
Phone : .....

Specification reference :
☐ THOMSON SEMICONDUCTEURS reference .....
☐ Special customer data reference* .....

Number of interrupt vector : _ _

Quality level :
☐ STD
☐ D
☐ Other* (customer's quality specification ref.) :
.....

Software developed by :
☐ THOMSON SEMICONDUCTEURS application lab.
☐ External lab.
☐ Customer

PATTERN MEDIA (a listing may be supplied in addition for checking purposes) :

☐ EPROM Reference :

☐ EFDOS/MDOS* disk file (DEVICE/EXORciser)
☐ 8" floppy
☐ 5" 1/4 floppy

☐ Other*

OPTION LIST :
— Oscillator input :
☐ Xtal
☐ RC

— Interrupt Trigger
☐ Edge-sensitive
☐ Level-and edge-sensitive

— Port A output drive (4 I/Os)
☐ CMOS and TTL
☐ TTL only
☐ Open drain

— Port B output drive
☐ CMOS and TTL
☐ TTL only
☐ Open drain

— Port C output drive
☐ CMOS and TTL
☐ TTL only
☐ Open drain

* Requires prior factory approval

Yearly quantity forecast :

- start of production date :
- for a shipment period of :

CUSTOMER CONTACT NAME : DATE : SIGNATURE :

THOMSON SEMICONDUCTEURS
43 - 45, Avenue de l'Europe 78140 VELIZY-FRANCE Tel. (1) 39.46.97.19 Telex : 240780F

THOMSON COMPONENTS SEMICONDUCTEURS

TS68HC04J3

8-BIT MICROCOMPUTER

PRODUCT PREVIEW

The TS68HC04J3 microcomputer unit (MCU) is a member of the 68HC04 family of very low cost and low power single chip microcomputers. This 8 bit microcomputer contains a CPU, on-chip clock, ROM, RAM, I/O, and timer. It is designed for the user who needs an economical microcomputer with the proven capabilities of the 6800 based instruction set. The following are some of the hardware and software highlights of the TS68HC 04J3 MCU.

HARDWARE FEATURES

- Low power HCMOS
- Power saving stop and wait modes
- Single 2.0 to 6.0 volt power supply
- 8-bit architecture
- Fully static operation
- Pin compatible with 6804J2
- 124 bytes of on-chip RAM with standby mode
- 2 Kbytes of program ROM including 356 bytes for self-check program
- 72 bytes of user data ROM for look-up tables
- 12 TTL/CMOS compatible bidirectional I/O lines
- On-chip clock generator
- Extensive self-check capability allowing complete functional test of the chip (including ROM content)
- Master RESET and power-on-reset
- 8-bit timer with software programmable 7-bit prescaler
- TIMER pin programmable as input or output
- Complete development system support on DEVICE®.

SOFTWARE FEATURES

- Similar to 6800 family
- Byte efficient instruction set
- Easy to program
- True bit manipulation
- Stop, Wait and bit manipulation instructions
- Bit test and branch instructions
- Versatile interrupt handling
- Separate flags for normal and interrupt processing
- True LIFO 4-level stack eliminating stack pointer
- Maskable timer interrupt
- Versatile indirect registers
- Conditional branches
- Single instruction memory examine/change
- 9 powerful addressing modes.

USER SELECTABLE OPTIONS

- Crystal or low-cost resistor oscillator option
- Mask selectable internal clock generator options
- Mask selectable edge or level sensitive interrupt pin
- Program ROM protection option
- Optional pull-down devices on I/O lines.

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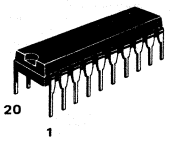
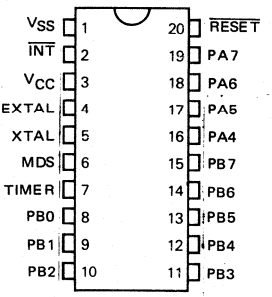
8-BIT MICROCOMPUTER

CASE CB-194



P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT



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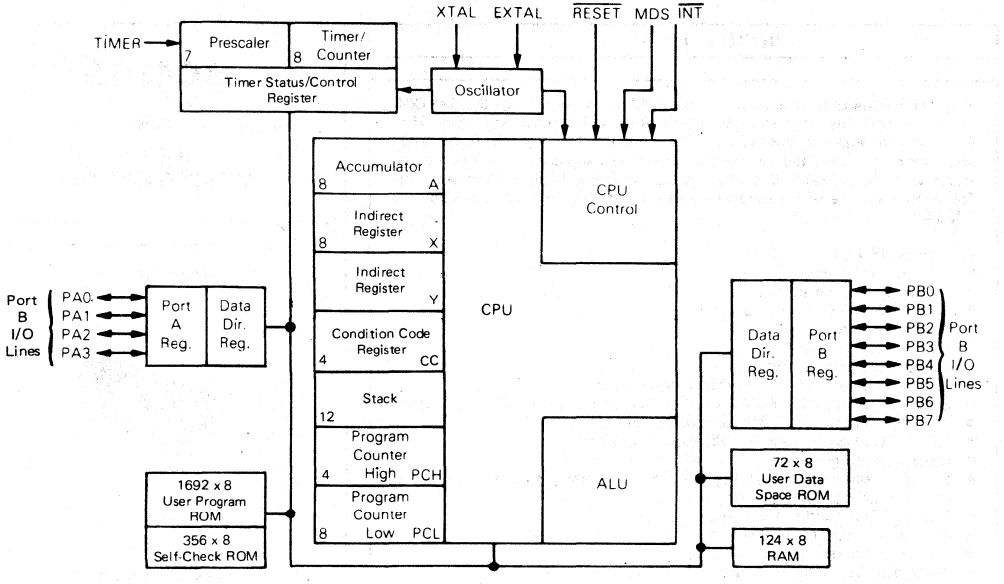

NOTE : 8-Bit Indirect Registers X and Y, although shown as part of the CPU are actually located in the 124 x 8 RAM at locations $80 and $81.

TS68HC04J3 MCU BLOCK DIAGRAM

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THOMSON COMPONENTS SEMICONDUCTEURS

EF68HC04P3

8-BIT HCMOS MICROCOMPUTER UNIT

ADVANCE INFORMATION

The EF68HC04P3 microcomputer unit (MCU) is a member of the EF68HC 04 family of very low cost and low power single chip microcomputers. This 8 bit microcomputer contains a CPU, on-chip clock, ROM, RAM, I/O, and timer. It is designed for the user who needs an economical microcomputer with the proven capabilities of the EF6800 based instruction set. The following are some of the hardware and software highlights of the EF68HC04P3 MCU.

HARDWARE FEATURES

- Low power HCMOS
- Power saving stop and wait modes
- Single 2.0 to 6.0 volt power supply
- 8-bit architecture
- Fully static operation
- Pin compatible with the EF6805P2 and EF6804P2
- 124 bytes of on-chip RAM with standby mode
- 2 Kbytes of program ROM including 356 bytes for self-check program
- 72 bytes of user data ROM for look-up tables
- 20 open-collector TTL/CMOS compatible bidirectional I/O lines
- On-chip clock generator
- Extensive self-check capability allowing complete functional test of the chip (including ROM content)
- Master RESET and power-on-reset
- 8-bit timer with 7-bit software programmable prescaler
- TIMER pin programmable as input or output
- Complete development system support on DEVICE®.

SOFTWARE FEATURES

- Similar to EF6800 family
- Byte efficient instruction set
- Easy to program
- True bit manipulation
- Stop, Wait and bit manipulation instructions
- Bit test and branch instructions
- Versatile interrupt handling
- Separate flags for normal and interrupt processing
- True LIFO 4-level stack eliminating stack pointer
- Maskable timer interrupt
- Versatile indirect registers
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- Single instruction memory examine/change
- 9 powerful addressing modes.

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- Mask selectable internal clock generator options
- Mask selectable edge or level sensitive interrupt pin
- Program ROM protection option
- Optional pull-down devices on I/O lines.

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HCMOS

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8-BIT MICROCOMPUTER

CASES

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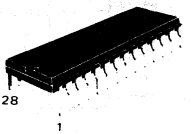

P SUFFIX
PLASTIC PACKAGE

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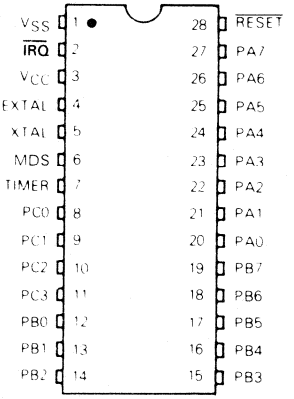
FN SUFFIX
PLCC 28

PIN ASSIGNMENT



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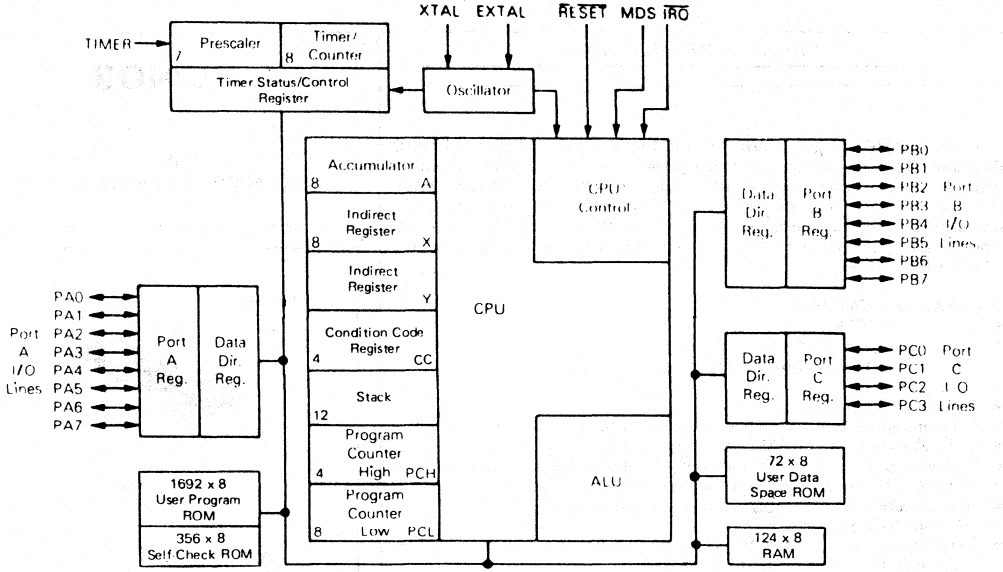

NOTE : 8-Bit Indirect Registers X and Y, although shown as part of the CPU are actually located in the 124 x 8 RAM at locations $80 and $81.

Figure 1-1. EF68HC04P3 MCU Block Diagram

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SECTION 2
FUNCTIONAL PIN DESCRIPTION, MEMORY, CPU, AND REGISTERS

This section provides a description of the functional pins, memory spaces, the central processing unit (CPU), and the various registers and flags.

2.1 FUNCTIONAL PIN DESCRIPTION

2.1.1 V_{CC} and V_{SS}

Power is supplied to the MCU using these two pins. V_{CC} is power and V_{SS} is the ground connection.

2.1.2 $\overline{IRQ}$

This pin provides the capability for asynchronously applying an external interrupt to the MCU. Refer to **4.1 INTERRUPT** for additional information.

2.1.3 XTAL and EXTAL

These pins provide connections to the on-chip clock oscillator circuit. A crystal, a resistor and capacitor, or an external signal, depending on the user selectable manufacturing mask option, can be connected to these pins to provide a system clock source with various stability/cost tradeoffs. Lead lengths and stray capacitance on these two pins should be minimized. Refer to **4.4 INTERNAL CLOCK GENERATOR OPTIONS** for recommendations concerning these inputs.

2.1.4 TIMER

In the input mode, the timer pin is connected to the prescaler input and serves as the timer clock or as an enable input for the internal clock. In the output mode, the timer pin signals that a time out of the timer has occurred. Refer to **SECTION 3 TIMER** for additional information.

2.1.5 $\overline{RESET}$

The $\overline{RESET}$ pin is used to restart the processor of the EF68HC04P3 to the beginning of a program. This pin, together with the MDS pin is also used to select the operating mode of the EF68HC04P3. If the MDS pin is at zero volts, the normal mode is selected and the program counter is loaded with the user restart vector. However, if the MDS pin is at +5 volts, then pins PA6 and PA7 are decoded to allow selection of the operating mode. Refer to **4.3 RESET** for additional information.

2.1.6 MDS

The MDS (mode select) pin is used to place the MCU into special operating modes. If MDS is held at +5 volts at the exit of the reset state, the decoded state of PA6 and PA7 is latched to determine the operating mode (single-chip, self-check, or ROM verify). However, if MDS is held at zero volts at the exit of the reset state, the single-chip operating mode is automatically selected (regardless of PA6 and PA7 state).

For those users familiar with the EF6801 microcomputer, mode selection is similar but much less complex in the EF68HC04P3. No special external diodes, switches, transistors, etc. are required in the EF68HC04P3.

2.1.7 Port Input/Output Lines (PA0-PA7, PB0-PB7, PC0-PC3)

These 20 lines are arranged into two 8-bit ports (A and B) and one 4-bit port (C). All lines are programmable as either inputs or outputs under software control of the data direction registers. Refer to **SECTION 5 INPUT/OUTPUT PORTS** for additional information.

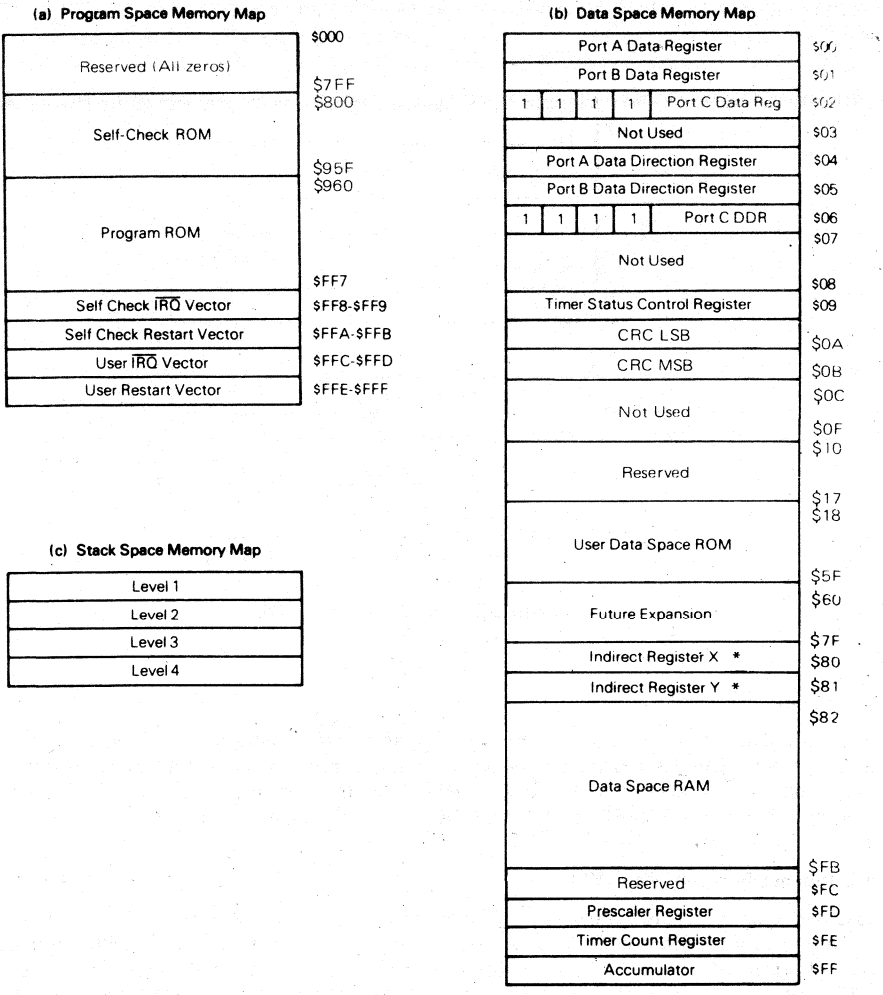
2.2 MEMORY

The MCU operates in three different memory spaces: program space, data space, and stack space. A representation of these memory spaces is shown in Figure 2-1. The program space (Figure 2-1a) contains all of the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, and the self-check and user vectors. The data space (Figure 2-1b) contains all of the RAM locations, plus I/O locations and some ROM used for storage of tables and constants. The stack space (Figure 2-1c) contains RAM which is used for stacking subroutine and interrupt return addresses.

The MCU is capable of addressing 4096 bytes of program space memory with its program counter and 256 bytes of data space memory with its instructions. The data space memory contains three bytes for port data registers, three bytes for port data direction registers, one byte for timer status/control, 72 bytes ROM, 124 bytes RAM (which includes two bytes for XP and YP indirect registers), two bytes for timer prescaler and count registers, and one byte for the accumulator. The program space section contains 2048 bytes of ROM including 356 bytes of self-check ROM and 8 bytes of vectors for self-check and user programs.

2.3 CENTRAL PROCESSING UNIT

The CPU of the EF68HC04 Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control buses.



* $80, $81, $82, $83 are used for short direct addressing.

Figure 2-1. EF68HC04P3 MCU Address Map

2.4 REGISTERS

The EF68HC04 Family CPU has four registers and two flags available to the programmer. They are shown in Figure 2-2 and are explained in the following paragraphs.

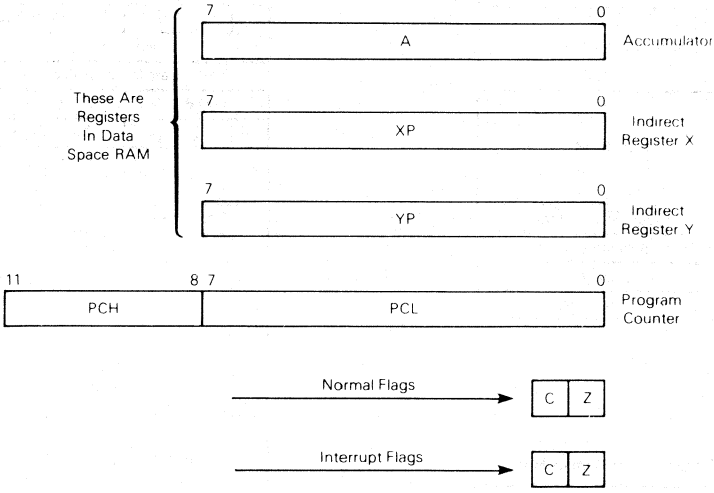


Figure 2-2. Programming Model

2.4.1 Accumulator (A)

The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator is implemented as the highest RAM location ($FF) in data space and thus implies that several instructions exist which are not explicitly implemented. Refer to **6.3 IMPLIED INSTRUCTIONS** for additional information.

2.4.2 Indirect Registers (XP, YP)

These two indirect registers are used to maintain pointers to other memory locations in data space. They are used in the register-indirect addressing mode, and can be accessed with the direct, indirect, short direct, or bit set/clear addressing modes. These registers are implemented as two of the 124 RAM locations ($80, $81) and as such generate implied instructions and may be manipulated in a manner similar to any RAM memory location in data space. Refer to **6.3 IMPLIED INSTRUCTIONS** for additional information.

2.4.3 Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next ROM word to be used (may be opcode, operand, or address of operand). The 12-bit program counter is contained in PCL (low byte) and PCH (high nibble).

2.4.4 Flags (C, Z)

The carry (C) bit is set on a carry or a borrow out of the ALU. It is cleared if the result of an arithmetic operation does not result in a carry or a borrow. The (C) bit is also set to the value of the bit tested in a bit test instruction, and participates in the rotate left instruction.

The zero (Z) bit is set if the result of the last arithmetic or logical operation was equal to zero, otherwise it is cleared.

There are two sets of these flags, one set is for interrupt processing, the other for all other routines. When an interrupt occurs, a context switch is made from the program flags to the interrupt flags (interrupt mode). An RTI forces the context switch back to the program flags (program mode). While in either mode, only the flags for that mode are available. Further, the interrupt flags will not be cleared upon entering the interrupt mode. Instead, the flags will be as they were at the exit of the last interrupt mode. Both sets of flags are cleared by reset.

2.4.5 Stack

There is a true LIFO stack incorporated in the EF68HC04P3 which eliminates the need for a stack pointer. Stack space is implemented in separate RAM (12-bits wide) shown in Figure 2-1c. Whenever a subroutine call (or interrupt) occurs, the contents of the PC are shifted into the top register of the stack. At the same time (same cycle), the top register is shifted to the next level deeper. This happens to all registers with the bottom register falling out the bottom of the stack.

Whenever a subroutine or interrupt return occurs, the top register is shifted into the PC and all lower registers are shifted up one level higher. Stack level 4 is loaded with the previous content of stack level 3. The stack RAM is four levels deep.

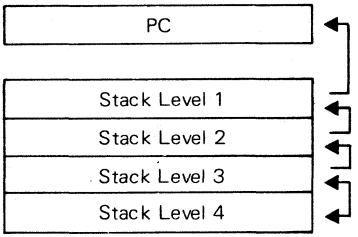


Figure 2-3. Stack Operation when RTS or RTI occurs

SECTION 3
TIMER

3.1 INTRODUCTION

A block diagram of the EF68HC04P3 timer circuitry is shown in Figure 3-1. The timer logic in the MCU is comprised of a simple 8-bit counter (timer count register, TCR) with a 7-bit prescaler, and a timer status/control register (TSCR). The timer count register, which may be loaded under program control is decremented towards zero by a clock input (prescaler output). The prescaler is used to extend the maximum interval of the overall timer. The prescaler tap is selected by bits 0-2 (PS0-PS2) of the timer status/control register. Bits PS0-PS2 control the actual division of the prescaler within the range of divide-by-1 (2^0) to divide-by-128 (2^7). The timer count register (TCR) and prescaler are decremented on rising clock edges. The coding of the TCSR PS0-PS2 bits produces a division in the prescaler as shown in Table 3-1.

Table 3-1. Prescaler Coding Table

PS2	PS1	PS0	Divide By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8

PS2	PS1	PS0	Divide By
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

TIMER pin may be programmed as either an output or an input depending on the status of DOUT and TOUT bits. Three modes are available.

Output mode (TOUT = 1)
The TIMER pin is connected to the DOUT latch. Therefore, the timer prescaler is clocked by the internal SYNC pulse. (Divide-by-12, -24 or -48 of the internal oscillator according to selected mask option, refer to 4.4 INTERNAL CLOCK GENERATOR OPTIONS). The prescaler then divides its clock input by a value determined by the coding of the TSCR bits PS0 - PS2 as shown in table 3-1. The divided prescaler output then clocks the 8-bit timer count register (TCR). When the TCR count reaches zero, it sets the TMZ bit in the TSCR. The TMZ bit can be tested under program control to perform a timer function whenever it goes high. The low-to-high TMZ bit transition is used to latch the DOUT bit of the TSCR and provides it for the TIMER pin.

Controlled mode (TOUT = 0, DOUT = 1)
The TIMER pin is an input which controls the counting by the prescaler-timer. When high, it enables counting Counting is disabled as long as this input remains low. Operation is similar to that described for the output mode.

Clock input mode (TOUT = 0 DOUT = 0)
The TIMER pin is connected directly to the prescaler input. Therefore the timer prescaler is clocked by the signal applied from the TIMER pin. Operation is similar to that described for the output mode. The frequency of the signal applied to the TIMER pin must be less than $1/t_{byte}$ ($f_{osc} \div 12$, $\div 24$ or $\div 48$ according to selected mask option) because of internal synchronization.

NOTE

TMZ is normally set to logic one when the timer times out (TCR count reaches $00) ; however, it may be set by a write of $00 to the TCR or by a write to bit 7 of the TSCR.

- TMZ bit is cleared by a read-only of the TSCR even if TMZ bit is not concerned by this read.

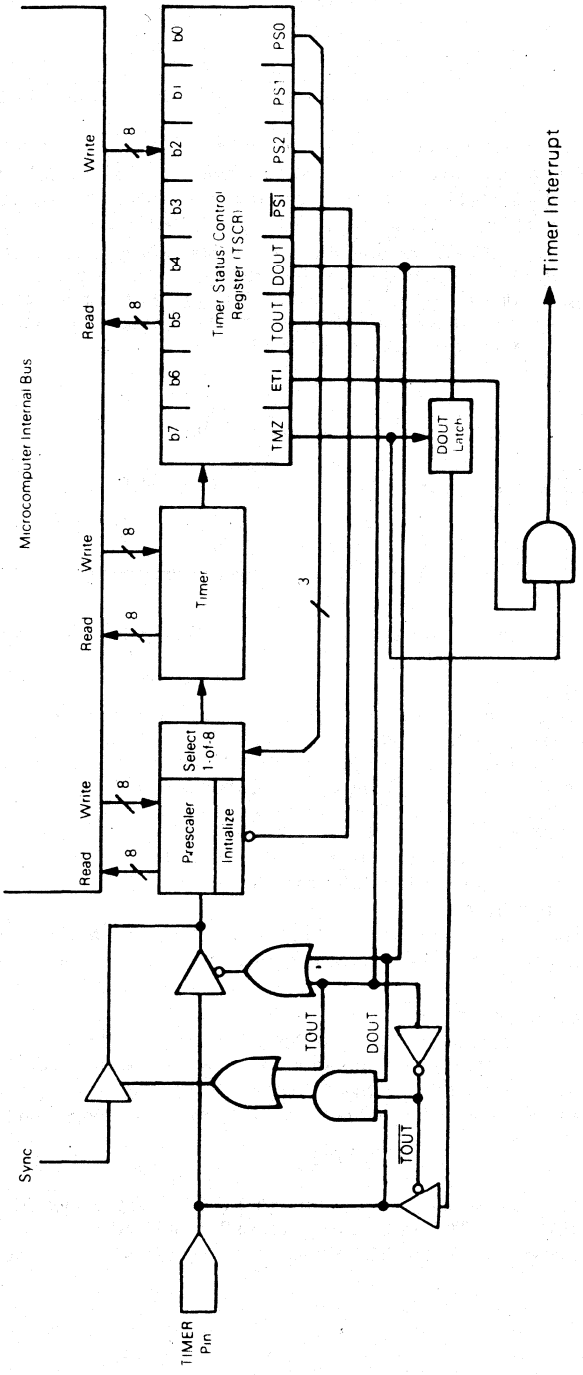
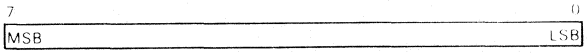


Figure 3-1. Timer Block Diagram

During reset, the timer count register and prescaler are set to $FF, while the timer status/control register is cleared to $00 and the DOUT LATCH (TIMER pin is in the high-impedance input mode) is forced to a logic high. The prescaler and timer count register are implemented in data space RAM locations ($FD, $FE); therefore, they are both readable and writeable. A write to either will predominate over the TCR decrement-to-$00 function; i.e., if a write and a TCR decrement-to-$00 occur simultaneously, the write will take precedence, and the TMZ bit is not set until the next timer time out.

3.2 TIMER REGISTERS

3.2.1 Timer Count Register (TCR)



TCR Address = $FE

The timer count register indicates the state of the internal 8-bit counter.

3.2.2 Timer Status/Control Register (TSCR)

7	6	5	4	3	2	1	0
TMZ	ETI	TOUT	DOUT	$\overline{PSI}$	PS2	PS1	PS0

TSCR Address = $09

b7, TMZ — Low-to-high transition indicates the timer count register has decremented to zero since the timer status/control register was last read. Cleared by a read of TSCR register if TMZ was read as a logic one.

b6, ETI — This bit, when set, enables the timer interrupt.

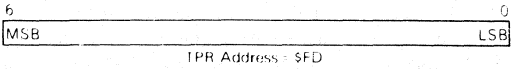
b5, TOUT — When low, this bit selects the input modes for the timer. When high, the output mode is selected.

b4, DOUT — Data sent to the timer output pin when TMZ is set high (output mode only). Choice of input mode (input mode only).

b3, $\overline{PSI}$ — Used to initialize the prescaler and inhibit its counting while $\overline{PSI} = 0$. The initialized value is set to $FF. The timer count register will also be inhibited (contents unchanged). When $\overline{PSI} = 1$ the prescaler begins to count downward.

b0, b1, b2 PS0-PS1-PS2 — These bits are used to select the prescaler divide-by ratio; therefore, effecting the clock input frequency to the timer count register.

3.2.3 Timer Prescaler Register



The timer prescaler register indicates the state of the internal 7-bit prescaler. This 7-bit prescaler divide ratio is normally determined by bits PS0-PS2 of the timer status/control register (see Table 3.1).

SECTION 4
INTERRUPT, SELF-CHECK, RESET, AND INTERNAL CLOCK GENERATOR

4.1 INTERRUPT

The EF68HC04P3 can be interrupted by applying a logic low signal to the $\overline{IRQ}$ pin ; however, a mask option selected at the time of manufacture determines whether the negative-going edge or the actual low level is sensed to indicate an interrupt. The EF68HC04P3 can also be interrupted by the timer if ETI bit in TCSR register is set.

4.1.1 Edge-Sensitive Option

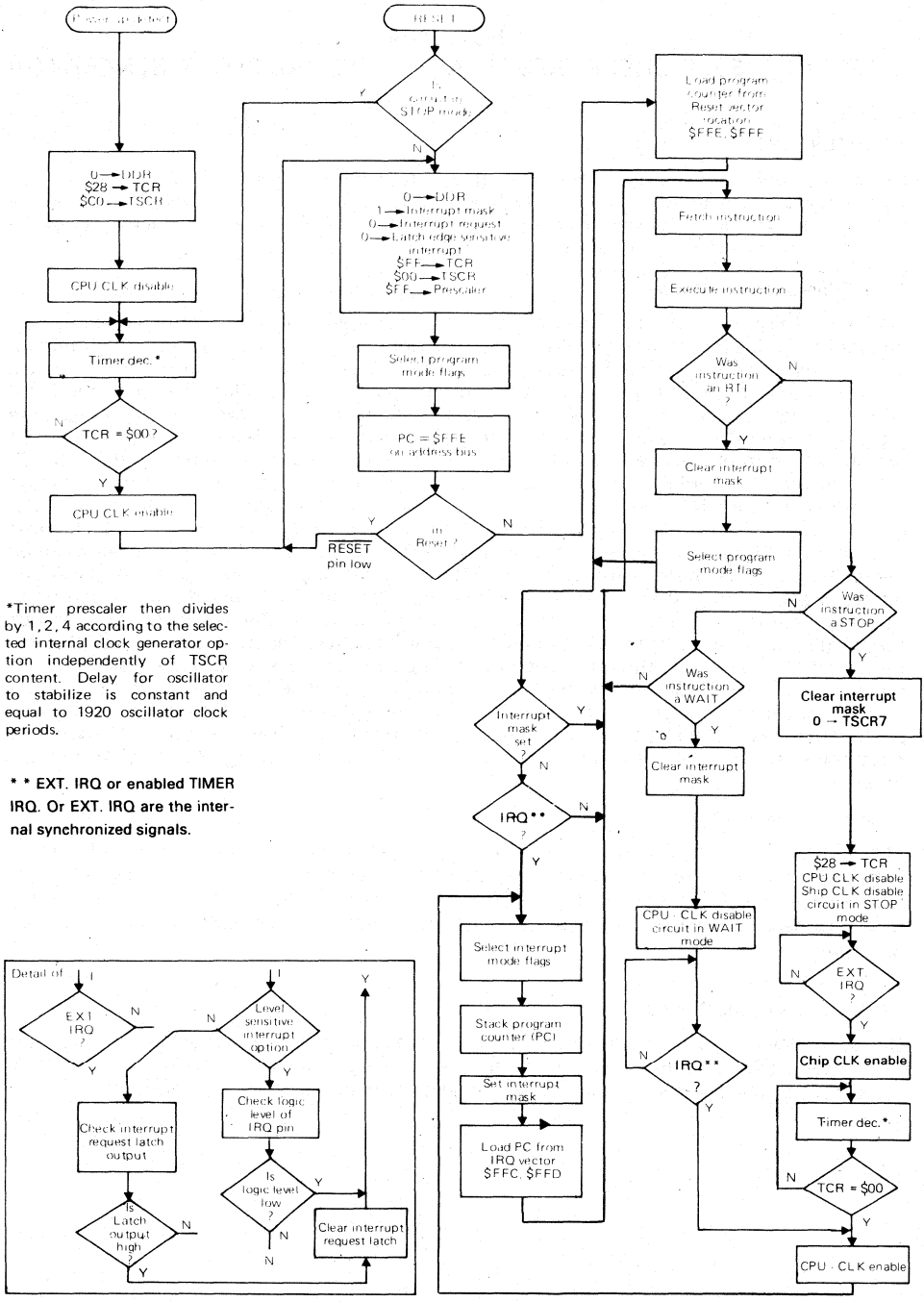
When the $\overline{IRQ}$ pin is pulled low, the internal interrupt request latch is set after a maximum of 3 machine cycles for internal synchronization. Prior to each instruction fetch, the interrupt latch is tested and, if its output is high, an interrupt sequence is initiated (provided the interrupt mask is cleared). Figure 4-1 contains a flowchart which illustrates both the reset and interrupt sequence. The interrupt sequence consists of one cycle during which the interrupt request latch is cleared, the interrupt mode flags are selected, the PC is saved on the stack, the interrupt mask is set, and the $\overline{IRQ}$ vector (single chip mode = $FFC/$FFD, self-check mode = $FF8/$FF9) is loaded into the PC. Internal processing of the interrupt continues until an RTI (return from interrupt) instruction is processed. During the RTI instruction, the interrupt mask is cleared and the program mode flags are selected. The next instruction of the program is then fetched and executed unless the $\overline{IRQ}$ pin has been pulled low at least 3 cycles before the end of the RTI instruction (see above). In this case, another interrupt sequence is initiated. Once the interrupt was initially detected and the interrupt sequence started, the interrupt request latch is cleared so that the next (second) interrupt may be detected even while the previous (first) one is being serviced. However, even though the second interrupt sets the interrupt request latch during processing of the first interrupt, the second interrupt sequence will not be initiated until completion of the interrupt service routine for the first interrupt. Completion of an interrupt service routine is always accomplished using an RTI instruction to return to the main program. The interrupt mask (which is not directly available to the programmer) is cleared during the last cycle of the RTI instruction.

4.1.2 Level-Sensitive Option

The actual operation of the level-sensitive and edge-sensitive options are similar except that the level-sensitive option does not have an interrupt request latch. With no interrupt request latch, the logic level of the $\overline{IRQ}$ pin is checked for detection of the interrupt. Also, in the interrupt sequence, there is no need to clear the interrupt request latch. These differences are illustrated in the flowchart of Figure 4-1.

4.1.3 Power Up and Timing

During the power-up sequence the interrupt mask is set to preclude any false or "ghost" interrupts from occurring. To clear the interrupt mask, the programmer should write a JSR (instead of a JMP) instruction to an initialization routine as the first instruction in a program. The initialization routine



*Timer prescaler then divides by 1, 2, 4 according to the selected internal clock generator option independently of TSCR content. Delay for oscillator to stabilize is constant and equal to 1920 oscillator clock periods.

*** * EXT. IRQ or enabled TIMER IRQ. Or EXT. IRQ are the internal synchronized signals.**

Figure 4-1. STOP, WAIT, INTERRUPT and RESET processing flowchart

should end with an RTI (instead of RTS) or with a STOP or WAIT instruction which clears the interrupt mask. Maximum interrupt response time is eight machine (t_{byte}) cycles (see **4.4 INTERNAL CLOCK GENERATOR OPTIONS).** This includes five machine cycles for the longest instruction, plus one machine cycle for stacking the PC and switching flags and plus two machine cycles for synchronization of the $\overline{IRQ}$ input with internal machine cycles. Minimum response time is four machine cycles for internal synchronization (3 cycles) and for stacking PC and switching flags (see **2.4.4 Flags (C, Z)**).

4.2 SELF-CHECK

The self-check capability of the EF68HC04P3 MCU provides an internal check to determine if the part a functional check of the MCU, connect it as shown in Figure 4-2a and monitor the LEDs for a 00100 ($04) pattern on port A. The MCU is left in the WAIT mode. A logical low signal applied to the $\overline{IRQ}$ pin places the MCU in the STOP mode. A 00101 ($05) pattern appears on port A. Another logical low signal applied on the $\overline{IRQ}$ pin enables exit from the STOP mode. The "final good" pattern (00110 - $06) appears on port A). To initiate a ROM self-check of the memory simply connect the circuit as shown in Figure 4-2b and check that the "good" LED turns on to indicate a good memory. The ROM verify uses a cyclical redundancy check (CRC) to conduct a ROM check by means of signature analysis circuit. This circuit consists of two 8-bit shift registers configured to perform the check using the CCITT polynominal. A manufacturing mask option inhibits the outputs of the CRC data and the ROM data until the final result is available in order to protect the program ROM when the option is selected.

4.3 RESET

The MCU can be reset in two ways: by the external reset input ($\overline{RESET}$) and by power-up detect (PUD).

4.3.1. $\overline{RESET}$ input

This input can be used to reset the MCU internal state and provides an orderly software start-up procedure.

4.3.2 PUD

It occurs when a positive transition is detected on V_{CC} on initial power-up. No external RC network is needed. PUD is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. There is no provision in this block for power-down detect. When the MCU is reset by means of PUD, an internal delay of 1920 oscillator clock periods is generated for the oscillator to stabilize. The MCU emerges from the reset condition at the end of this temporization.

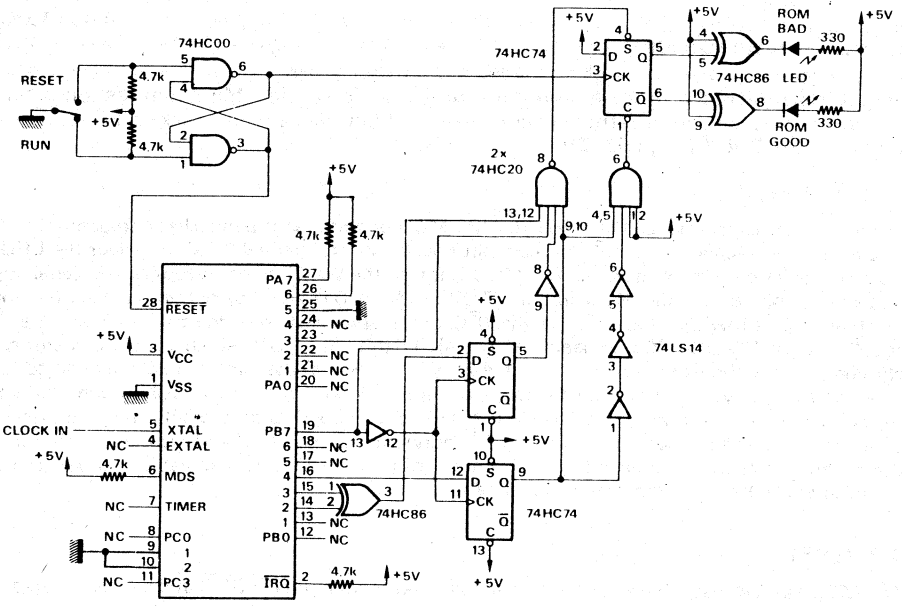


Figure 4-2. ROM Verify Circuit

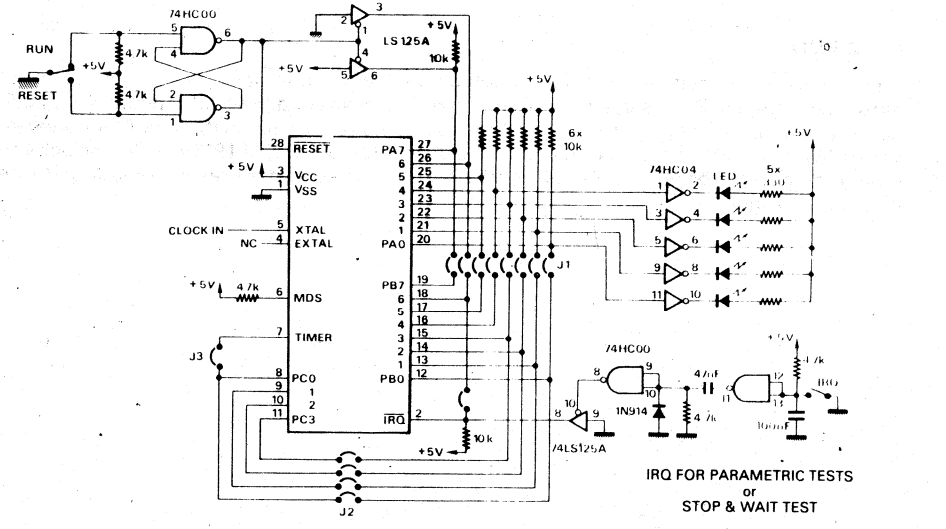


Figure 4-3. Self-Check Circuit

(Beware of $\overline{IRQ}$ pulse width when using level - Sensitive option - 10 machine cycles max. length).

4.4 INTERNAL CLOCK GENERATOR OPTIONS

The internal clock generator circuit is designed to require a minimum of external components. A crystal, a resistor-capacitor, or an external signal may be used to generate a system clock with various stability/cost tradeoffs. A manufacturing mask option is required to select either the crystal oscillator or the RC oscillator circuit. The different clock generator option connection methods are shown in Figure 4-4, crystal specifications and suggested PC board layouts are given in Figure 4 5, resistor-capacitor selection graph is given in Figure 4-6, and a timing diagram is illustrated in Figure 4-7. The crystal oscillator startup time is a function of many variables: crystal parameters (especially R_S), oscillator load capacitance (C_L), IC parameters, ambient temperature, and supply voltage. To ensure rapid oscillator startup, neither the crystal characteristics nor the load capacitance should exceed recommendations.

The oscillator output frequency is internally divided by four, two or one depending upon a manufacturing mask option selection to produce the internal $\phi 1$ and $\phi 2$ clocks. The $\phi 1$ clock is divided by twelve to produce a machine byte (cycle) clock (internal SYNC pulse). A byte cycle is the smallest unit needed to execute any operation (i.e., increment the program counter). An instruction may need two, four, or five byte cycles to be executed.

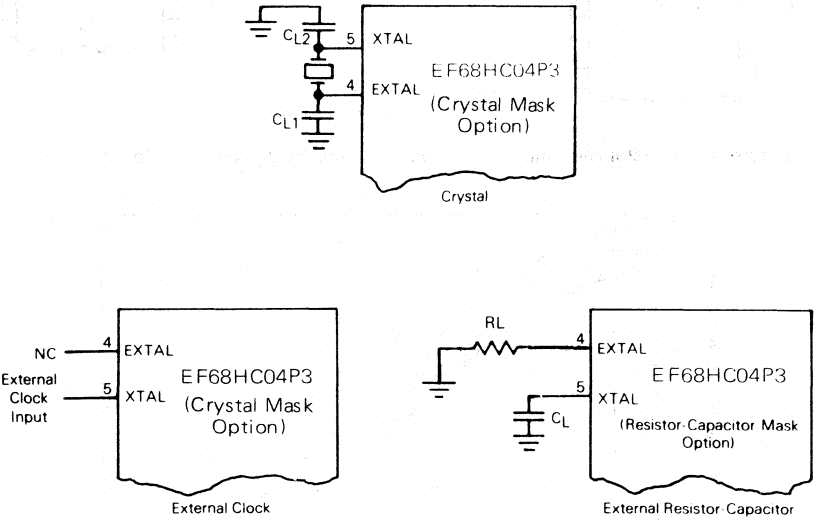


Figure 4-4. Clock Generator Options

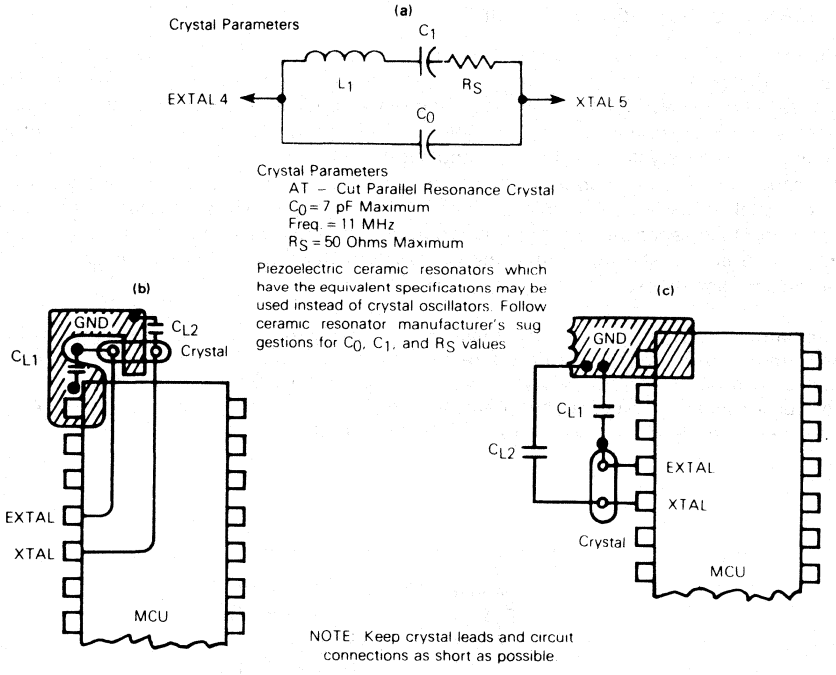


Figure 4-5. Crystal Motional Arm Parameters and Suggested PC Board Layout

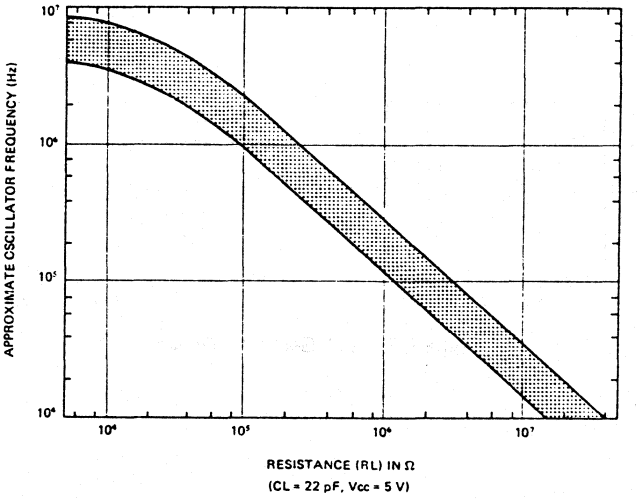
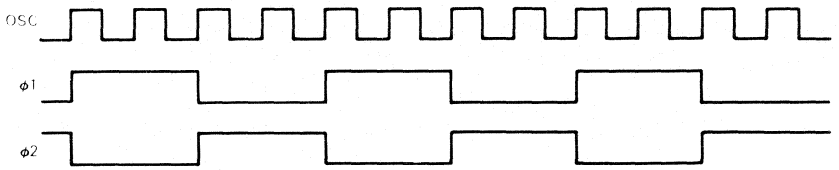


Figure 4-6. Typical Frequency Selection For Resistor-Capacitor Oscillator Option

(a) Oscillator – $\phi 1$ - $\phi 2$ Timing (divide-by-four option)



(b) $\phi 1$ – Sync Timing

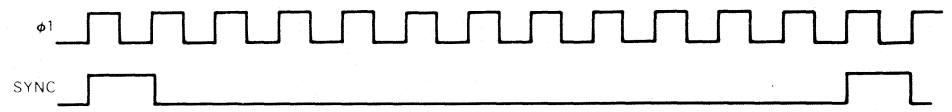


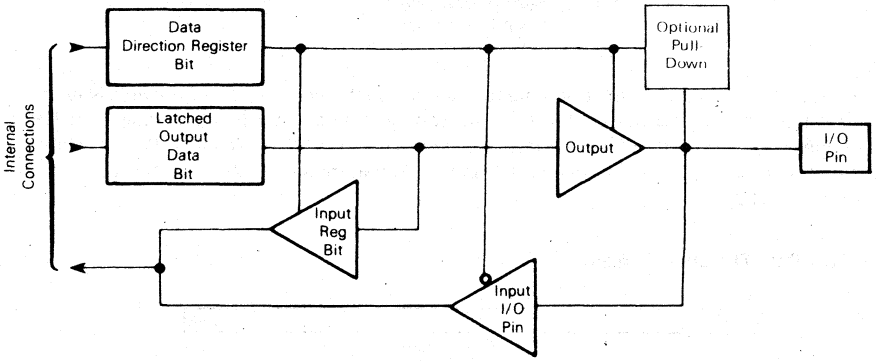
Figure 4-7. Clock Generator Timing Diagram

SECTION 5
INPUT/OUTPUT PORTS

5.1 INPUT/OUTPUT

There are 20 input/output pins. All pins (port A, B, and C) are programmable as either inputs or outputs under software control of the corresponding data direction register (DDR). The port I/O programming is accomplished by writing the corresponding bit in the port DDR to a logic one for output or a logic zero for input. On reset, all the DDRs are initialized to a logic zero state to put the ports in the input mode. The port output registers are not initialized on reset but should be initialized before changing the DDR bits to avoid undefined levels. When programmed as outputs, the latched output data is readable as input data, regardless of the logic levels at the output pin due to output loading ; see Figure 5-1. All input/output pins are open collector LSTTL/CMOS compatible as both inputs and outputs. A manufacturing mask option enables the choice of additional pull-down devices on all I/O pins (Selection in 5 groups: PA7, PA(5:6), PA(1:4), Port B, PA0 + Port C).

The address map in Figure 2-1 gives the address of data registers and DDRs. The register configuration is discussed under the registers paragraph below.



Data Direction Register Bit	Output Data Bit	Output State	Input To MCU
1	0	0	0
1	1	1	1
0	X	Hi-Z	Pin

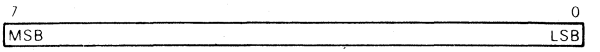
Figure 5-1. Typical I/O Port Circuitry

The latched output data bit (see Figure 5-1) may always be written. Therefore, any write to a port writes to all of its data bits even though the port DDR is set to input. This may be used to initialize the data registers and avoid undefined outputs; however, care must be exercised when using read-modify-write instructions since the data read corresponds to the pin level if the DDR is an input (0) and corresponds to the latched output data when the DDR is an output (1).

5.2 REGISTERS

The registers described below are implemented as RAM locations and thus may be read or written.

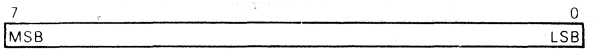
5.2.1 Port Data Register



Port A Address = $00
Port B Address = $01
Port C Address = $02 (Bits 0-3)

The source of data read from the port data register will be the port I/O pin or previously latched output data depending upon the contents of the corresponding data direction register (DDR). The destination of data written to the port data register will be an output data latch. If the corresponding data direction register (DDR) for the port I/O pin is programmed as an output, the data will then appear on the port pin.

5.2.2 Port Data Direction Register



Port A Address = $04
Port B Address = $05
Port C Address = $06 (Bits 0-3)

The port DDRs configure the port pins as either inputs or outputs. Each port pin can be programmed individually to act as an input or an output. A zero in the pins corresponding bit position will program that pin as an input while a one in the pins corresponding bit position will program that pin as an output.

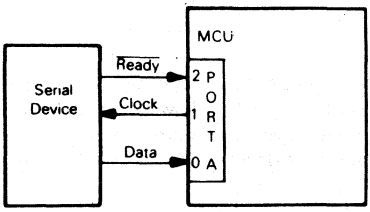
SECTION 6
SOFTWARE AND INSTRUCTION SET

6.1 SOFTWARE

6.1.1 Bit Manipulation

The EF68HC04P3 MCU has the ability to set or clear any register or single random access memory (RAM) writable bit with a single instruction (BSET, BCLR). Any bit in data space, including ROM, can be tested, using the BRSET and BRCLR instructions, and the program may branch as a result of its state. The carry bit equals the value of the bit referenced by BRSET or BRCLR. A rotate instruction may then be used to accumulate serial input data in a RAM location or register. The capability to work with any bit in RAM, ROM, or I/O allows the user to have individual flags in RAM or to handle I/O bits as control lines.

The coding example in Figure 6-1 illustrates the usefulness of the bit manipulation and test instructions. Assume that the MCU is to communicate with an external serial device. The external device has a data ready signal, a data output line, and a clock line (to clock data one bit at a time, MSB first, out of the device). The MCU waits until the data is ready, clocks the external device, picks up the data in the carry flag (C bit), clears the clock line, and finally accumulates the data bit in the accumulator.




```
                .
                .
                .
SELF    BRSET   2,PORTA,SELF
                .
                .
                .
        BSET    1,PORTA
        BRCLR   0,PORTA,CONT
CONT    BCLR    1,PORTA
        ROLA    .
                .
                .
                .
```

Figure 6-1. Bit Manipulation Example

6.1.2 Addressing Modes

The EF68HC04P3 MCU has nine addressing modes which are explained briefly in the following paragraphs. The EF68HC04P3 deals with objects in three different address spaces : program space, data space, and stack space. Program space contains the instructions which are to be executed, plus the data for immediate mode instructions. Data space contains all of the RAM locations, XP and YP registers, accumulator, timer, I/O locations, and some ROM (for storage of tables and constants). Stack space contains RAM for use in stacking the return addresses for subroutines and interrupts.

The term "Effective Address" (EA) is used in describing the address modes. EA is defined as the address from which the argument for an instruction is fetched or stored.

6.1.2.1 IMMEDIATE. In the immediate addressing mode, the operand is located in program ROM and is contained in a byte following the opcode. The immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

6.1.2.2 DIRECT. In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the 256 bytes in data space memory with a single two-byte instruction.

6.1.2.3 SHORT DIRECT. The MCU also has four locations in data space RAM ($80, $81, $82, $83) which may be used in a short-direct addressing mode. In this mode the opcode determines the data space RAM location, and the instruction is only one byte. Short direct addressing is a subset of the direct addressing mode. (Note : $80 and $81 are the X and Y register locations).

6.1.2.4 EXTENDED. In the extended addressing mode, the effective address is obtained by concatenating the four least significant bits of the opcode with the byte following the opcode (12-bit address). Instructions using the extended addressing mode (JMP, JSR) are capable of branching anywhere in program space. An extended addressing mode instruction is two bytes long.

6.1.2.5 RELATIVE. The relative addressing mode is only used in conditional branch instructions. In relative addressing, that address is formed by adding the sign extended lower five bits of the opcode (the offset) to the program counter if and only if the condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from − 15 to + 16 from the opcode address. The programmer need not worry about calculating the correct offset when using the assembler since it calculates the proper offset and checks to see if it is within the span of the branch.

6.1.2.6 BIT SET/CLEAR. In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode specifies the direct address of the byte in which the specified bit is to be set or cleared. Thus, any bit in the 256 locations of data space memory, which can be written to, can be set or cleared.

6.1.2.7 BIT TEST AND BRANCH. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit and condition (set or clear) which is to be tested is included in the opcode, and the data space address of the byte to be tested is in the single byte immediately following the opcode byte. The third byte is sign extended to twelve bits and becomes the offset added to the program counter if the condition is true. The single three-byte instruction allows the program to branch based on the condition of any bit in data space memory. The span of branching is from − 125 to + 130 from the opcode address. The state of the tested bit is also transferred to the carry flag.

6.1.2.8 REGISTER-INDIRECT. In the register-indirect addressing mode, the operand is at the address (in data space) pointed to by the contents of one of the indirect registers (X or Y). The particular X or Y register is selected by bit 4 of the opcode. Bit 4 of the opcode is then decoded into an address which selects the desired X or Y register ($80 or $81). A register-indirect instruction is one byte long.

6.1.2.9 INHERENT. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

6.2 INSTRUCTION SET

The EF68HC04P3 MCU has a set of 44 basic instructions, which when combined with nine addressing modes produce 244 usable opcodes. They can be divided into five different types : register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

6.2.1 Register/Memory Instructions

Most of these instructions use two operands. One operand is the accumulator and the other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operands. Refer to Table 6-1.

6.2.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. There are ten instructions which utilize read-modify-write cycles. All INC and DEC forms along with all bit manipulation instructions use this method. Refer to Table 6-2.

6.2.3 Branch Instructions

The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 6-3.

6.2.4 Bit Manipulation Instructions

These instructions are used on any bit in data space memory. One group either sets or clears. The other group performs the bit test branch operations. Refer to Table 6-4.

Table 6-1. Register/Memory Instructions

		Addressing Modes																				
		Indirect				Immediate			Direct			Inherent			Extended			Short-Direct				
Function	Mnem	Opcode XP	Opcode YP	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Special Notes
Load A from Memory	LDA	E0	F0	1	4	E8	2	4	F8	2	4	–	–	–	–	–	–	AC-AF	1	4	1
Load XP from Memory	LDXI	--	–	–	–	B0	3	4	–	–	–	–	–	–	–	–	–	–	–	–	4
Load YP from Memory	LDYI	–	–	–	–	B0	3	4	–	–	–	–	–	–	–	–	–	–	–	–	4
Store A in Memory	STA	E1	F1	1	4	–	–	–	F9	2	4	–	–	–	–	–	–	BC-BF	1	4	2
Add to A	ADD	E2	F2	1	4	EA	2	4	FA	2	4	–	–	–	–	–	–	–	–	–	–
Subtract from A	SUB	E3	F3	1	4	EB	2	4	FB	2	4	–	–	–	–	–	–	–	–	–	–
Arithmetic Compare with Memory	CMP	E4	F4	1	4	EC	2	4	FC	2	4	–	–	–	–	–	–	–	–	–	–
AND Memory to A	AND	E5	F5	1	4	ED	2	4	FD	2	4	–	–	–	–	–	–	–	–	–	–
Jump to Subroutine	JSR	–	–	–	–	–	–	–	–	–	–	–	–	–	8 (TAR)	2	4	–	–	–	3
Jump Unconditional	JMP	–	–	–	–	–	–	–	–	–	–	–	–	–	9 (TAR)	2	4	–	–	–	3
Clear A	CLRA	–	–	–	–	–	–	–	FB	2	4	–	–	–	–	–	–	–	–	–	–
Clear XP	CLRX	–	–	–	–	–	–	–	FB	2	4	–	–	–	–	–	–	–	–	–	–
Clear YP	CLRY	–	–	–	–	–	–	–	FB	2	4	–			–	–	–	–	–	–	–
Complement A	COMA	–	–	–	–	–	–	–	–	–	–	B4	1	4	–	–	–	–	–	–	–
Move Immediate Value to Memory	MVI	–	–	–	–	B0	3	4	B0	3	4	–	–	–	–	–	–	–	–	–	5
Rotate A Left and Carry	ROLA	–	–	–	–	–	–	–	–	–	–	B5	1	4	–	–	–	–	–	–	–
Arithmetic Left Shift of A	ASLA	–	–	–	–	–	–	–	FA	2	4	–	–	–	–	–	–	–	–	–	–

SPECIAL NOTES

1. In Short-Direct addressing, the LDA mnemonic represents opcode AC, AD, AE, and AF. This is equivalent to RAM locations $80 (AC), $81 (AD), $82 (AE), and $83 (AF)
2. In Short-Direct addressing, the STA mnemonic represents opcode BC, BD, BE, and BF. This is equivalent to RAM locations $80 (BC), $81 (BD), $82 (BE), and $83 (BF).
3. In Extended addressing, the four LSBs of the opcode (Mnemonic JSR and JMP) are formed by the four MSBs of the target address (TAR).
4. In Immediate addressing, the LDXI and LDYI are mnemonics which are recognized as follows:
   LDXI = MVI $80,data
   LDYI = MVI $81,data Where data is a one-byte hexadecimal number.
5. The MVI instruction refers to both Immediate and Direct addressing.

Table 6-2. Read-Modify-Write Instructions

		Addressing Modes										
		Indirect				Direct			Short-Direct			
		Opcode		#	#		#	#		#	#	Special
Function	Mnem	XP	YP	Bytes	Cycles	Opcode	Bytes	Cycles	Opcode	Bytes	Cycles	Notes
Increment Memory Location	INC	E6	F6	1	4	FE	2	4	A8-AB	1	4	1, 3
Increment A	INCA	–	–	–	–	FE	2	4	–	–	–	–
Increment XP	INCX	–	–	–	–	–	–	–	A8	1	4	–
Increment YP	INCY	–	–	–	–	–	–	–	A9	1	4	–
Decrement Memory Location	DEC	E7	F7	1	4	FF	2	4	B8-BB	1	4	2, 4
Decrement A	DECA	–	–	–	–	FF	2	4	–	–	–	–
Decrement XP	DECX	–	–	–	–	–	–	–	B8	1	4	–
Decrement YP	DECY	–	–	–	–	–	–	–	B9	1	4	–

SPECIAL NOTES

1. In Short-Direct addressing, the INC mnemonic represents opcode A8, A9, AA, and AB. These are equivalent to RAM locations $80 (A8), $81 (A9), $82 (AA), and $83 (AB).
2. In Short-Direct addressing, the DEC mnemonic represents opcode B8, B9, BA, and BB. These are equivalent to RAM locations $80 (B8), $81 (B9), $82 (BA), and $83 (BB).
3. In Indirect addressing, the INC mnemonic represents opcode E6 or F6, and causes the location pointed to by XP (E6 opcode) or YP (F6 opcode) to be incremented.
4. In Indirect addressing, the INC mnemonic represents opcode E7 or F7, and causes the location pointed to by XP (E7 opcode) or YP (F7 opcode) to be incremented.

Table 6-3. Branch Instructions

		Relative Addressing Mode			
Function	Mnem	Opcode	# Bytes	# Cycles	Special Notes
Branch if Carry Clear	BCC	40-5F	1	2	1
Branch if Higher or Same	(BHS)	40-5F	1	2	1, 2
Branch if Carry Set	BCS	60-7F	1	2	1
Branch if Lower	(BLO)	60-7F	1	2	1, 3
Branch if Not Equal	BNE	00-1F	1	2	1
Branch if Equal	BEQ	20-3F	1	2	1

SPECIAL NOTES

1. Each mnemonic of the Branch Instructions covers a range of 32 opcodes, e.g., BCC ranges from 40 through 5F. The actual memory location (target address) to which the branch is made is formed by adding the sign extended lower 5 bits of the opcode to the contents of the program counter
2. The BHS instruction (shown in parentheses) is identical to the BCC instruction. The C bit is clear if the register was higher or the same as the location in the memory to which it was compared
3. The BLO instruction (shown in parentheses) is identical to the BCS instruction. The C bit is set if the register was lower than the location in memory to which it was compared

Table 6-4. Bit Manipulation Instructions

		Addressing Modes						
		Bit Set/Clear			Bit Test and Branch			
Function	Mnem	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Special Note
Branch IFF Bit n is set	BRSET n (n=0 7)				C8 + n	3	5	1
Branch IFF Bit n is clear	BRCLR n (n=0 7)				C0 + n	3	5	1
Set Bit n	BSET n (n=0 7)	D8 + n	2	4				1
Clear Bit n	BCLR n (n=0 7)	D0 + n	2	4				1

SPECIAL NOTE

1. The opcode is formed by adding the bit number (0-7) to the basic opcode. For example: to clear bit six using the BCLR instruction the opcode becomes DE (D8 + 6), BCLR5 becomes (C0 + 5), etc.

6.2.5 Control Instructions

The control instructions control the MCU operations during program execution. Refer to Table 6-5.

6.2.5.1 Stop instruction

The STOP instruction places the EF68HC04P3 in its lowest power consumption mode. In STOP mode the internal oscillator is turned off causing all internal processing and the timer to be halted. In STOP mode, timer STATUS/CONTROL register bits 6 (ETI) and 7 (TMZ) are cleared to remove any pending timer interrupt requests and to disable any further timer interrupts. External interrupts are enabled. All I/O lines remain unchanged. The processor can only be brought out of the STOP mode by pulling low $\overline{IRQ}$ or $\overline{RESET}$ input pins. During the exit from the STOP mode, the timer is used to provide a delay of 1920 oscillator clock periods for the oscillator to stabilize. If an external clock is used, it should be kept high during all the time the MCU is in STOP mode.

6.2.5.2 Wait instruction

The WAIT instruction places EF68HC04P3 in a low-power consumption mode, but WAIT mode consumes more power than the STOP mode. In WAIT mode the clock is disabled from all internal circuitry except the timer circuit. Thus all internal processing is halted. The timer may, if desired, continue to count down ($\overline{PSI}$ bit of TCSR).
During the WAIT mode, external interrupts are enabled. All other registers memory, and I/O lines remain in their last state. Timer interrupt (ETI bit) may be enabled by software prior to entering the WAIT mode to allow an exit from the WAIT mode via a Timer Interrupt.

6.2.6 Alphabetical Listing

The complete instruction set is given in alphabetical order in Table 6-6. There are certain mnemonics recognized by the assember and converted to other instructions. The fact that all registers and accumulator are in RAM allows many implied instructions to exist. The implied instructions recognized by the assembler are identified in Table 6-6.

6.2.7 Opcode Map Summary

Table 6-7 contains an opcode map for the instructions used on the MCU.

6.3 IMPLIED INSTRUCTIONS

Since the accumulator and all other registers are located in RAM many implied instructions exist. The assembler-recognized implied instructions are given in Table 6-6. Some examples not recognized by the assembler are shown below.

BCLR,7 $FF	Ensures accumulator is plus
BSET,7 $FF	Ensures accumulator is minus
BRCLR,7 $FF	Branch iff accumulator is plus
BRSET,7 $FF	Branch iff accumulator is minus
BRCLR,7 $80	Branch iff X is plus (BXPL)
BRSET,7 $80	Branch iff X is minus (BXMI)
BRCLR,7 $81	Branch iff Y is plus (BYPL)
BRSET,7 $81	Branch iff Y is minus (BYMI)

Table 6-5. Control Instructions

		Addressing Modes									
		Short-Direct			Inherent			Relative			
Function	Mnem	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Special Notes
Transfer A to XP	TAX	BC	1	4	–	–	–	–	–	–	–
Transfer A to YP	TAY	BD	1	4	–	–	–	–	–	–	–
Transfer XP to A	TXA	AC	1	4	–	–	–	–	–	–	–
Transfer YP to A	TYA	AD	1	4	–	–	–	–	–	–	–
Return from Subroutine	RTS	–	–	–	B3	1	2	–	–	–	–
Return from Interrupt	RTI	–	–	–	B2	1	2	–	–	–	–
No-Operation	NOP	–	–	–	–	–	–	–	–	–	1
Stop	STOP	–	–	–	B6	1	2	–	–	–	–
Wait	WAIT	–	–	–	B7	1	2	–	–	–	–

SPECIAL NOTE

1. The NOP instruction is equivalent to a branch if equal (BEQ) to the location designated by PC + 1

Table 6-6. Instruction Set

Mnemonic	Addressing Modes: Inherent	Immediate	Direct	Short Direct	Bit Set Clear	Bit-Test-Branch	Register Indirect	Extended	Relative	Flags: Z	C
ADD		X	X				X			Λ	Λ
AND		X	X				X			Λ	•
ASLA	Assembler converts this to "ADD $FF"									Λ	Λ
BCC									X	•	•
BCLR					X					•	•
BCS									X	•	•
BEQ									X	•	•
BHS	Assembler converts this to "BCC"									•	•
BLO	Assembler converts this to "BCS"									•	•
BNE									X	•	•
BRCLR						X				•	Λ
BRSET						X				•	Λ
BSET					X					•	•
CLRA	Assembler converts this to "SUB $FF"									Λ	Λ
CLRX	Assembler converts this to "MVI = 0, $80"									•	•
CLRY	Assembler converts this to "MVI = 0, $81"									•	•
CMP		X	X				X			Λ	Λ
COMA	X									Λ	Λ
DEC			X	X			X			Λ	•
DECA	Assembler converts this to "DEC $FF"									Λ	•
DECX	Assembler converts this to "DEC $80"									Λ	•
DECY	Assembler converts this to "DEC $81"									Λ	•
INC			X	X			X			Λ	•
INCA	Assembler converts this to "INC $FF"									Λ	•
INCX	Assembler converts this to "INC $80"									Λ	•
INCY	Assembler converts this to "INC $81"									Λ	•
JMP								X		•	•
JSR								X		•	•
LDA		X	X	X			X			Λ	•
LDXI	Assembler converts this to "MVI DATA, $80"									•	•
LDYI	Assembler converts this to "MVI DATA, $81"									•	•
MVI		X	X							•	•
NOP	Assembler converts this to "BEQ (PC) + 1"									•	•
ROLA	X									Λ	Λ
RTI	X									Λ	Λ
RTS	X									•	•
STA			X	X			X			Λ	•
STOP	X									•	•
SUB		X	X				X			Λ	Λ
TAX	Assembler converts this to "STA $80"										•
TAY	Assembler converts this to "STA $81"										•
TXA	Assembler converts this to "LDA $80"										•
TYA	Assembler converts this to "LDA $81"										•
WAIT	X									•	•

Flag Symbols: Z = Zero, C = Carry/Borrow, Λ = Test and Set if True, Cleared Otherwise, • = Not Affected

Table 6-7. EF68HC04P3 Microcomputer

Branch Instructions

Hi / Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111
0 0000	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
1 0001	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
2 0010	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
3 0011	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
4 0100	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
5 0101	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
6 0110	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
7 0111	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
8 1000	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
9 1001	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
A 1010	2 BNE 1 REL	2 BNE 2 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
B 1011	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
C 1100	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
D 1101	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
E 1110	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL
F 1111	2 BNE 1 REL	2 BNE 1 REL	2 BEQ 1 REL	2 BEQ 1 REL	2 BCC 1 REL	2 BCC 1 REL	2 BCS 1 REL	2 BCS 1 REL

Abbreviations for Address Modes

INH	Inherent
S-D	Short Direct
B-T-B	Bit Test and Branch
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
R-IND	Register Indirect

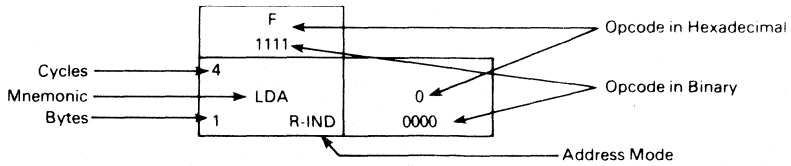
* Indicates Instruction Reserved for Future Use

\# Indicates Illegal Instruction

Instruction Set Opcode Map

Register/Memory, Control, and Read/Modify/Write Instructions				Bit Manipulation Instructions		Register/Memory and Read/Modify/Write		
8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Hi / Low
4 JSRn 2 EXT	4 JMPn 2 EXT	*	4 MVI 3 IMM	5 BRCLR0 3 BTB	4 BCLR0 2 BSC	4 LDA 1 R IND	4 LDA 1 R IND	0 0000
4 JSRn 2 EXT	4 JMPn 2 EXT	*	*	5 BRCLR1 3 BTB	4 BCLR1 2 BSC	4 STA 1 R IND	4 STA 1 R IND	1 0001
4 JSRn 2 EXT	4 JMPn 2 EXT	*	2 RTI 1 INH	5 BRCLR2 3 BTB	4 BCLR2 2 BSC	4 ADD 1 R IND	4 ADD 1 R IND	2 0010
4 JSRn 2 EXT	4 JMPn 2 EXT	*	2 RTS 1 INH	5 BRCLR3 3 BTB	4 BCLR3 2 BSC	4 SUB 1 R IND	4 SUB 1 R IND	3 0011
4 JSRn 2 EXT	4 JMPn 2 EXT	*	4 COMA 1 INH	5 BRCLR4 3 BTB	4 BCLR4 2 BSC	4 CMP 1 R IND	4 CMP 1 R IND	4 0100
4 JSRn 2 EXT	4 JMPn 2 EXT	*	4 ROLA 1 INH	5 BRCLR5 3 BTB	4 BCLR5 2 BSC	4 AND 1 R IND	4 AND 1 R IND	5 0101
4 JSRn 2 EXT	4 JMPn 2 EXT	*	2 STOP 1 INH	5 BRCLR6 3 BTB	4 BCLR6 2 BSC	4 INC 1 R IND	4 INC 1 R IND	6 0110
4 JSRn 2 EXT	4 JMPn 2 EXT	*	2 WAIT 1 INH	5 BRCLR7 3 BTB	4 BCLR7 2 BSC	4 DEC 1 R IND	4 DEC 1 R IND	7 0111
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 SD	4 DEC 1 SD	5 BRSET0 3 BTB	4 BSET0 2 BSC	4 LDA 2 IMM	4 LDA 2 DIR	8 1000
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 SD	4 DEC 1 SD	5 BRSET1 3 BTB	4 BSET1 2 BSC	#	4 STA 2 DIR	9 1001
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 SD	4 DEC 1 SD	5 BRSET2 3 BTB	4 BSET2 2 BSC	4 ADD 2 IMM	4 ADD 2 DIR	A 1010
4 JSRn 2 EXT	4 JMPn 2 EXT	4 INC 1 SD	4 DEC 1 SD	5 BRSET3 3 BTB	4 BSET3 2 BSC	4 SUB 2 IMM	4 SUB 2 DIR	B 1011
4 JSRn 2 EXT	4 JMPn 2 EXT	4 LDA 1 SD	4 STA 1 SD	5 BRSET4 3 BTB	4 BSET4 2 BSC	4 CMP 2 IMM	4 CMP 2 DIR	C 1100
4 JSRn 2 EXT	4 JMPn 2 EXT	4 LDA 1 SD	4 STA 1 SD	5 BRSET5 3 BTB	4 BSET5 2 BSC	4 AND 2 IMM	4 AND 2 DIR	D 1101
4 JRSn 2 EXT	4 JMPn 2 EXT	4 LDA 1 SD	4 STA 1 SD	5 BRSET6 3 BTB	4 BSET6 2 BSC	#	4 INC 2 DIR	E 1110
4 JSRn 2 EXT	4 JMPn 2 EXT	4 LDA 1 SD	4 STA 1 SD	5 BRSET7 3 BTB	4 BSET7 2 BSC	#	4 DEC 2 DIR	F 1111

LEGEND



SECTION 7
ELECTRICAL SPECIFICATIONS

7.1 INTRODUCTION

This section contains the electrical specifications and associated timing for the EF68HC04P3.

7.2 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{in}	V_{SS} -0.3 to V_{SS} +0.3	V
Current Drain per Pin	I	10	mA
Total Current for Ports A, B, C and XTAL, TIMER Pins — Sink	I_I	30	mA
Total Current for Ports A, B, C and XTAL, TIMER Pins — Source	I_O	15	mA
Operating Temperature Range	T_A	T_L to T_H	°C
L Range		0 to 70	
D Range		-25 to 70	
V Range		-40 to 85	
Storage Temperature Range	T_{stg}	-55 to 150	°C
Thermal Resistance	θ_{JA}		°C/W
Plastic		85	
PLCC		85	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$. Reliability of operation is enhanced if unused inputs except EXTAL are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

7.3 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction Temperature	T_J		°C
Plastic		150	
PLCC		150	

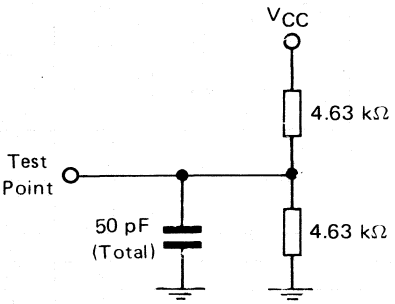


Figure 7-1. Open Collector LSTTL Compatible Equivalent Test Load (Ports A, B, C,)

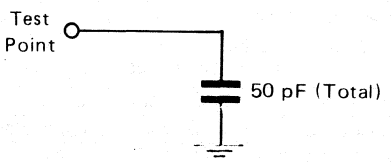


Figure 7-2. CMOS Equivalent Test Load (Ports A, B, C)

7.4 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts – Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts – User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

7.5 ELECTRICAL CHARACTERISTICS @ 5.0 V

(V_{CC} = 5.0 Vdc ± 10 % ; V_{SS} = 0 Vdc ; $T_A = T_L$ to T_H unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output voltage					
(I_{Load} = 10 µA)	V_{OL}	–	–	0.1	V
(I_{Load} = –10 µA)	V_{OH}	V_{CC} – 0.1	–	–	
Output Low Voltage (I_{Load} = 0.8 mA) PA0-PA7, PB0-PB7, PC0-PC3	V_{OL}	–	–	0.4	V
Output High Voltage (I_{Load} = –0.8 mA) PA0-PA7, PB0-PB7, PC0-PC3	V_{OH}	V_{CC} –0.4	–	–	V
Input Low Voltage					
PA0-PA7, PB0-PB7, PC0-PC3, TIMER	V_{IL}	V_{SS}	–	0.3 V_{CC}	V
XTAL, MDS, $\overline{IRQ}$, $\overline{RESET}$	V_{IL}	V_{SS}	–	0.2 V_{CC}	
Input High Voltage					
PA0-PA7, PB0-PB7, PC0-PC3, TIMER	V_{IH}	0.7 V_{CC}	–	V_{CC}	V
XTAL, MDS, $\overline{IRQ}$, $\overline{RESET}$	V_{IH}	0.8 V_{CC}	–	V_{CC}	
Total Supply Current (No dc Loads, (No dc Loads, V_{IL} = 0.2 V ; V_{IH} = V_{CC} – 0.2 V)					
RUN Mode					
÷ 1 Option (f_{osc} = 5.5-MHz)	I_{DD}	–	2	3.3	mA
÷ 2 Option (f_{osc} = 11.0 MHz)	I_{DD}	–	2.4	3.9	mA
÷ 4 Option (f_{osc} = 11.0 MHz)	I_{DD}	–	1.6	2.6	mA
WAIT Mode (See Note)					
÷ 1 Option (f_{osc} = 5.5 MHz)	I_{DD}	–	0.7	1.1	mA
÷ 2 Option (f_{osc} = 11.0 MHz)	I_{DD}	–	1.1	1.8	mA
÷ 4 Option (f_{osc} = 11.0 MHz)	I_{DD}	–	0.9	1.5	mA
STOP Mode (See Note)	I_{DD}	–	1.0	5	µA
I/O Hi-Z Leakage Current (V_{in} = 0.4 V to V_{CC} - 0.4 V) Timer, PA0-PA7, PB0-PB7, PC0-PC3 (with no pull-downs)	I_{TSI}	–10	–	10	µA
Hi-Z State Input Current (V_{in} = V_{CC} – 0.4 V) PA0-PA7, PB0-PB7, PC0-PC3 (with pull-downs)	I_{TSI}	40	–	300	µA
Input Current $\overline{IRQ}$, $\overline{RESET}$, XTAL, MDS	I_{in}	–1	–	+ 1	µA
I/O Output Capacitance Timer, PA0-PA7, PB0-PB7, PC0-PC3	C_{out}	–	–	12	pF
Input Capacitance $\overline{IRQ}$, $\overline{RESET}$, XTAL, MDS	C_{in}	–	–	8	pF

NOTE : Test conditions for I_{DD} as follows :

XTAL input is a square wave from 0.2 V to V_{CC} – 0.2 V.

EXTAL output load = 10 pF

Circuit in self check-mode

In WAIT and STOP Modes, Port A is programmed as output, Ports B and C are programmed as inputs.

In STOP Mode : all inputs are tied to V_{IL} excepted $\overline{IRQ}$, $\overline{RST}$, MDS, XTAL, EXTAL which are tied to V_{IH}.

7.6 CONTROL TIMING @ 5.0 V

(V_{CC} = 5.0 Vdc ± 10 % ; V_{SS} = 0 Vdc ; $T_A = T_L$ to T_H unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency					
÷ 2, ÷ 4 options	f_{osc}	0	–	11.0	MHz
÷ 1 option	f_{osc}	0	–	5.5	MHz
Bit Time	t_{bit}	0.182	–	–	µs
Bit Cycle Time	t_{byte}	2.18	–	–	µs
$\overline{IRQ}$ and TIMER Pulse Width	t_{WL}, t_{WM}	2	–	–	t_{byte}
$\overline{RESET}$ Pulse Width	t_{RWL}	2	–	–	t_{byte}
Oscillator Pulse Width ÷ 2, ÷ 4 options	t_{OL}, t_{OH}	45	–	–	ns
÷ 1 option		90	–	–	ns

7.7 ELECTRICAL CHARACTERISTICS @ 3.3 V

(V_{CC} = 3.3 Vdc ± 10 % ; V_{SS} = 0 Vdc ; $T_A = T_L$ to T_H unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output voltage					
(I_{Load} = 10 µA)	V_{OL}	–	–	0.1	V
(I_{Load} = −10 µA)	V_{OH}	V_{CC} − 0.1	–	–	
Output Low Voltage (I_{Load} = 0.4 mA) PA0-PA7, PB0-PB7, PC0-PC3	V_{OL}	–	–	0.4	V
Output High Voltage (I_{Load} = −0.4 mA) PA0-PA7, PB0-PB7, PC0-PC3	V_{OH}	V_{CC} −0.4	–	–	V
Input Low Voltage					
PA0-PA7, PB0-PB7, PC0-PC3, TIMER	V_{IL}	V_{SS}	–	0.3 V_{CC}	V
XTAL, MDS, $\overline{IRQ}$, $\overline{RESET}$	V_{IL}	V_{SS}	–	0.2 V_{CC}	
Input High Voltage					
PA0-PA7, PB0-PB7, PC0-PC3, TIMER	V_{IH}	0.7 V_{CC}	–	V_{CC}	V
XTAL, MDS, $\overline{IRQ}$, $\overline{RESET}$	V_{IH}	0.8 V_{CC}	–	V_{CC}	
Total Supply Current (No dc Loads, (No dc Loads, V_{IL} = 0.2 V ; V_{IH} = V_{CC} − 0.2 V)					
RUN Mode					
÷ 1 Option (f_{osc} = 3.0 MHz)	I_{DD}	–	0.7	TBD	mA
÷ 2 Option (f_{osc} = 6.0 MHz)	I_{DD}	–	0.9	TBD	mA
÷ 4 Option (f_{osc} = 6.0 MHz)	I_{DD}	–	0.6	TBD	mA
WAIT Mode (See Note)					
÷ 1 Option (f_{osc} = 3.0 MHz)	I_{DD}	–	0.25	TBD	mA
÷ 2 Option (f_{osc} = 6.0 MHz)	I_{DD}	–	0.40	TBD	mA
÷ 4 Option (f_{osc} = 6.0 MHz)	I_{DD}	–	0.35	TBD	mA
STOP Mode (See Note)	I_{DD}	–	0.5	2	µA
I/O Hi-Z Leakage Current (V_{in} = 0.4 V to V_{CC} = 0.4 V) Timer, PA0-PA7, PB0-PB7, PC0-PC3 (with no pull-downs)	I_{TSI}	−10	–	10	µA
Hi-Z State Input Current (V_{in} = V_{CC} − 0.4 V) PA0-PA7, PB0-PB7, PC0-PC3 (with pull-downs)	I_{TSI}	–	125	–	µA
Input Current $\overline{IRQ}$, $\overline{RESET}$, XTAL, MDS	I_{in}	−1	–	+ 1	µA
I/O Output Capacitance Timer, PA0-PA7, PB0-PB7, PC0-PC3	C_{out}	–	–	12	pF
Input Capacitance $\overline{IRQ}$, $\overline{RESET}$, XTAL, MDS	C_{in}	–	–	8	pF

NOTE : Test conditions for I_{DD} as follows :
XTAL input is a square wave from 0.2 V to V_{CC} − 0.2 V.
EXTAL output load = 10 pF
Circuit in self check-mode
In WAIT and STOP Modes, Port A is programmed as output, Ports B and C are programmed as inputs.
In STOP Mode : all inputs are tied to V_{IL} excepted $\overline{IRQ}$, $\overline{RST}$, MDS, XTAL, EXTAL which are tied to V_{IH}.

7.8 CONTROL TIMING @ 3.3 V

(V_{CC} = 3.3 Vdc ± 10 % ; V_{SS} = 0 Vdc ; $T_A = T_L$ to T_H unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency					
÷ 2, ÷ 4 options	f_{osc}	0	–	6.0	MHz
÷ 1 option	f_{osc}	0	–	3.0	MHz
Bit Time	t_{bit}	0.333	–	–	µs
Bit Cycle Time	t_{byte}	4.0	–	–	µs
$\overline{IRQ}$ and TIMER Pulse Width	t_{WL}, t_{WM}	2	–	–	t_{byte}
$\overline{RESET}$ Pulse Width	t_{RWL}	2	–	–	t_{byte}
Oscillator Pulse Width ÷ 2, ÷ 4 options	t_{OL}, t_{OH}	80	–	–	ns
÷ 1 option		160	–	–	ns

7.9 ELECTRICAL CHARACTERISTICS @ 2.2 V

(V_{CC} = 2.2 Vdc ± 10 % ; V_{SS} = 0 Vdc ; $T_A = T_L$ to T_H unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output voltage					
(I_{Load} = 10 µA)	V_{OL}	–	0.1	–	V
(I_{Load} = – 10 µA)	V_{OH}	–	V_{CC} – 0.1	–	
Output Low Voltage (I_{Load} = 0.2 mA) PA0-PA7, PB0-PB7, PC0-PC3	V_{OL}	–	0.4	–	V
Output High Voltage (I_{Load} = 0.2 mA) PA0-PA7, PB0-PB7, PC0-PC3	V_{OH}	–	V_{CC} – 0.4	–	V
Input Low Voltage					
PA0-PA7, PB0-PB7, PC0-PC3, TIMER	V_{IL}	–	0.3 V_{CC}	–	V
XTAL, MDS, $\overline{IRQ}$, $\overline{RESET}$	V_{IL}	–	0.2 V_{CC}	–	
Input High Voltage					
PA0-PA7, PB0-PB7, PC0-PC3, TIMER	V_{IH}	–	0.7 V_{CC}	–	V
XTAL, MDS, $\overline{IRQ}$, $\overline{RESET}$	V_{IH}	–	0.8 V_{CC}	–	
Total Supply Current (No dc Loads, (No dc Loads, V_{IL} = 0.2 V ; V_{IH} = V_{CC} – 0.2 V)					
RUN Mode					
÷ 1 Option (f_{osc} 1.0 MHz)	I_{DD}	–	150	TBD	µA
÷ 2 Option (f_{osc} 2.0 MHz)	I_{DD}	–	175	TBD	µA
÷ 4 Option (f_{osc} 2.0 MHz)	I_{DD}	–	115	TBD	µA
WAIT Mode (See Note)					
÷ 1 Option (f_{osc} 1.0 MHz)	I_{DD}	–	50	TBD	µA
÷ 2 Option (f_{osc} 2.0 MHz)	I_{DD}	–	80	TBD	µA
÷ 4 Option (f_{osc} 2.0 MHz)	I_{DD}	–	70	TBD	µA
STOP Mode (See Note)	I_{DD}	–	0.5	2	µA
I/O Hi-Z Leakage Current (V_{in} 0.4 V to V_{CC} – 0.4 V) Timer, PA0-PA7, PB0-PB7, PC0-PC3 (with no pull-downs)	I_{TSI}	–10	–	10	µA
Hi-Z State Input Current (V_{in} V_{CC} – 0.4 V) PA0-PA7, PB0-PB7, PC0-PC3 (with pull-downs)	I_{TSI}	–	75	–	µA
Input Current $\overline{IRQ}$, $\overline{RESET}$, XTAL, MDS	I_{in}	–1	–	+ 1	µA
I/O Output CapacitanceTimer, PA0-PA7, PB0-PB7, PC0-PC3	C_{out}	–	–	12	pF
Input Capacitance $\overline{IRQ}$, $\overline{RESET}$, XTAL, MDS	C_{in}	–	–	8	pF

NOTE : Test conditions for I_{DD} as follows :
XTAL input is a square wave from 0.2 V to V_{CC} – 0.2 V.
EXTAL output load = 10 pF
Device in self check-mode
In WAIT and STOP Modes, Port A is programmed as output, Ports B and C are programmed as inputs.
In STOP Mode : all inputs are tied to V_{IL} excepted $\overline{IRQ}$, $\overline{RST}$, MDS, XTAL, EXTAL which are tied to V_{IH}.

7.10 CONTROL TIMING @ 2.2 V

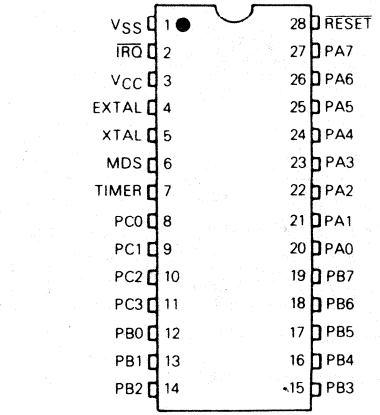
(V_{CC} = 2.2 Vdc ± 10 % ; V_{SS} = 0 Vdc ; $T_A = T_L$ to T_H unless otherwise noted).

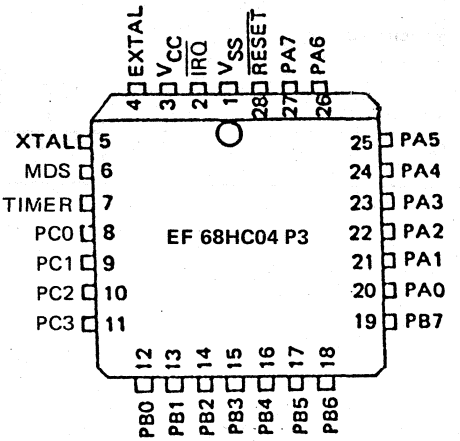
Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency					
÷ 2, ÷ 4 options	f_{osc}	0	2.0	–	MHz
÷ 1 option	f_{osc}	0	1.0	–	MHz
Bit Time	t_{bit}	–	1.0	–	µs
Bit Cycle Time	t_{byte}	–	12.0	–	µs
$\overline{IRQ}$ and TIMER Pulse Width	t_{WL}, t_{WM}	2	–	–	t_{byte}
$\overline{RESET}$ Pulse Width	t_{RWL}	2	–	–	t_{byte}
Oscillator Pulse Width ÷ 2, ÷ 4 options	t_{OL}, t_{OH}	–	250	–	ns
÷ 1 option		–	500	–	ns

SECTION 8
MECHANICAL DATA

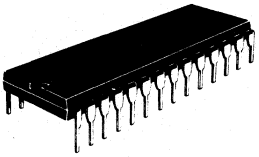
This section contains the pin assignment and package dimension diagrams for the EF68HC04P3 microcomputer.

8.1 PIN ASSIGNMENTS

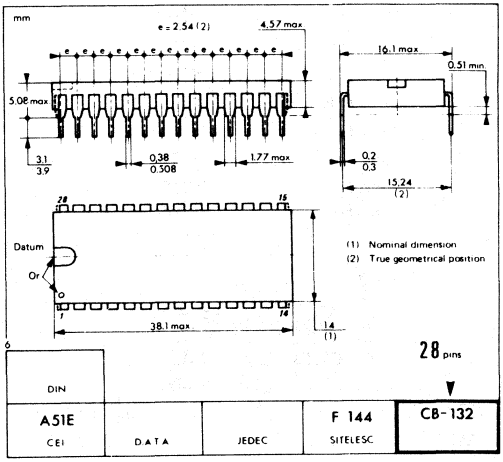




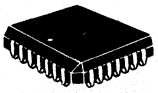
CASE CB-132



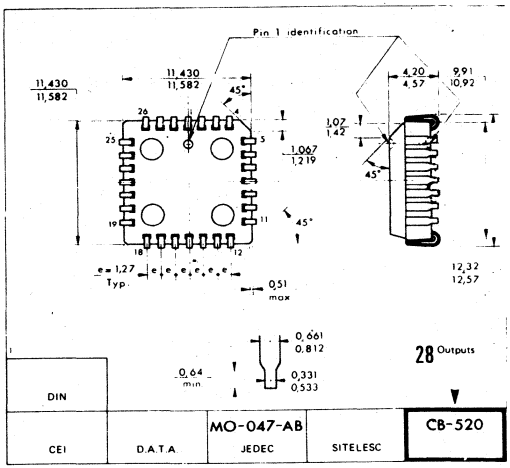
P SUFFIX
PLCC 28



CASE CB-520



FN SUFFIX
PLCC 28



SECTION 9
ORDERING INFORMATION

9.1 INTRODUCTION

The following information is required when ordering a custom MCU. The information may be transmitted to THOMSON SEMICONDUCTEURS in the following media:

EPROM(s), ET2716 or ET2732
EFDOS/MDOS*, disk file

To initiate a ROM pattern for the MCU, it is necessary to first contact your local field service office, local sales person, or your local THOMSON SEMICONDUCTEURS representative.

9.1.1 EPROMs

A 2716 or 2732 type EPROM, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. Since all program and data space information will fit on one 2716 or 2732 EPROM, the EPROM must be programmed as follows in order to emulate the EF68HC04P3 MCU. **Start the data space ROM at EPROM address $018 and start program space ROM at EPROM address $960 and continue to memory space $FFF. All unused bytes, including the user's space, must be set to zero.** For shipment to THOMSON SEMICONDUCTEURS the EPROMs should be placed in a conductive IC carrier and packed securely. Do not use styrofoam.

9.1.2 EFDOS/MDOS* Disk File

An EFDOS/MDOS* disk, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. **When using the EFDOS/MDOS* disk, include the entire memory image of both data and program space. All unused bytes, including the user's space, must be set to zero.**

9.2 VERIFICATION MEDIA

All original pattern media (EPROMs or floppy disk) are filed for contractual purposes and are not returned. A computer listing of the ROM code will be generated and returned along with a listing verification form. The listing should be thoroughly checked and the verification form completed, signed, and returned to THOMSON SEMICONDUCTEURS. The signed verification form constitutes the contractural agreement for creation of the customer mask. If desired, THOMSON SEMICONDUCTEURS will program a blank 2716, 2732, or EFDOS disk **(supplied by the customer)** from the data file used to create the custom mask to aid in the verification process.

* Requires prior factory approval.

9.3 ROM VERIFICATION UNITS (RVUs)

Ten MCUs containing the customer's ROM pattern will be sent for program verification. These units will have been made using the custom mask but are for the purpose of ROM verification only. For expediency they are usually unmarked, packaged in ceramic, and tested only at room temperature and five volts. These RVUs are included in the mask charge and are not production parts. These RVUs are not backed nor guaranteed by THOMSON SEMICONDUCTEURS Quality Assurance.

9.4 FLEXIBLE DISKS

The disk media submitted must be single-sided, EFDOS/MDOS* compatible floppies. The customer must clearly label the disk with the ROM pattern file name. The minimum EFDOS/MDOS* system files as well as the absolute binary object files (filename.LO type of file) and filename.DO if necessary from the EF6804 cross-assembler must be on the disk. An object file made from a memory dump, using the ROLLOUT command is also admissable. Consider submitting a source listing as well as : filename, .LX (DEVICE®/EXORciser® loadable format) . This file will of course be kept confidential and is used 1) to speed up the process in house if any problems arise, and 2) to speed up our customer to factory interface if a user finds any software errors and needs assistance quickly from the factory representative.

* Requires prior factory approval.
DEVICE® is a registered trademark from THOMSON SEMICONDUCTEURS.
EXORciser® is a registered trademark of MOTOROLA INC.

ORDERING INFORMATION

EF68HC04P3 | C | V
Device
Package
Screening level
Oper. temp.

The table below horizontally shows all available suffix combinations for package, operating temperature and screening level. Other possibilities on request.

DEVICE	PACKAGE					OPER. TEMP			SCREENING LEVEL			
	C		P		FN	L*	D	V**	Std	D	T	
EF68HC04P3			●		●	●	●		●			

Examples : EF68HC04P3P, EF68HC04P3FN.

Package: C: Ceramic DIL, **DIL, P:** Plastic DIL, **FN:** PLCC.
Oper. temp.: L*: 0°C to + 70°C, **D:** — 25°C to + 70°C, **V:** — 40°C to + 85°C, **T:** — 40°C to + 105°C
Screening level: Std: (no-end suffix), **D:** NFC 96883 level D.
* **May be omitted.**

A reduced-packaged version of the EF68HC04P3 (28 pins) will be available in a 20-pin package : EF68HC04J3.

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

EF6804 FAMILY – MCU CUSTOMER ORDERING SHEET

Commercial reference : E F 6 8 H C 0 4 P 3

Customer's marking : _____ (11 characters max.)

Application : .....

.....

ROM capacity required : _____ bytes

Temperature range :

- ☐ 0°C/ + 70°C
- ☐ – 25°C/+ 70°C
- ☐ – 40°C/ + 85°C

Package :

- ☐ Plastic
- ☐ PLCC

Customer name : .....
Company : .....
Address : .....
Phone : .....

Specification reference :

- ☐ THOMSON SEMICONDUCTEURS reference .....
- ☐ Special customer data reference* .....

Quality level :

- ☐ STD
- ☐ D
- ☐ Other* (customer's quality specification ref.) :

.....

Software developed by :

- ☐ THOMSON SEMICONDUCTEURS application lab.
- ☐ External lab.
- ☐ Customer

PATTERN MEDIA (a listing may be supplied in addition for checking purposes) :

- ☐ EPROM Reference :
- ☐ EFDOS/MDOS* disk file (DEVICE/EXORciser)
  - ☐ 8" floppy
  - ☐ 5" 1/4 floppy
- ☐ Other*

OPTION LIST :

– Oscillator input :
- ☐ Xtal
- ☐ RC

– I/O pull-down selection*
- ☐ on PA7
- ☐ on PA(5:6)
- ☐ on PA(1:4)
- ☐ on Port B
- ☐ on PA0 and Port C

– Program ROM protection selected ☐

– Interrupt Trigger
- ☐ Edge-sensitive
- ☐ Level-and edge-sensitive

– Oscillator divider :
- ☐ 2^0
- ☐ 2^1
- ☐ 2^2

* Requires prior factory approval

Yearly quantity forecast :

- start of production date :
- for a shipment period of :

CUSTOMER CONTACT NAME : DATE : SIGNATURE :

54/54

THOMSON SEMICONDUCTEURS

43 - 45, Avenue de l'Europe 78140 VELIZY-FRANCE Tel. (1) 39.46.97.19 Telex 240780F

EF6805 FAMILY

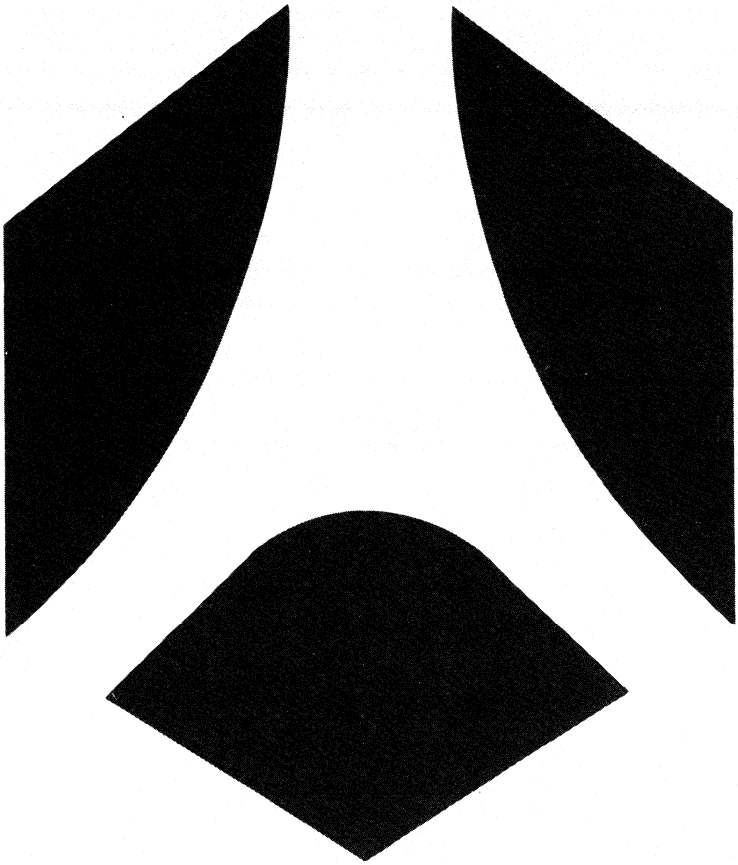
8-BIT MICROCOMPUTER UNIT

PART Nber	TECHNOLOGY	ROM x 8	RAM x 8	I/O	FEATURES	ALT. SOURCE	Nb PINS
EF 6805P2	HMOS	1100	64	20		MC 6805P2 HD 6805S1	28
EF 6805P4	HMOS	1100	112	20		MC 6805P4	28
EF 6805P6	HMOS	1796	64	20		MC 6805P6	28
EF 6805R2	HMOS	2048	64	32	A/D Converter	MC 6805R2	40
EF 6805R3	HMOS	3776	112	32	A/D Converter	MC 6805R3 HD 6805W0	40
EF 6805U2	HMOS	2048	64	32		MC 6805U2	40
EF 6805U3	HMOS	3776	112	32		MC 6805U3	40

Available in plastic, ceeramic, DIL packages or chip-carrier. Ext. temp. range (— 40°C, + 85°C). All software compatible. Interrupt capabilities. Timer.

43, Avenue de l'Europe - 78140 VÉLIZY-VILLACOUBLAY - FRANCE - Tel. (1) 39 46 97 19 - Telex TCSF 204780F - Telecopie (1) 39 46 52 64

NOTES



Gate arrays

BIPOLAR GATE ARRAYS

Application	Part number	Characteristic	Package	Page
LINEAR ARRAYS		- Bipolar linear arrays. - 20 volt max supply voltage. - Standard NPN F_T: 550 MHz - 2 metal layers		
	POLY-USE A	424 components	14, 16, 24 pins DIP	7-5
	POLY-USE G	835 components	22, 24, 28, 40 pins DIP	
LINEAR ARRAYS	POLY-USE K	- Bipolar linear array - 20 V supply voltage - Standard NPN F_T: 3 GHz - 2 metal layers - 906 components	8 to 28 pins package DIL and 14 or 16 pins SO	7-13
High speed gate arrays for TTL and ECL inferface environment		- High speed ECL/TTL gate arrays - Typical gate delay 0.8 ns - 2 metal gates		
	TSC-06	748 gates		
	TSC-12	1339 gates		7-15
	TSC-17	1712 gates		

CMOS GATE ARRAYS

Application	Part number	Characteristic	Package	Page
Low power gate arrays		- HC-MOC gate arrays. - Typical gate delay: 2.5 μs - 1 metal layer - Open drain or 3 state outputs		
	TSGA0400	360 gates		7-23
	0700	648 gates		
	1000	1080 gates		
	1500	1458 gates		
High speed low power gate arrays		- High speed HC-MOS gate arrays. - Typical gate delay: 1.5 μs - 2 metal layers - High latch-up immunity. - Full electrostatic protection.		
	TSGB1000	1120 gates	24 to 68	7-31
	TSGB2000	2128 gates	24 to 84	
	TSGB3000	3264 gates	28 to 120	
	TSGB4000	4256 gates	28 to 124	
	TSGB6000	5880 gates	68 to 144	
	TSGB8000	7872 gates	84 to 208	
	TSGB10000	9776 gates	84 to 208	

THOMSON COMPONENTS SEMICONDUCTEURS

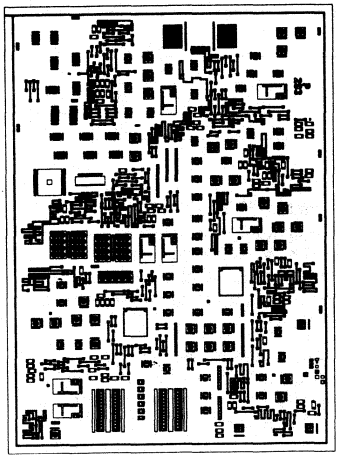
POLY-USE A/G

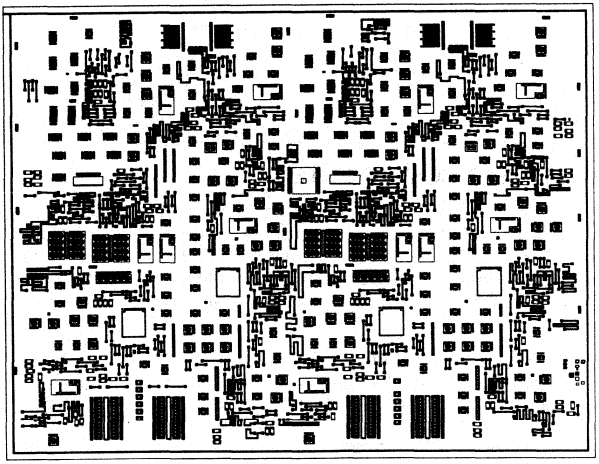
LINEAR COMPONENT ARRAYS

The THOMSON SEMICONDUCTEURS **linear component arrays** are semicustom bipolar integrated circuits that contain an array of uncommitted discrete transistors, resistors and capacitors. A user can interconnect these individual components on second level metal to form a custom linear integrated circuit.

- 20 volt (max) supply operation
- Standard NPN f_T = 550 MHz typ.
- Wide variety of NPN and PNP transistor types on each array
- Base, pinched-base, and emitter resistors (10 ohm to 100K ohm)
- MOS and junction capacitors
- 2 layer metalization for ease of interconnect
- Digitized customer layout sheet for computer-aided routing

A unique feature of the POLY-USE A and G array is the two level metalization which simplifies routing, increases the percent utilization of the components on the array and provides improved electrical characteristics. First level metal is a standard, predefined pattern that provides low resistance distribution of the positive and negative supply voltages across the chip. All custom interconnection and routing is done on second level metal along a predefined routing grid which automatically maintains the proper metal pitch. All contact vias to the individual components and to the first level metal supply voltages lie on intersection points of this grid. This two layer system reduces layout time by a factor of 3 over single layer arrays and up to 90% of the components on the array may be utilized. Computer assisted layout, available as an option, further simplifies and speeds up layout and reduces the risk of errors.





POLY-USE A

- 150 X 106 mil die size (3.8 x 2.7mm)
- 424 components
- 24 pins max
- ≤20 Volt supply max
- 14,16,24 pin plastic or ceramic DIP

POLY-USE G

- 192 X 152 mil die size (4.88 x 3.85mm)
- 835 components
- 40 pins max
- ≤20 Volt supply max
- 22,24,28,40 pin plastic or ceramic DIP

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TABLE I — Summary of Components on POLY-USE A and G

CIRCUIT COMPONENTS	DESCRIPTION		A	G
NPN Transistors	QN1 — Standard 10 mA NPN		46	92
	QN2 — High frequency NPN (rbb' = 150 ohm)		12	23
	QN3 — Low noise NPN (rbb' = 70 ohm)		2	4
	QN4 — 100 mA NPN		2	4
	QN5 — Standard 10 mA NPN with merged PN junction capacitor (C2)		7	12
	Total NPN Transistors		69	135
PNP Transistors	QP6 — Standard lateral PNP (1 mA)		32	60
	QP7 — Multiple lateral PNP (5X)		1	2
	QP8 — Multiple lateral PNP (16X)		2	4
	QP9 — Substrate PNP (1 mA)		1	2
	QP10 — High Current Substrate PNP (5 mA)		2	4
	Total PNP Transistors		38	72
DIODES	D1 — P+N+ Zener		3	0
CAPACITORS	C1 — MOS Capacitor (8 pf)		2	4
	C2 — PN junction (merged with QN5)		7	12
	C3 — P+N+ isolated junction		1	2
	C4 — P+N+ junction (P+ connected to substrate)		1	1
	Total Capacitors		11	19
RESISTORS	P Base	100 ohm	24	45
		220 ohm	34	65
		470 ohm	41	83
		1 K ohm	70	142
		2.2K ohm	62	128
		4.7K ohm	30	59
		10 K ohm	26	53
	Pinched Base	40 K ohm	6	12
		100 K ohm	5	10
	N+ Emitter	10 ohm	12	24
	Total Resistors		310	621
TOTAL COMPONENTS			431	847

THE LINEAR COMPONENTS

The POLY-USE A and G use the same family of NPN and PNP transistors, capacitors and resistors. These components are completely characterized in the **linear component array** Design Manual. A brief description of these components and their features follows.

NPN Transistors: There are five basic NPN transistor types on the arrays. QN1 is a standard NPN vertical structure designed for 10 mA nominal and 30 mA maximum collector current. QN2 is a higher frequency version NPN with two base contacts which reduce the series base resistance (rbb') to 150 ohm typ. QN3 is a low noise NPN that has a rbb' of only 70 ohm typ. The high current NPN, QN4 will handle 100 mA nominal and 300 mA maximum collector current. This transistor contains an extra deep collector diffusion which lowers the VCE(sat) to 250 mV at 100 mA. Finally, QN5 is a standard NPN transistor with an additional P diffusion in the collector which forms a merged PN junction capacitor (C2) off the collector. This is a convenient structure for use in designs requiring Miller capacitance.

PNP Transistors: The arrays have both lateral and substrate PNP transistors. QP6 is a standard lateral PNP designed to handle 1 mA nominal collector current. QP7 is a 5X multiple lateral PNP and QP8 is a 16X lateral PNP. These two PNP transistors contain multiple emitter-collector structures diffused into the same base for higher current handling capability. QP9 is a standard substrate PNP transistor that can handle 1 mA collector current. QP10 is a higher current substrate PNP designed for 5mA nominal collector current.

Diodes: The POLY-USE A also contains 3P+N+ zener diodes with a nominal voltage of 5.5 volts. Additionally, all NPN transistors can be used as zener diodes by connecting the emitter to the collector and using the emitter base junction breakdown for the zener voltage.

Resistors: Three types of resistor construction are used on the arrays; base, pinched-base and emitter. The resulting resistors are arranged in strings of 2 or 3 each in a wide range of standard discrete values. The majority of the resistors on the array are base diffused resistors of either 30 μm or 8 μm width with the values from 100 ohm to 10K ohm. For higher resistance, pinched-base resistors are available in 40K ohm and 100K ohm values. A maximum voltage of 5 volts can be applied to the pinched-base resistors. There are several low value emitter resistors on the arrays of 10 ohm each. Although the initial tolerance on these diffused resistors is not as close as with discrete components, the resistance matching of identical value resistors is superior to discrete versions.

Capacitors: The arrays contain both junction and MOS capacitors which may be used in ac coupling, Miller capacitance or compensation applications. The MOS capacitors are made with a layer of aluminum isolated from an N+ emitter diffusion by a thin layer of oxide. These capacitors have a nominal value of 8 pf which is voltage independent. They also exhibit very low series resistance (high Q). The junction capacitors C3 and C4 have voltage dependent capacitance and may be biased to several hundred picofarads. However, depending on the application, use of these junction capacitors may be limited due to non-negligible leakage currents. The P+N+ junction capacitor (C4) merged with a standard NPN transistor (QN5) provides Miller capacitance capability.

TABLE II — Typical Electrical Characteristics (T_{amb} = + 25°C)

Transistors	NPN (QN1, 2, 3, 4, 5)	Lateral PNP (QP6, 7, 8)	Substrate PNP (QP9, 10)
BVcbo	45 V	45 V	45 V
BVceo	20 V	40 V	45 V
BVebo	6.1 V	30 V	25 V
h_{FE}	140	35	60
f_T	550 MHz	3.5 MHz	14 MHz

Capacitors	MOS (C1)	Junction (C2)	Junction (C3)	Junction (C4)
Nominal value	8 pf	$\frac{5\text{ pf}}{(1 + Vc/0.5)^{0.4}}$	$\frac{30\text{ pf}}{(1 + Vc/0.75)^{0.33}}$	$\frac{100\text{ pf}}{(1 + Vc/0.75)^{0.33}}$
Max. Voltage	±20 V	20 V	2.0 V	2.0 V

Resistors	Base	Pinched Base	Emitter
Initial tolerance	±30%	+100% – 50%	+40% – 30%
Matching (Same value pairs)	±2%	±5%	±10%
Temperature coefficient (typ.)	+0.1%/°C	+0.5%/°C	+0.15%/°C

KIT PARTS

Successful **linear component array** design may require a bread board analysis of the custom circuit prior to committing to layout. A complete set of array components is available in kit part form for this purpose. In addition to kit parts for the various transistors and capacitors on the POLY USE A and G there are also several "linear functions" which have been built and characterized using the array components including a wide band differential amplifier, an active load differential amplifier, a 1.3 volt band gap reference voltage source, a temperature dependent current source and an NPN mixer configuration. All kit parts are packaged in standard 16 pin ceramic DIPs.

TABLE III — Available Breadboard Kit Parts

Kit Part #	Description
KP01	5 standard NPN transistor array (QN1)
KP02	4 standard lateral PNPs (QP6) 1 substrate PNP (QP9)
KP06	1 standard NPN (QN1) 1 standard PNP (PQ6) 1 high current NPN (QN4) 1 high current lateral PNP, 16x (QP8) 1 high current substrate PNP (QP10)
KP054	2 mixer configurations of standard NPNs (QN1)
KP121A	2 low noise NPNs (QN3) 1 wide band differential amplifier circuit
KP122	5 high frequency NPN transistor array (QN2)
KP124A	1 high current lateral PNP (QP8) 1 MOS capacitor (C1) 1 P+N+ capacitor (C4) 1 active load differential amplifier circuit
KP128A	1 P+N+ capacitor (C3) 1 temperature dependent current source circuit 1 wide band differential amplifier circuit 1 band gap 1.3 V voltage source

CIRCUIT MODELING AND SIMULATION

Instead of, or in addition to, bread board evaluation, the customer may want to perform computer analysis of the circuit to verify correct operation over a range of environmental and process variations. To assist with this analysis, a complete set of modeling parameters is available in the **linear component array** Design Manual for each component type on the POLY-USE A and G. The parameters are given for Ebers-Moll and Gummel-Poon bipolar transistor models which are used in simulation programs such as SPICE.

LAYOUT TECHNIQUES

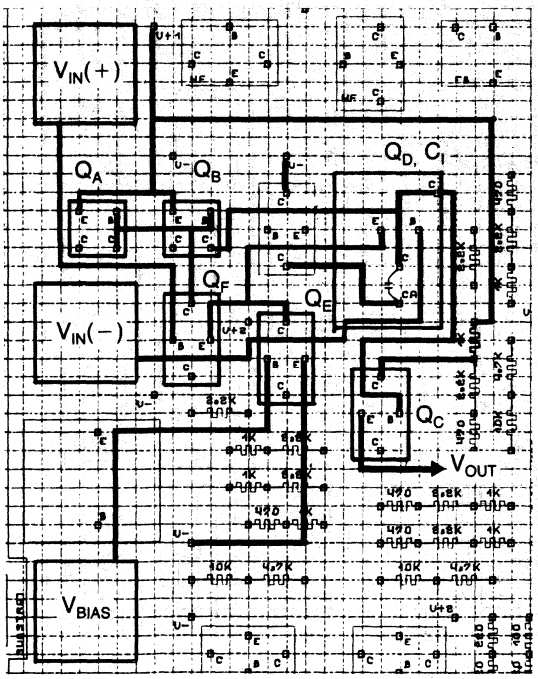
The **linear component arrays** may be routed manually by the customer on routing sheets provided by **THOMSON SEMICONDUCTEURS.** The POLY-USE A and G arrays have been designed to be much easier for the customer to manually interconnect and route than competing single level metal linear arrays. All of the customization of each array is done on second metal. The first level metal pattern is standard on each array, and it provides low resistance distribution of the power and ground buses throughout the array. The POLY-USE G has two separate power buses (+5, +12 volts, for example) and one ground bus. This simplifies the required interconnection on second metal as all supply routing is already provided on first metal. Contact to any of the power supply buses is made by simply routing the interconnect to one of the many V− and V+ contact vias (V−, V+1, V+2 on the POLY-USE G located throughout the array.

Another feature that simplifies the manual layout is the grid on which all interconnect metal is placed. The grid pitch is 31 μm and by specifying the routing along the grid, proper metal spacing and metal width, (16 μm line width is standard), are automatically maintained. Where higher current handling is required (>40 mA) the line width may be drawn wider to indicate the necessary metal width.

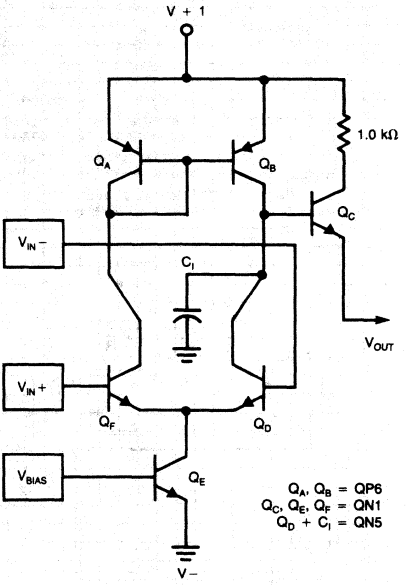
All contact vias to the individual component terminals as well as all power and ground contacts are

located on intersection points on the grid, further simplifying routing. All NPN transistors have two collector contacts which can be used as crossunder connections. There are also contacts to a number of first level metal crossunders throughout the array which are strategically located so as to simplify connections from the center of the array to the bonding pads on the periphery of the chip. These features reduce the average manual layout time by a factor of 3 over similar complexity single level metal arrays. A high percentage of component utilization is also possible on the POLY-USE A and G, typically 80 to 90 percent, and better electrical characteristics should be expected.

LAYOUT EXAMPLE: Differential Amplifier Circuit on the POLY-USE G



Completed Manual Layout on Routing Sheet

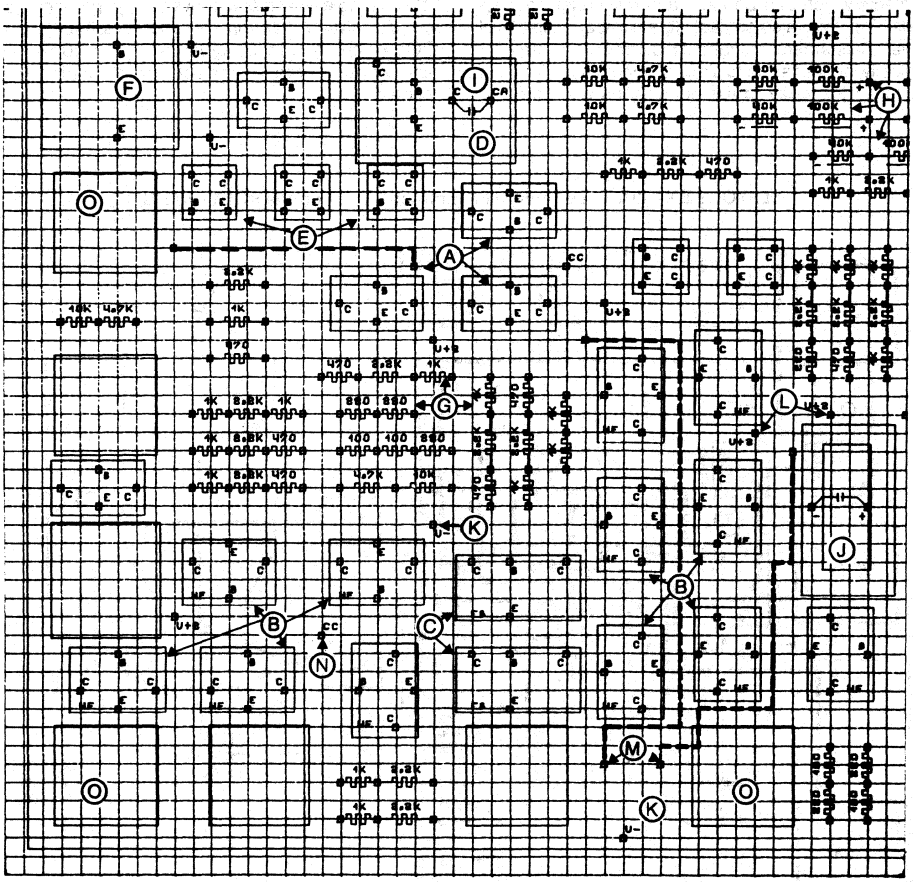


Circuit Schematic

The layout example demonstrates some of the "user-friendly" features of the VSI routing sheets:

- Conveniently located supply and ground contacts (V + 1 and V−) simplify bias connections.
- Collector contacts of the unused NPN transistor form a handy crossunder connection.
- Both C_I and Q_D of the circuit schematic are implemented with the QN5, merged capacitor transistor.

POLY-USE G ROUTING SHEET DETAIL



LEGEND

TRANSISTORS

- Ⓐ — Standard NPN — QN1
- Ⓑ — High Frequency NPN — QN2
- Ⓒ — Low Noise NPN — QN3
- Ⓓ — Standard NPN with Merged PN Junction Capacitor — QN5
- Ⓔ — Standard Lateral PNP — QP6
- Ⓕ — High Current Substrate PNP — QP10

RESISTORS

- Ⓖ — Base Resistor Strings
- Ⓗ — Pinched-base Resistor Strings

CAPACITORS

- Ⓘ — PN Junction Merged with QN5 — C2
- Ⓙ — P^+N^+ Isolated Junction — C3

OTHER CONTACTS

- Ⓚ — Negative Supply Voltage or Ground Contacts
- Ⓛ — Positive Supply Voltage Contacts
- Ⓜ — First Level Metal Crossunder Connections
- Ⓝ — Resistor Tub Biasing Contact
- Ⓞ — Bonding Pad Location.

DESIGN MANUAL

The starting point in developing a custom linear circuit on the POLY-USE A and G is a review of the LINEAR COMPONENT ARRAY DESIGN MANUAL. The Manual contains all the information necessary for a customer to design and layout a custom linear circuit on the POLY-USE A and G arrays including:

- Description of the bipolar processing technology used
- Description of the basic linear component structures and their topology
- Electrical characteristics of the components
- Modeling parameters of the components for computer simulation
- Data sheets for the breadboard Kit Parts
- Explanation of layout and routing procedures
- Manual routing sheets for both the POLY-USE A and G

DESIGN DEVELOPMENT PROCEDURE

The development of a custom linear circuit is a joint effort involving THOMSON SEMICONDUCTEURS and the customer. Typical development work is divided as follows:

The CUSTOMER Tasks:

- Review the Design Manual
- Generate a circuit schematic using POLY-USE A and G components
- Perform breadboard evaluation and/or computer simulation of the circuit
- Layout circuit on routing sheet
- Submit complete Design Package including: completed routing sheet, circuit schematic, breadboard schematic (if applicable), description of circuit operation, application, circuit performance and test specifications

THOMSON SEMICONDUCTEURS Tasks:

- Review the Design Package
- Convert the completed routing sheet to custom metalization mask
- Process wafers and probe to basic process test patterns
- Assemble die into packages
- Test functional prototypes and ship to customer

THOMSON SEMICONDUCTEURS will normally ship the prototypes within 6 to 10 weeks after receiving the customer's Design Package. The testing of the prototypes will be sufficient to ensure proper circuit functionality. After the customer completes evaluation and characterization of the prototypes, **THOMSON SEMICONDUCTEURS** will work closely with the customer to finalize the test programs and procedures for use in volume production.

NOTES

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

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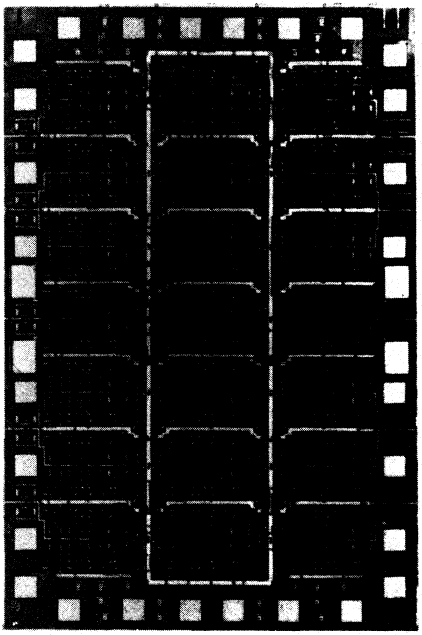
THOMSON COMPONENTS SEMICONDUCTEURS

POLY-USE K

BIPOLAR LINEAR ARRAYS

PRODUCT PREVIEW



The POLY-USE linear arrays are semi-custom bipolar ICs containing an array of uncommitted discrete transistors, resistors and capacitors.
These individual components may be interconnected by the user on the second metal layer to form a custom linear IC.

- **NPN f_T= 3 GHz**
- Two metal layers for ease of interconnection
- Number of components : 906
- Chip size : 7.66 mm^2
- Available in plastic DIL from 8 to 28-pin package
- **Mountable in SO package (14 or 16-pin)**

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TYPICAL ELECTRICAL CHARACTERISTICS (T_{amb} = + 25 °C)

TRANSISTORS

Characteristic	Symbol	Value		Unit
		NPN	PNP	
Collector-base breakdown voltage	$V_{(BR)CBO}$	>25	>25	V
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	>15	>20	V
Early voltage	V_{EA}	>30	>30	V
Current gain	h_{FE}	100	>20	–
Cut-off frequency (unity gain)	f_T	3	–	GHz

RESISTORS

Characteristic	Symbol	Value	Unit
Extrinsic base resistance	R□ Bex	350	Ω/□
P^+ resistance	R□ P^+	60	Ω/□

NUMBER OF COMPONENTS

Number of pads	Transistors		Capacitors	Resistors
	NPN	PNP		
28	188	28	4	686

AVAILABLE COMPONENTS

126	NPN	transistors - Small signal
42	NPN	transistors - 2 emitters connected
10	NPN	transistors - Low noise, high current
28	PNP	transistors - Lateral
4 capacitors - Oxide - Nitrate - 6 pF		
364 P^+ resistors - 100 Ω, 200 Ω, 400 Ω, 800 Ω 322 Base resistors - 1 kΩ to 16 kΩ		

- The two-layers system reduces lay-out time by a factor of 3 compared to single layer arrays and up to 90 % of components on the array may be used.
- Successful linear component array design may require a bread board of the circuit prior to committing the design lay-out.
- A complete set of array components is available in kit parts for this purpose.

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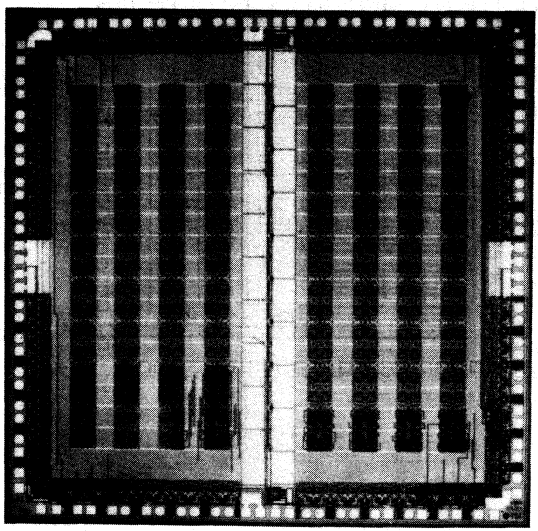
THOMSON COMPONENTS SEMICONDUCTEURS

TSC06/12/17
BIPOLAR MACRO ARRAYS

ADVANCE INFORMATION



Two standard electrical interface environments have evolved for digital integrated circuits, TTL and ECL. TTL compatible products such as LS, FAST, CMOS, NMOS, etc., represent the majority of digital ICs in use today. However, ECL products are necessary for applications requiring the highest available switching performance. Interfacing these two incompatible environments has usually required dedicated level translation circuits as few logic ICs can operate in both environments simultaneously.

The TSC Bipolar MACRO ARRAYS exceed present offerings in compatibility, user friendliness, flexibility and performance. One comprehensive macro library and one set of industry standard CAD software tools support the entire family of arrays. The user may input a design in a variety of ways, from submitting a logic schematic to inputting a complete CAD design file via a remote terminal. Each array can be configured to operate in a TTL and/or ECL environment and all array pins can be configured as inputs or outputs providing maximum design flexibility. The internal macro logic is implemented with high performance series gated ECL circuits. These MACRO ARRAY features give the user a custom design solution with lower risk, lower cost and shorter design cycle than a full custom integrated circuit.

- TSC06 : 748 gates, TSC12 : 1338 gates, TSC17 : 1712 gates
- Typical internal equivalent gate delay : 0.8 ns
- Typical ECL I/O buffer pair delay : 2.0 ns
- Typical TTL I/O buffer pair delay : 8.0 ns
- All I/O cells may be configured as input, output, or bidirectional pins.
- True 10K ECL compatible interface
- Optional 2 kΩ on-chip pulldown resistor for direct wiring of ECL.
- True LS-TTL compatible interface including 8 mA or 16 mA outputs and three-state or open collector output options.
- High performance, oxide-isolated, 2 layer metalization process technology.
- Temperature range : −55 to + 125°C
- Identical macro library for all three arrays.
- Complete set of VAX/VMS and workstation CAD tools for the entire family.
- Commercial, Industrial and full MIL-STD-883C level B screening available.

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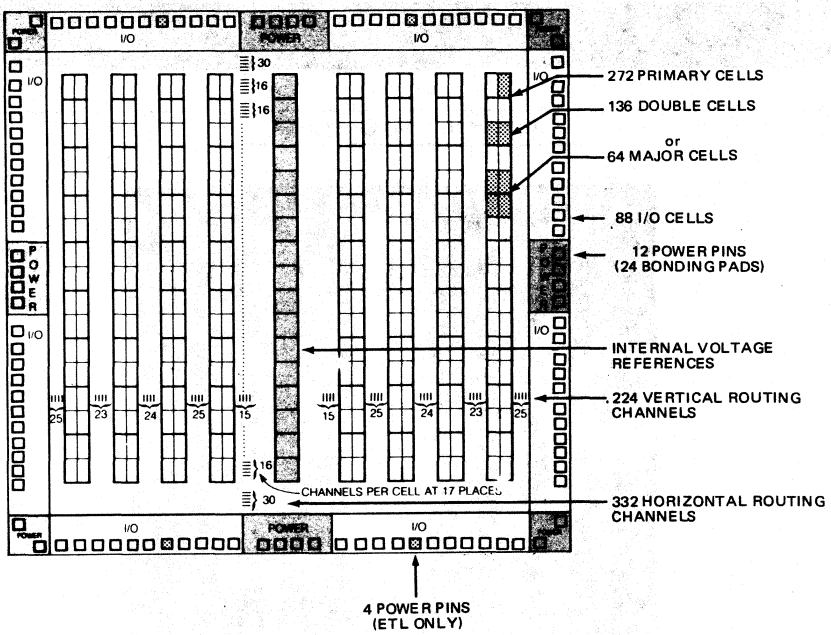
FIGURE 1



INTERFACE MODE

Each bipolar MACRO ARRAY can be designed to operate in either a TTL, ECL or combined TTL and ECL interface environment. Prior to generating a custom logic design on the arrays, the user selects the array size and the array interface mode. Selection of the interface mode determines the fixed metal pattern for all power busing and the assignment of supply voltages to package pins. The mode selection also determines which group of I/O Macros will be used. Selection of macros for primary, double, or major macro functions is not affected by the interface mode or array size. The ECL and TTL modes do not restrict the number of I/O's available or location. The ETL mode is restricted in that ECL I/O's and TTL I/O's are available on two sides respectively. In addition, four ECL I/O locations are eliminated because additional power pins are necessary. The number of available I/O's for each mode is listed below.

POWER

The power supply pins are located at the corners and centers of array periphery. Each power pin ties to two adjacent building pads. The number and assignment of supply voltages to the power pins depends on the interface mode. The power buses for internal array and I/O buffers are separated. This allows for improved array and system performance. The internal ARRAY is referenced to ECL power supply levels in both the ECL and DUAL interface mode and to TTL power levels in the TTL interface mode.

Interface mode	Number of I/O's		
	TSC06	TSC12	TSC17
ECL	52	72	88
TTL	52	72	88
DUAL		ECL 32 TTL 30	ECL 40 TTL 44

Mode	4–5.2 V	0 V	5.0 V
ECL	X	X	
TTL		X	X
DUAL	X	X	X

THE TSC BIPOLAR MACRO ARRAYS

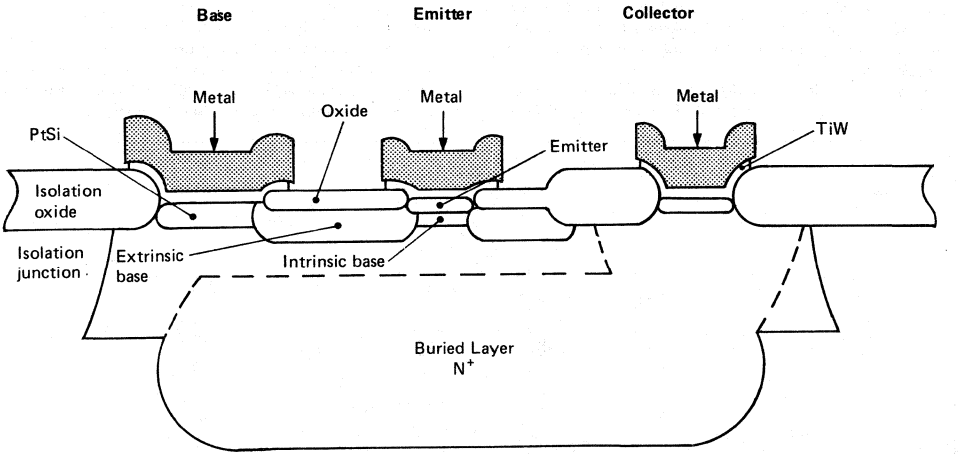
	TSC06	TSC12	TSC17
Primary cells	108	210	272
I/O cells	52	72	88
Max. Equivalent Gates (1)	748	1338	1712
Typical Array power	750 mW	1.5 mW	2.0 mW

(1) - Assumes that all array cells are utilized at an average of 5 equivalent, 2-input gates per primary cell and 4 equivalent gates per I/O cell.

PROCESS DESCRIPTION

The TSC bipolar MACRO ARRAYS are fabricated on THOMSON SEMICONDUCTEURS' HBIP2 high performance two metal process.

This technology provides improved speed power products over convention junction isolated product.

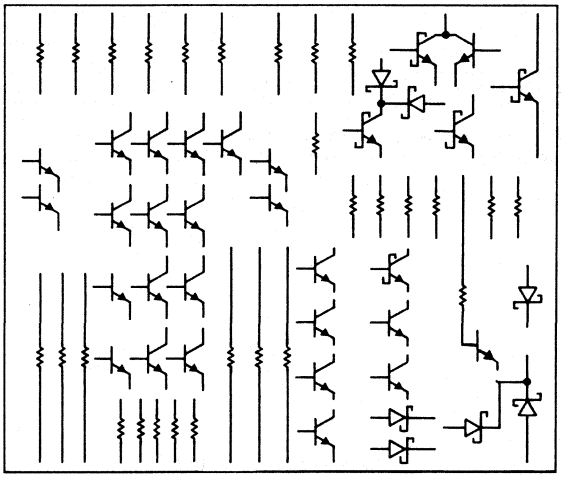


I/O MACRO CELLS

I/O macro cells are located around the periphery of the array. Each I/O cell has the required components to operate in either a ECL or TTL mode as an input or output. The I/O cell contains 28 transistors, 7 schottky diodes and 28 resistors. A schematic representation is shown in figure 2.

All signals to and from array must pass through an I/O cell for level translation and/or current drive capability. Each I/O location has a fixed bonding pad location allowing for single input and single output macros.

FIGURE 2



PRIMARY CELLS

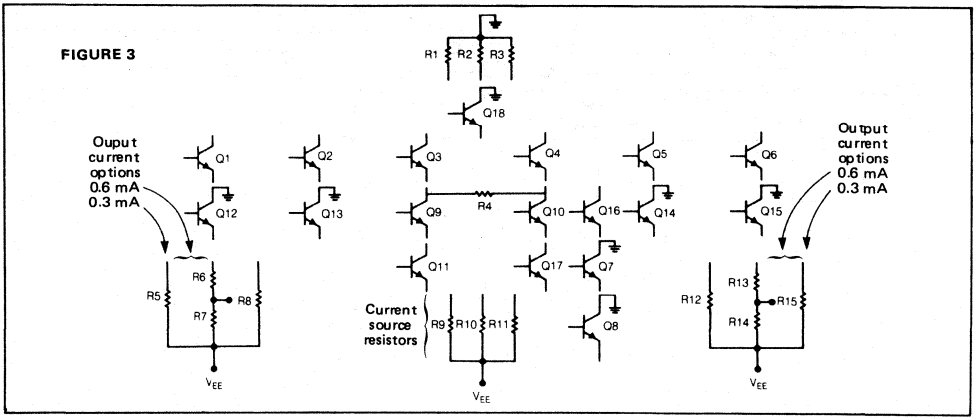
A primary cell is the basic logic building block in the internal array. Each primary cell contains 18 transistors and 15 resistors. A schematic representation is shown in figure 3. Logic functions are formed using first level metal interconnects. To incorporate more complex functions, adjacent cells are combined to form double cell or four symmetrical cells are combined to form a major cell.

All internal logic is configured with ECL logic structures using series gating. Other internal signals use one set of ECL logic levels. Some competing products use upper and lower logic levels which increases design risk.

The primary cell inputs can only be driven by an I/O cell or another primary cell and not from the external environment. Three drive levels are available from each primary output by paralleling resistors on the emitter follower : 0.300 mA and 0.600 mA. The outputs cannot be used as off-chip output drivers.

This primary cell has an increased component density over competing array product. This allows for more efficient utilisation of available cell locations.

FIGURE 3



PRIMARY CELL

CELL LIBRARY

I/O MACROS : to assist the designer in secreting the appropriate I/O macro, they have been given symbolic names which indicates logic function, fanout capability and interface mode :

First character : **I** for Input macro
O for Ouput macro
Second character : A number indicating logic function
Third character : Fanout capability (**N**-Normal, **F**-Fast)
Fourth character : Interface mode
(**E**-ECL, **T**-TTL, **D**-DUAL)

I/O macro	Macro description
I 1ND	TTL input LATCH
I 1NE	ECL input LATCH
I 1NT	TTL input LATCH
I 2ND	TTL input buffer/converter
I 2NE	ECL input buffer/converter
I 2NT	TTL input buffer/converter
I 3ND	TTL chip enable
I 3NT	TTL chip enable
I 4NE	ECL latch clock input
O INT	TTL bidirectional buffer
O 2ND	TTL output with LATCH
O 2NE	ECL output with LATCH
O 2NT	TTL output with LATCH
O 3ND	3 input OR with TTL output
O 3NE	3 input OR with ECL output
O 3NT	3 input OR with TTL output
O 4ND	3 input NOR with TTL output
O 4NE	4 input NOR with ECL output
O 4NT	4 input NOR with ECL output
O 5ND	2 input AND with TTL output
O 5NE	2 input AND with ECL output
O 5NT	2 input AND with TTL output
O 6ND	2 input NAND with TTL output
O 6NE	2 input NAND with ECL output
O 6NT	2 input NAND with TTL output

INTERNAL MACROS : The designer uses the same internal macros regardless of the interface mode. These macros have mnemonic names to assist the designer in the selection of macro function.

First character : define the logic function
AR - combined AND/OR
D - D Flip Flop
L - Latch
M - Mux
N - Inverter
R - OR
X - Exclusive OR
Second character : Inverter specifics about logic function.
Last character : Defines fanout ability.
N-Fanout up to 6 (0.3 mA)
F-Fanout up to 10 (0.6 mA).

Logic macro	Macro description
AR1N	3 input OR-AND
AR2N	2 wide 3-input active low AND-OR/NOR
AR3N	3 input OR-AND/NAND with 3 active low enable
AR4N	3 wide active low AND-OR/NOR
F1N	Positive edge D flip-flop with asynchronous reset
F2N	Positive edge D flip-flop with asynchronous set and reset
L1N	Negative clock transparent LATCH with reset
L2N	Positive clock transparent LATCH with reset
L3N	2 bit LATCH with asynchronous reset and active low enable
M1N	2 to 1 MUX with OR select and active low enable
M2N	2 to 1 MUX with OR select and active high enable
M3N	4 to 1 MUX
M4N	4 to 1 MUX with active low enable
M5N	DUAL 2 to 1 MUX
M7N	DUAL 2 to 1 MUX with common select
NR2N	4 input OR/NOR
NR2N	DUAL 3 input OR - 3 input NOR
NR4N	6 input OR/NOR
NR5N	DUAL 3 input NOR with 2 common input
NR7N	7 input OR-NOR
NR8N	12 input OR-NOR
R1N	DUAL 3 input OR
R2N	DUAL 3 input OR with 2 common inputs
X1N	3 input OR-exclusive OR/NOR
X2N	2 input OR-exclusive OR with active low
X3N	4 input ODD parity checker
X4N	4 input exclusive OR/NOR
X5N	2 input NOR-exclusive OR/NOR.

A.C. PERFORMANCE

The cell library provides the maximum delay time for worst case technology, 25°C ambient and $V_{CC} = -5.2$ V. Worst case performance can be calculated using the formula provided in the design manual or the CAD system.

The CAD system provides the designer with both a prerouting and routed A.C performance simulation. The prerouting simulation is based upon statistical loading estimates based upon fanout.

The designer can also calculate the typical and best case performance by multiplying worst case performance by 0.5 and 0.7 respectively.

The designer will be able to select the speed power products of an internal macro. Each function, where possible, will be released using a 0.300 mA and 0.600 mA source current. By doubling the power, the designer is able to obtain a 30 % performance improvement.

Table 1 provides a summary of typical performances for selected internal and I/O logic functions. The internal macros performance does not vary based upon interface mode.

TABLE 1 – TYPICAL TIMING DELAYS

INTERNAL MACRO (1)	TYPICAL DELAY
3 Input gate	1.8 ns
3 Input AND/OR	2.0 ns
Flip-flop	2.7 ns
Latch	2.2 ns
Mux	2.0 ns
INPUT MACRO (1)	
Latch (ECL)	3.9 ns
Latch (TTL)	4.2 ns
Buffer (ECL)	2.2 ns
Buffer (TTL)	2.7 ns
OUTPUT MACRO (2)	
Latch (ECL)	3.5 ns
Latch (TTL)	8.4 ns
Buffer (ECL)	2.1 ns
Buffer (TTL)	8.1 ns

(1) FANOUT = 3, routing metal 2.5 mm
(2) ECL load 50 Ω to – 2 V,
TTL load = 300 Ω.

PACKAGING OPTIONS

Package Type	Leads	TSC06	TSC12	TSC17
Ceramic DIP	28	X		
	40	X	X	
	48	X	X	
	64	X	X	X
Plastic DIP	28	X		
	40	X		
	48	X		
	64	X		
Leadless Ceramic Chip Carrier	68	X	X	X
	84		X	X
Pin Grid Array	68	X	X	X
	84		X	X

Other packages available on request.

QUALITY LEVELS

In addition to the standard quality procedures for commercial grade product, THOMSON SEMICONDUCTEURS offers a variety of extended temperature ranges and high reliability screening levels for the TSC MACRO Arrays. All extended screening is performed at THOMSON SEMICONDUCTEURS' Military and Spatial Division facility in France, which is completely equipped with state-of-the-art assembly, electrical test and environmental stress equipment. The Military and Spatial Division is dedicated to performing quality control and reliability assurance for all THOMSON SEMICONDUCTEURS integrated circuits for military and space applications.

AVAILABLE SCREENING LEVELS

Level	Description
Standard	Commercial Temp. Range 0° to + 70°C Industrial Temp. Range –40° to + 85°C Military Temp. Range –55° to + 125°C
D	Standard Level with Burn-in
B/B	Full MIL-STD-883C, Class B Screening
G/B	MIL-STD-883C Without Constant Acceleration or Temp. Test, PDA < 10 %.

CAD SYSTEM

All of the THOMSON SEMICONDUCTEURS Array Products are supported by a fully automated VAX/VMS based CAD System. The CAD System provides a complete set of industry standard design, layout and verification tools to ensure fast, error-free design of the TSC MACRO ARRAYS. The CAD System resides at THOMSON SEMICONDUCTEURS Design Center and is accessed with a Tektronix 4109 (or equivalent) graphics terminal.

The CAD System can also accept verified netlists from a variety of popular engineering workstations, including Daisy® , Valid® , Mentor®, and IBM PC-XT® - based workstations that are equipped with the TSC Series Macro library. The key components of the THOMSON SEMICONDUCTEURS CAD System are :

Schematic Capture	SDS®
Netlist Extraction	SDS®
Logic Simulation	HILO®
Timing Analysis	HILO®
Fault Grading	HILO®
Tester Program Interface	HILO®
Automatic Placement and Routing	GARDS®
Interactive Placement and Routing	GARDS®
Design Rule Checking	GARDS®
Automatic Mask Generation	GARDS®

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Design entry is easily accomplished with the SDS menu driven software and a graphics terminal (Tek 4109). The SDS generated logic schematic is converted to a netlist and checked for logic design rule violations (excessive fanout, for instance). The netlist is then automatically converted to HILO simulation format.

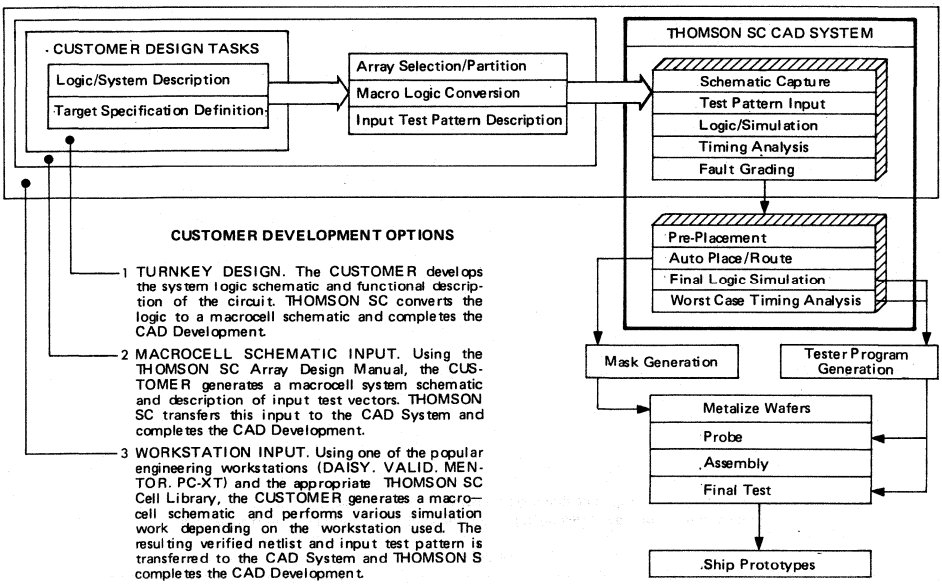
The HILO simulation program performs logic simulation based on the user defined input test pattern and timing analysis using pre-routing statistical load capacitances for delay calculations. HILO also can be used to perform fault grade analysis of the input test pattern.

The GARDS program is used to automatically place and route the array's cell logic as described in the SDS netlist. GARDS also has an interactive mode that allows cell or I/O preplacement and manual routing to optimize critical paths if necessary. After placement and routing is completed, HILO timing analysis can be performed again to determine worst case critical path delays using the actual interconnect length and fanout capacitances.

When the array design work is completed on the CAD System, the HILO simulation output is automatically converted to a tester program tape and the GARDS place and route file is converted to a graphics data base for mask generation. These two data bases are then sent to the factory for prototype generation.

DESIGN DEVELOPMENT PROCEDURE

The design of an array option is a joint development effort involving THOMSON SEMICONDUCTEURS and the CUSTOMER. THOMSON SEMICONDUCTEURS offers a very flexible interface to the CAD System, providing the CUSTOMER with several options in performing the various CAD Development Procedures as shown below :



NOTES

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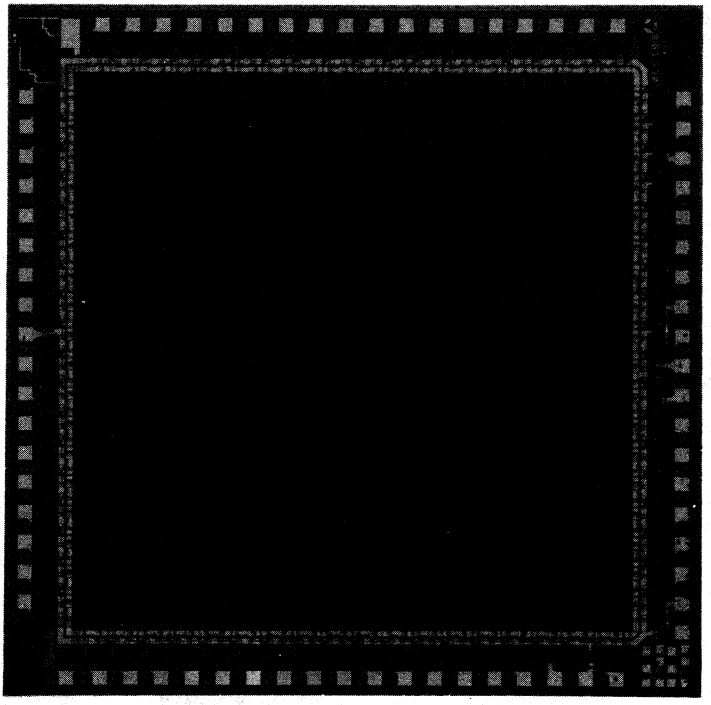
THOMSON COMPONENTS SEMICONDUCTEURS

TSGA SERIES

3 μ/1 METAL HCMOS GATE ARRAYS



THOMSON SEMICONDUCTEURS high-speed Gate Arrays, developed in silicon-gate CMOS technology (3-micron drawn gate length), offer high density, high performances and low power consumption. Complexity ranges from 360 to 1458 cells, each cell equivalent to a 3-input NAND or NOR gate. I/O pin count ranges from 36 to 72.

Using very effective CAD tools such as an interactive graphics system to generate the logical description, efficient logical simulation software, automatic placement and routing software allow THOMSON SEMICONDUCTEURS to offer low cost products and short development cycles.

FEATURES :

- Silicon gate 3 microns (drawn) HCMOS 1 Technology
- P and N transistor effective channel length : 1.9 microns
- Single layer metal interconnection
- TTL-LS speed - 2.5 ns through a 2 input NAND gate, fan-out = 3, $T_A = 25°C$ and $V_{DD} = 5$ volts
- Maximum switching frequency = 50 MHz
- Complexity ranging from 360 to 1458 cells
- Highly flexible I/O buffers range from 36 to 72 as input, output, bidirectional, or power pads
- CMOS or TTL compatible I/O (1 TTL or 4 TTL-LS loads)
- Open drain or 3 state outputs
- Analog functions such as current mirrors, differential amplifiers, and Power on Reset
- All inputs and outputs protected from overvoltage and latchup
- Fully supported by THOMSON SEMICONDUCTEURS CAD system
- Extensive cell libraries
- Commercial and military versions (- 55°C, + 125°C)
- DIL and chip-carrier packages, ceramic or plastic.

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ARRAY SELECTION CHART

Designation	Number of 3-input gates	Number of transistors	Number of pads	Number of I/O buffers *	Smallest usable package
TSGA0400	360	2196	38	36	14
TSGA0700	648	3936	50	48	24
TSGA1000	1080	6542	64	62	24
TSGA1500	1458	8822	74	72	24

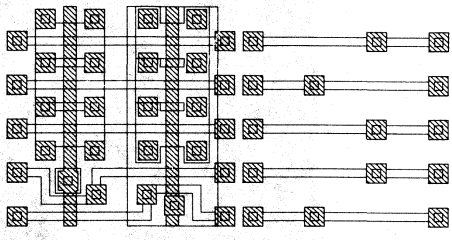
(*) Including Power Supply Pads

PRODUCT DESCRIPTION

BASIC CELL CIRCUIT SYSTEM

The basic cell consists of :

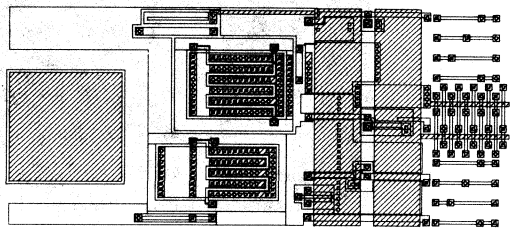
- 3 N channel and 3 P channel uncommitted transistors which share common sources, drains and gates
- 5 polysilicon interconnect channels
- 2 polysilicon feed-thru
- 7 free metal interconnect channels (vertical)
- 5 free metal interconnect channels (horizontal)
- Metal supply voltage distribution.



BASIC I/O SYSTEM

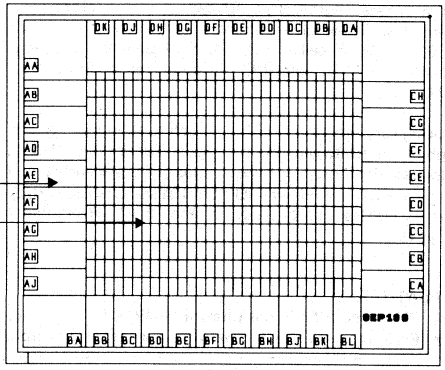
All I/O buffer cells consist of :

- Input protection network (resistor and 2 clamping diodes)
- One large N-channel transistor
- One large P-channel transistor
- One medium P-channel transistor
- Two high impedance transistors for pull-up and pull-down applications.



TYPICAL TOPOLOGY

The internal array consists of matrix of basic cell arranged in columns. The periphery contains the basic I/O buffer cells used to implement the interface between the internal area and the outside environment.



The TSGA0400 array organization.

GATE ARRAY MACRO LIBRARY

- Macrocells are the simplest building blocks available to the user. To specify his logic, the user can build elements of greater complexity from macrocells. These elements are called MACROFUNCTIONS.

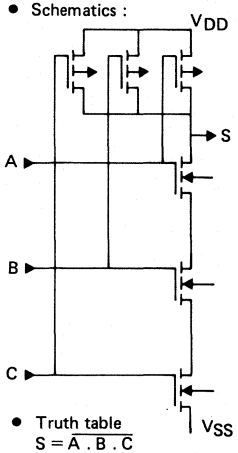
- PRESENT MACROCELL LIBRARY

MACRO	DESCRIPTION	CELL COUNT
INV	Inverter	1
INV2	Dual inverter	1
NO2	2 Input NOR	1
OR2E	2 Input OR	1
NO2I	2 Input NOR + Inverter	1
NA2	2 Input NAND	1
AN2	2 Input AND	1
NA2I	2 Input NAND + Inverter	1
NO3	3 Input NOR	1
NA3	3 Input NAND	1
NO4	4 Input OR	2
NO42	4 Input NOR + 2 Input NOR	2
NO44	Dual 4 Input NOR	3
NA4	4 Input NAND	2
NA42	4 Input NAND + 2 Input NAND	2
NA44	Dual 4 Input NAND	3
ANO	2 Input AND NOR	1
ONA	2 Input OR NAND	1
OEX	2 Input Exclusive OR	2
NOEX	2 Input Exclusive NOR	2
TSI	Internal Three states	1
BUIT	Internal Buffer	1
BNI	Internal Buffer	1
TTC	Internal TTL CMOS LEVEL Shifter	6
REF	Stuck at "0" and "1"	1
LA	Latch	2
LAR	Latch with Reset	2
FF	D Flip Flop	4
FFR	D Flip-Flop with Reset	4
FFS	D Flip-Flop with Set	4
FFSR	D Flip-Flop with Set and Reset	6
CSR	Toggle Flip-Flop with Reset	6
MU2	2 to 1 multiplexer	1
MU4	4 to 1 multiplexer	4
PE	Direct input	
PEBC	Direct Input and Internal Buffer	
BET	TTL Compatible input buffer	
BEC	CMOS Compatible input buffer	
BST	TTL Compatible output buffer	
B3T	TTL Compatible 3-state output buffer	
B3B	Bidirectional Buffer	
PU	P transistor output	
OD	N transistor output	
PLOV$_{DD}$	V_{DD} power supply pad	
PLOV$_{SS}$	V_{SS} power supply pad	

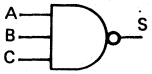
- LIBRARY EXTENSION
  A MACROFUNCTION library including a lot of TTL-LS standard functions will be soon made available to customers.

EXAMPLE OF MACRO DESCRIPTION (for complete description, refer THOMSON SEMICONDUCTEURS HCMOS Gate Array Manual).

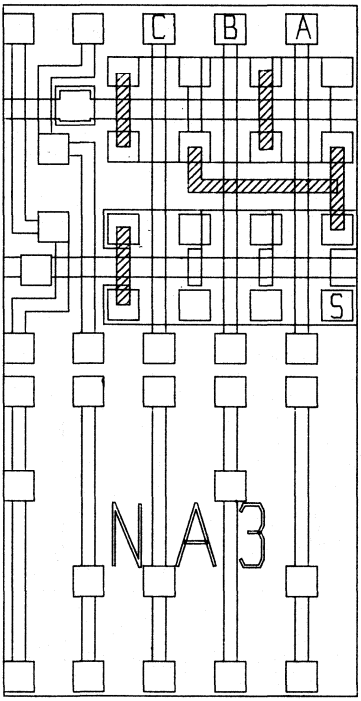
- Name : 3 Input NAND
- Type NA3
- Schematics :



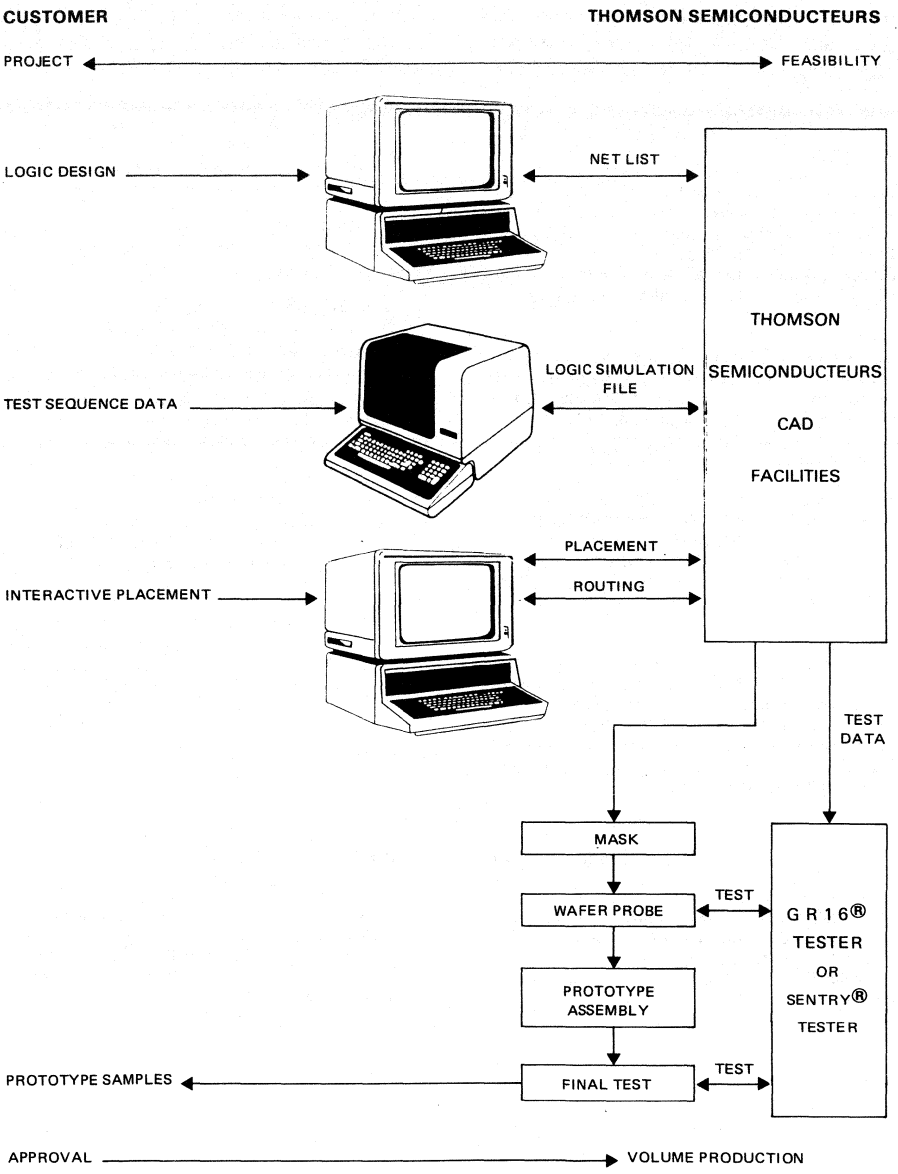
- Symbol



- Truth table
  $S = \overline{A \cdot B \cdot C}$
- Fan In
  A, B, C : 0.1 pF
- Propagation delay
  $t_{PHL} = 0.6 + 6.8 \times C$
  $t_{PLH} = 1 + 10 \times C$
- Topology



TYPICAL DEVELOPMENT INTERFACE



CUSTOMER INTERFACE OPTIONS

A typical gate array development flowchart is shown page 5 ; THOMSON SEMICONDUCTEURS offers a full development program for customized arrays from specifications, logic diagrams, timing contraints, truth tables supplied by the customer.

There are different interface options available to the customer from THOMSON SEMICONDUCTEURS in the development of gate arrays :

- Customers with little experience in semi-custom circuit development, or experienced users with limited in-house capabilities can interface with THOMSON SEMICONDUCTEURS. By supplying it only with product specifications, THOMSON SEMICONDUCTEURS will make the complete design and will provide 20 tested samples.

- The customer supplies, based on a THOMSON SEMICONDUCTEURS library description, a logic diagram and test vectors. In this case THOMSON SEMICONDUCTEURS will handle data capture, placement and routing, mask generation, test program generation and will provide the customer with 20 tested samples.

- The customer has suitable in-house design capabilities. He works with THOMSON SEMICONDUCTEURS CAD or in-house compatible CAD. In this case, the user will supply to THOMSON SEMICONDUCTEURS a test file and a logic file for placement and routing. THOMSON SEMICONDUCTEURS will provide 20 tested samples.

- The customer has suitable in-house design capabilities which include CALMA® format or DAVIDMANN compatible pattern generator (PG) tape generation. In this case, THOMSON SEMICONDUCTEURS will supply all necessary information, such as gate array database or interconnect rules, and provide the customer with 20 tested samples.

CAD SYSTEM FEATURES

THOMSON SEMICONDUCTEURS has made available complete CAD software package in order to insure fast and efficient gate array development. All phases in the development process are automated :

- SCHEMATICS CAPTURE : an interactive graphics system is used to create and edit user symbols and schematic diagrams.
  Diagrams are stored in a centralized design data base. This software supports the hierarchical design.

- SIMULATION : the logic description is automatically extracted from the centralized design data base for the logic simulator.

- PLACEMENT and ROUTING : a compatible net list is extracted from the centralized design data base and used for both interactive placement, and fully automatic complement placement and routing.

  If necessary, manual pre-routing and end-routing are performed interactively. Note that manual editing is on-line checked with the centralized data base.

- TEST SEQUENCE GENERATION : compressed functional test patterns based on the results of the logic simulation are automatically generated. DC parametric tests are merged with compressed functional patterns for a full dynamic test program used in the GR16® tester.

- DAVIDMANN TAPE GENERATION : the placement and routing results are used to generate a metal interconnect mask. A program automatically performs a DRC and generates a Davidmann pattern tape.

THOMSON SEMICONDUCTEURS ORGANIZATION

THOMSON SEMICONDUCTEURS has set up a specific organization fully dedicated to the design and the support of semicustom circuits, with full capability to support customers either directly or through local representatives or subsidiaries.

This specific organization, mainly devoted to gate array development and support, both in HCMOS 1 and BIPOLAR technologies includes GR16® and LTX80® testers, CALMA® GDSII system, DEC VAX II/780® computer and prototyping facilities.

ABSOLUTE MAXIMUM RATINGS (referenced to V_{SS})

Rating	Symbol	Min	Max	Unit
DC supply voltage	V_{DD}	- 0.5	7	V
Input voltage	V_I	- 0.5	V_{DD} + 0.5	V
Storage temperature	T_{stg}	- 65	+ 150	°C
Max operating current	$I_{DD\ max}$	–	50	mA

RECOMMENDED OPERATING CONDITIONS (referenced to V_{SS})

Rating	Symbol	Min	Max	Unit
DC supply voltage	V_{DD}	4.5	5.5	V
Input voltage	V_I	0	V_{DD}	V
Operating temperature range	T_{amb}			°C
Military		- 55	+ 125	
Industrial		- 40	+ 85	
Commercial		0	+ 70	

DC CHARACTERISTICS

V_{DD} = 5 V ± 10 %, military temperature range (unless otnerwise specified)

Characteristic	Symbol	Min	Max	Unit
Low level input voltage	V_{IL}			V
TTL input		–	0.8	
CMOS input		–	0.9	
High level input voltage	V_{IH}			V
TTL input		2	–	
CMOS input		V_{DD} – 1.4	–	
Input current	I_{IN}			µA
TTL or CMOS		- 1	+ 1	
with pullup $V_{IN} = V_{SS}$		- 150	–	
with pulldown $V_{IN} = V_{DD}$		–	150	
Low level output voltage	V_{OL}			V
TTL output				
T_{amb} = + 85°C, I_{OL} = 2.4 mA		–	0.5	
T_{amb} = + 125°C, I_{OL} = 1.6 mA		–	0.4	
CMOS output (I_{OL} = 1.6 mA)				
T_{amb} = + 85°C		–	0.33	
T_{amb} = + 125°C		–	0.4	
High level output voltage	V_{OH}			V
TTL output				
T_{amb} = + 85°C, I_{OH} = -2 mA		2.7	–	
T_{amb} = + 125°C, I_{OH} = -1.6 mA		2.5	–	
CMOS output (I_{OH} = -0.8 mA)				
T_{amb} = + 85°C		3.84	–	
T_{amb} = + 125°C		3.7	–	

SWITCHING CHARACTERISTICS

Specified at V_{DD} = 4.5 V, T_{amb} = 25°C, technology worst case, all fan-out = 3.

TYPE	t_{PHL} (ns)	t_{PLH} (ns)
INV	2.3	3.5
NO2	3	6.7
OR2E	5.3	10.2
NA2	3	4.6
AN2	5.3	8.1
NA3	4.1	5.3
NO3	3.5	9.6
NA4	5.3	5.9
NO4	3.5	2.6
ANO	4.5	6.5
ONA	3.5	7.5
OEX	8.6	7.1
NOEX	6.6	6.7
BUIT	1	1.9
TSI	3.5	5.9
MU2	2	1.9
MU4	5.3	7.5
FF (Q)	5.7	5.2
FF (QB)	7.7	9.7
BET	2.1	7
BEC	1.6	2.3
BST	10.4	18.6 (30 pF load)

PACKAGING

- Table below shows a list of the preferred packages for the HCMOS 1 gate array series.
- Under special conditions THOMSON SEMICONDUCTEURS HCMOS 1 gate arrays can also be purchased in wafer or die form, or with special packaging if required.

Package type	Lead count	TSGA0400	TSGA0700	TSGA1000	TSGA1500
Ceramic DIL	14	X			
	16	X			
	18	X			
	24	X	X	X	X
	28	X	X	X	X
	40	X	X	X	X
	48		X	X	X
	64		X	X	X
Plastic DIL	14	X			
	16	X			
	18	X			
	24	X	X	X	
	40	X	X	X	X
	48		X	X	X
	64		X	X	X
SURPICOP Leaded plastic chip-carrier	44	X	X	X	X
	68		X	X	X
TRICECOP Leadless ceramic chip-carrier	24	X	X		
	28	X	X		
	44	X	X	X	X
	52		X	X	X
	68		X	X	X
	84				X
Pin Grid Array	68			X	X
	84				X

These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

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THOMSON COMPONENTS SEMICONDUCTEURS

TSGB SERIES
2 μ/2 METAL HCMOS GATE ARRAYS
1000 TO 10000 GATES

SEMICUSTOM PRODUCTS

TSGB SERIES - 2 μ/2 METAL GATE ARRAYS 1000 TO 10000 GATES

HCMOS FAMILY

FEATURES

- Gate delay : 1.5 ns typical with fan out of 2.
- Speed : up to 40 MHz operating frequency.
- Advanced HCMOS technology :
  - 2 μ Design rules.
  - 2 metal layers.
  - twin tub CMOS process.
- Operating temperature range
  - commercial : 0 to 70°C
  - industrial : - 40 to + 85°C
  - military : - 55 to + 125°C.
- High latch-up immunity
  ± 500 mA (typ)
- Full Electrostatic Protection
  ± 2000 V (min)
- Gate Count : Up to 10000 gates.
- Power Supply :
  - maximum ratings : - 0.5 to + 7 V.
  - operation : 3 to 6 V.
- Input/Output Cells :
  - comptability : TTL or CMOS levels.
  - configurability : individually programmable as driver receiver, 3 state, bidirectional, or power pad.
- Macro cell library :
  - hard macros : 70 different combinational/sequential SSI/MSI functions.
  - soft macros : more than 150 described soft macros.
- CAD software support :
  - fully integrated THOMSCAD™ design automation system.
  - up to 95 % silicon use with 100 % auto place and route.

TSGB 2 μ/2 METAL LAYER HCMOS SERIES

Part Number	Gate Count (1)	I/O Pads	V_{DD}/V_{SS} Pads	Total Pads (2)	Package Pin options
TSGB 01000	1120	56	12	68	24 to 68
TSGB 02000	2128	76	12	88	24 to 84
TSGB 03000	3264	96	12	108	28 to 120
TSGB 04000	4256	108	12	120	28 to 124
TSGB 06000	5880	132	12	144	68 to 144
TSGB 08000	7872	168	16	184	84 to 208
TSGB 10000	9776	192	16	208	84 to 208

Note 1 : 1 gate is the equivalent of a 2 input NAND or NOR gate (2 N and 2 P channel transistors).

Note 2 : The pad count is for the chip only. The final device pin count is package and application dependent with larger pin devices tending to have additional power and ground pins.

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TECHNOLOGY

The TSGB Series (1000 to 10000 gates) from Thomson semiconducteurs uses an advanced silicon gate dual metal layer/twin tub HCMOS technology.

This process achieves operating speed of the circuit up to 40 MHz with the inherent low power consumption of CMOS technology.

Four levels of customization are required to convert the standard array to a custom part. The levels are :

- contact : 1st level metal to diffusion and polysilicon.
- 1st level metal : macro cell wiring and horizontal wiring channel interconnect.
- via : contact between 1st and 2nd level metal.
- 2nd level metal : global power distribution and vertical wiring channels over the basic cell.

ARCHITECTURE

The 2 μ/2 metal HCMOS Thomson semiconducteurs gate arrays are organized as dual rows of uncommited logic gates (2 N and 2 P channel transistors per gate) separated from each other by an interconnect area reserved for Metal 1 routing. Additional routing is provided in Metal 2.

The dual row architecture allows an high efficiency in large macros design, and an high routability capability.

The internal array is surrounded by multi-function peripheral cells providing adequate interface with external circuitry.

The Figure 1 shows the array architecture of the TSGB 1000 matrix.

BASIC GATE

The Figure 1 shows the layout of the basic gate structure. The basic logic gate consists of 2 pairs of N and P channel MOS transistors. It is potentially equivalent to a 2 input NOR or NAND.

The P channel transistors have a larger size than N channel transistors providing then a good symetry on rise and fall times of the gate.

PERIPHERAL CELL

The peripheral cell provides a total flexibility of input/output configurations.

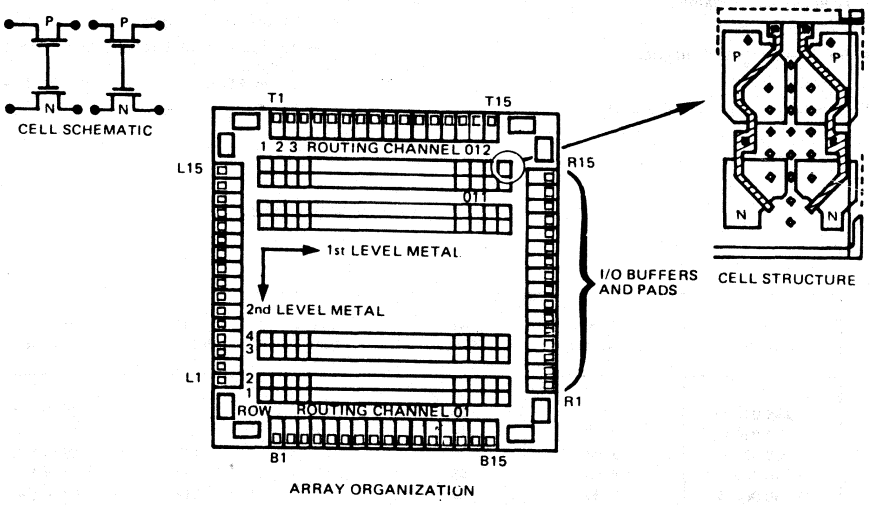


FIGURE 1 – TSGB 1000 MATRIX ARCHITECTURE

It offers very high and full immunity and protection against ESD and latch-up phenomenoms :

- typ ± 500 mA Latch-up immunity.
- min ± 2000 V Electrostatic protection.

Various functions can be implemented by selecting the appropriate macros listed in Fig. 2.

- TTL Buffers
- CMOS Buffers
- 3 State Buffers
- 3 State Bidirectional Buffers
- Open Drain Output Buffers
- Pull-up and Pull-down Resistors
- Schmitt Trigger
- Crystal-Oscillator Amplifier
- Power Supply Cells

FIGURE 2 – PERIPHERAL CELL FUNCTIONS

All functions dedicated to I/O cells are implemented within the peripheral cell area. Especially functions like 3 State Enable Command, Adaptation stage, are implemented within a predriver area, resulting then to 100 % of the internal array dedicated to customer circuit.

POWER SUPPLY DISTRIBUTION

To improve noise immunity and allow high operating speed, the V_{DD} and V_{SS} dispatching onto the die has been particularly very well designed.

Noise immunity is achieved by separate power rings : 1 ring distributes power to the driver cells, the other one to the core logic.

High speed and low voltage drop are achieved by a major power bus structure splitting the array into different quadrants. Within each quadrant, power distribution is accomplished wia a grid structure performing uniform voltage levels over the array.

The grid consists of 8 basic gate groups.

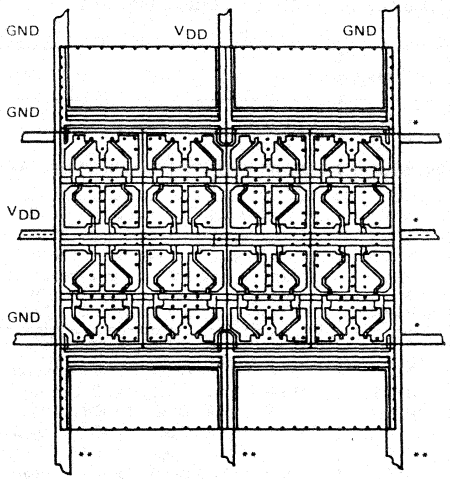
Figure 3 illustrates the power distribution within the cell group.

Thus each gate array circuit must have at least 4 power pins : 2 V_{DD} and 2 V_{SS} pins. According to the package, the matrix and the operating frequency of the circuit, an analysis will be done jointly between customer and Thomson semi-conducteurs in order to get the right and sufficient number of V_{DD} and V_{SS} power pins..

THOMSON MACRO LIBRARY

The TSGB gate array series is supported by a complete and extensive macrocell library.

Thomson Semiconducteurs has a comprehensive macrocell library consisting of both hard and soft macrocells. The hard macros are described in Fig. 5, the soft macros are described in a separate data sheet.



* 1st LEVEL METAL
** 2nd LEVEL METAL

FIGURE 3 – POWER DISTRIBUTION GRID

Hard macros have a fixed layout for efficiency. The interconnect is almost entirely within the active area of the cell, and the routing program has no opportunity to modify the cell internally.

Soft macros, on the other hand, are constructed from small, primitive macrocells. Soft macros are described only at the net list level. The same soft macro may have different layouts in different design situations.

Each macro is predefined and pre-characterized for electrical performances.

Propagation delays are given as a function of 3 parameters : fanout, operating temperature, power supply values. In addition typical, best and worst case values are given. An example is shown for a 2 input NAND in Fig. 4.

Switching Characteristics (V_{DD} = 5 V, T = 25°C, Typical Process) :

NA02

Delay Measured		Parameter	Typical propagation delay (ns) Fanout (Unit Loads)				
From	To		1	2	3	4	8
A	Q	t_{PLH}	0.98	1.48	1.99	2.49	4.51
		t_{PHL}	0.92	1.45	1.98	2.51	4.63
B	Q	t_{PLH}	1.26	1.76	2.27	2.77	4.79
		t_{PHL}	0.71	1.24	1.77	2.30	4.42

FIGURE 4 – 2 INPUT NAND (NA02) SWITCHING CHARACTERISTICS

TSGB SERIES HARD MACROCELL LIBRARY

Name	Description	Gate Count
AA02	2-Input AND	2
AA03	3-Input AND	2
AA04	4-Input AND	3
AA05	5-Input AND	3
AN01	Two 2-Input AND into 2-Input NOR	2
AN02	One 2-Input AND into 2-Input NOR	2
AN03	One 2-Input AND into 3-Input NOR	2
AN04	One 2-Input AND and one 2-Input NOR into 2-Input NOR	3
AN05	Four 3-Input AND into 4-Input NOR	6
AN06	Three 3-Input AND into 3-Input NOR	5
AO01	One 2-Input AND into 2-Input OR	2
DF08	D FF, 1-Phase Clock, Pos.-Edge Trigger	5
DF09	D FF, 1-Phase Clock, Pos.-Edge Trigger, Set (L)	6
DF0A	D FF, 1-Phase Clock, Pos.-Edge Trigger, Reset (L)	6
DF0B	D FF, 1-Phase Clock, Pos.-Edge Trigger, Set (L), Reset (L)	7
DF0C	D FF, 1-Phase Clock, Pos.-Edge Trigger, Set	6
DF0D	D FF, 1-Phase Clock, Pos.-Edge Trigger, Reset	7
DF0E	D FF, 1-Phase Clock, Pos.-Edge Trigger, Set, Reset	7
DF16	D FF, 1-Phase Clock, Pos.-Edge Trigger, Syn Reset	6
DF17	D FF, 1-Phase Clock, Pos.-Edge Trigger, Syn Set (L)	6
DL01	D Latch, 2-Phase Clock, Pos. Enable	3
DL18	D Latch, 2-Phase Clock, Pos. Enable, Set, Reset, Q Only	4
DL19	D Latch, 2-Phase Clock, Pos. Enable, Set, Q only	3
DL1A	D Latch, 2-Phase Clock, Pos. Enable, Reset, Q Only	3
DL1B	D Latch, 2-Phase Clock, Pos. Enable, Set (L), Q Only	3
DL1C	D Latch, 2-Phase Clock, Pos. Enable, Reset (L), Q Only	3
DL1D	D Latch, 2-Phase Clock, Pos. Enable, Set (L), Reset (L), Q Only	4
DL53	D Latch, 1-Phase Clock, Neg. Enable	3
DL55	D Latch, 1-Phase Clock, Neg. Enable, Set (L)	4
DL57	D Latch, 1-Phase Clock, Neg. Enable, Reset	4
EN01	Exclusive NOR	3
EO01	Exclusive OR	3
II11	Internal Buffer, 2 Inverters, 1X QN, 1X Q	1
II12	Internal Buffer, 2 Inverters, 1X QN, 2X Q	2
II13	Internal Buffer, 2 Inverters, 1X QN, 3X Q	2
II21	Internal Buffer, 2 Inverters, 2X QN, 1X Q	2
II22	Internal Buffer, 2 Inverters, 2X QN, 2X Q	2
II31	Internal Buffer, 2 Inverters, 3X QN, 1X Q	2
IN01	1X Power Inverter	1
IN02	2X Power Inverter	1
IN03	3X Power Inverter	2
IN04	4X Power Inverter	2
IN05	5X Power Inverter	3
IN06	6X Power Inverter	3
IT01	Internal 3-State Buffer, Non-Inverting	2
IT0F	Internal 3-State Buffer, Inverting	2
IT03	Internal 3-State Buffer, Double-Buffered, Inverting	3
MU23	2-To-1 Inverting Multiplexer	2
MU42	4-To-1 Inverting Multiplexer	4
NA02	2-Input NAND	1
NA03	3-Input NAND	2
NA04	4-Input NAND	2
NA05	5-Input NAND	3
NA06	6-Input NAND	3

TSGB SERIES HARD MACROCELL LIBRARY (Continued)

Name	Description	Gate Count
NA08	8-Input NAND	6
NAF6	6-Input Complex NAND	5
NO02	2-Input NOR	1
NO03	3-Input NOR	2
NO04	4-Input NOR	2
NO05	5-Input NOR	3
NO06	6-Input NOR	3
NO08	8-Input NOR	6
NOF6	6-Input Complex NOR	5
ON01	Two 2-Input OR into 2-Input NAND	2
ON02	One 2-Input OR into 2-Input NAND	2
ON03	One 2-Input OR into 3-Input NAND	2
ON04	One 2-Input OR And One 2-Input NAND into 2-Input NAND	3
OR02	2-Input OR	2
OR03	3-Input OR	2
OR04	4-Input OR	3
OR05	5-Input OR	3
RS00	Set (L) Reset (L) NAND Latch	2
RS01	Set/Reset NOR Latch	2
ZZ20	V_{SS} Power	0
ZZ21	V_{DD} Power	0

I/O BUFFERS

Name	Description	I/O Cell Count	Gate Count
IB01	Non-Inverting CMOS Input Buffer	1	0
IB02	Inverting CMOS Input Buffer	1	0
IB04	Inverting CMOS Input Buffer with Pull-Up	1	0
IB06	Inverting CMOS Input Buffer with Pull-Down	1	0
IB07	Non-Inverting TTL Input Buffer	1	0
IB08	Inverting TTL Input Buffer	1	0
IB0A	Inverting TTL Input Buffer with Pull-Up	1	0
IB0C	Inverting TTL Input Buffer with Pull-Down	1	0
IO11	Non- inverting TTL 3-State Output Buffer with Non-Inverting TTL Input Buffer	1	0
IO12	Inverting TTL 3-State Output Buffer with Inverting TTL Input Buffer	1	0
IO13	Non-Inverting CMOS 3-State Output Buffer with Non-Inverting CMOS Input Buffer	1	0
IO14	Inverting CMOS 3-State Output Buffer with Inverting CMOS Input Buffer	1	0
OB31	Non-Inverting TTL Output Buffer	1	0
OB32	Inverting TTL Output Buffer	1	0
OB33	Non-Inverting CMOS Output Buffer	1	0
OB34	Inverting CMOS Output Buffer	1	0
OB35	Non-Inverting Open-Drain Output Buffer, Current Source, with Pull-up	1	0
OB36	Inverting Open-Drain Output Buffer, Current Source	1	0
OB37	Non-Inverting Open-Drain Output Buffer, Current Sink, with Pull-Down	1	0
OB38	Inverting Open-Drain Output Buffer, Current Sink	1	0
OB39	Non-Inverting CMOS 3-State Output Buffer	1	0
OB3A	Inverting CMOS 3-State Output Buffer	1	0
OB3B	Non-Inverting TTL 3-State Output Buffer	1	0
OB3C	Inverting TTL 3-State Output Buffer	1	0

FIGURE 5 – TSGB MACROCELL LIBRARY HARD MACROS + I/O BUFFERS

THOMSCAD DESIGN AUTOMATION SYSTEM

The Thomson Semiconducteurs TSGB series is fully supported by a complete computer aided design (CAD) system. The Thomson CAD system, THOMSCAD, is complete in that once a design is entered all the tools necessary to complete that design are available to the user in this one system.

These tools include schematic capture, logic simulation fault simulation, automatic place and route, parasitic delay extraction, and test pattern generation.

THOMSCAD Design Automation System is available on a DEC™ VAX™ computer system. *

In addition, the TSGB series library is implemented and available on various CAE work stations :

- Mentor Graphics,
- Daisy Systems,
- Valid Logic.

Thomson Semiconducteurs has developped direct interfaces between these CAE workstations and itsTHOMSCAD system.

The main CAD tools available within THOMSCAD™ are :

SCHEMATIC GRAPHIC CAPTURE

SDS™ provides graphic capture of schematic circuit diagram. Designer can create blocks by using the 100 % hierarchy feature of SDS™.

LOGIC SIMULATION

HIL03™ hierarchical logic simulator allows design verification and timing analysis of the circuit. A pre-layout timing analysis is run with calculated delays based on fanout, V_{DD}, temperature and best, typical or worst case librairies.

The 2 input files to HIL03™ are the net list generated from graphic capture and the input test pattern description.

PLACEMENT AND ROUTING

CADISYS™ software is an efficient automatic place and route allowing up to 95 % silicon use (80 % for the largest arrays).

In addition to this, user is given other following features :

- hierarchical work,
- capability to preplace I/O, cells or blocks,
- capabitility to force priorities on nets for critical path routing.

PARASITIC DELAY EXTRACTION

POLYPE™ is computing the exact parasitic delays brought by the placement and routing. Delays are based both on resistance and capacitance of each interconnect.

As soon as the parasitic RC delays are extracted, user can run a post layout simulation for accurate timing new analysis.

TEST GENERATION

According to the input test patterns already described, user can determinate the testability coverage ratio of its test sequence thanks to the fault simulator which is incorporated within HIL03™.

Depending of the fault simulator results, user can generate new input test patterns in order to improve testability coverage.

EPIGRAD™ software converts automatically the post-layout simulation (with parasitic delays) file into test patterns directly compatible with Thomson Semiconducteurs Test equipments.

At same time static and dynamic parameters are added to the functional test pattern file : all input/ouptut levels are tested during the functional test sequence.

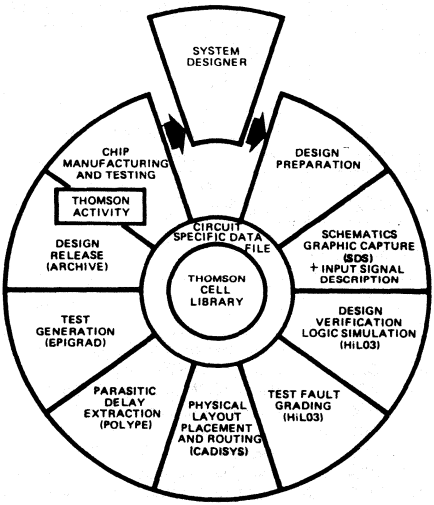


FIGURE 6 – THOMSCAD DESIGN AUTOMATION SYSTEM

* DEC and VAX are trademarks of Digital Equipment Corporation.

Design Automation system THOMSCAD is a trademark of Thomson Semiconducteurs.
SDS is a trademark of Silvar Lisco
HILO3 is a trademark of Genrad.
CADISYS is a trademark of Mentor Graphics.
POLYPE is a trademark of Thomson Semiconducteurs.
EPIGRAD is a trademark of Thomson Semiconducteurs.

Figure 7 shows the development phases of a TSGB series gate array. The design translation phase can be done either on VAX equipment with THOMSCAD or on CAE workstations like Daisy Systems, Mentor Graphics and VALID Logic. In that case, direct interfaces exist in order to pursure design implementation and test generation phases with THOMSCAD.

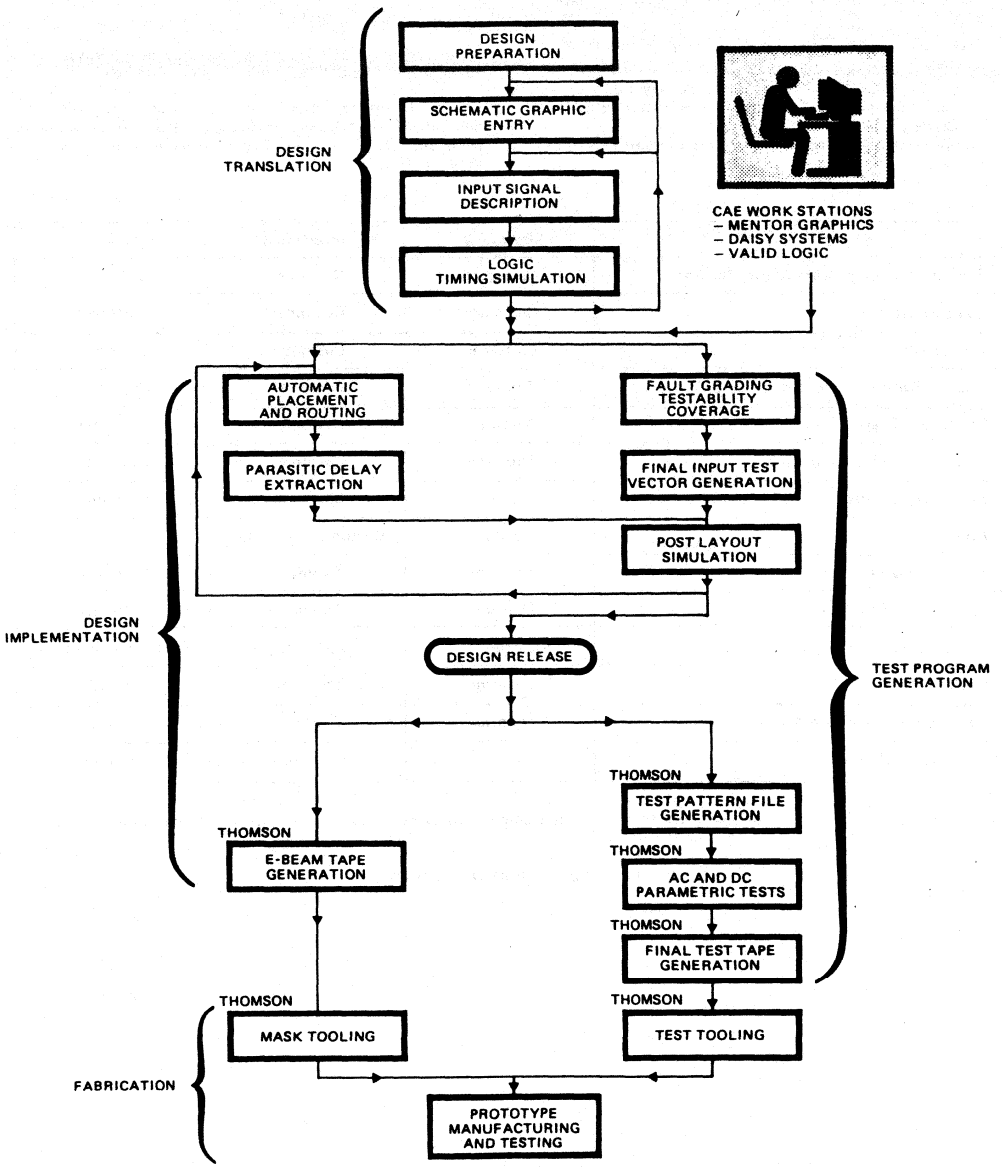


FIGURE 7 – TSGB SERIES GATE ARRAY DEVELOPMENT FLOW

CUSTOMER DESIGN INTERFACE

Thomson Semiconducteurs has developped several interfaces for customers giving them easy and flexible Design approaches for TSGB 2 µ/2 metal HCMOS gate arrays series.

User can access THOMSCAD Design Automation System :

- via the Thomson Semiconducteurs Design Centers,
- via connection to Thomson Semiconducteurs CAD Center,
- via the Thomson Semiconducteurs associated Design Centers.

Other Design capabilities are offered to user via CAE workstations :

- Daisy Systems,
- Mentor Graphics,
- Valid Logic.

or in the future via IBM PC.

According to all of these design possibilities, Thomson Semiconducteurs defined 3 main custom interface.

Figure 8 outlines these interfaces. Each interface delineates the responsabilities of customer and Thomson Semiconducteurs during circuit development flow shown in Fig. 7.

	Interface 2	Interface 3	Interface 4
Functional & Logic Circuit Specification	Customer	Customer	Customer
Logic description	Customer	Customer	Customer
Test pattern	Customer	Customer	Customer
Graphic Capture + input signal Entry	Thomson	Customer	Customer
Design Verification	Thomson	Customer	Customer
Pre-layout timing Simulation	Thomson	Customer	Customer
Testability coverage	Thomson	Customer	Customer
Approval	Customer	Customer/Thomson	–
Auto Place and Route	Thomson	Thomson	Customer
Post-Layout Simulation	Thomson	Thomson	Customer
Design Release	Customer	Customer/Thomson	Customer/Thomson
Mask tooling	Thomson	Thomson	Thomson
Waper personnalization & test	Thomson	Thomson	Thomson
Prototype Delivery	Thomson	Thomson	Thomson

With interface 2, design can be done either at Thomson Semiconducteurs Design Center facilities or at customer location.

FIGURE 8 – DESIGN INTERFACES

ABSOLUTE MAXIMUM RATINGS (Note 1)
(Referenced to V_{SS})

Supply Voltage V_{DD} . . . . . – 0.5 V to + 7.0 V
Input or Output Voltage . . . . . –0.5 V to (V_{DD} + 0.5 V)
DC Forward Bias Current, Input or Output, I_K . . . . . ± 100 mA
Storage Temperature (Ceramic) . . . . . – 65 to + 150°C
Storage Temperature (Plastic) . . . . . – 40 to + 125°C

Note 1 :Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Operating Supply Voltage, V_{DD} . . . . . 5.0 V ± 10 %
Extended Supply Voltage . . . . . 3.0 V to 6.0 V
Operating Ambient Temperature
Military . . . . . – 55 to + 125°C
Industrial . . . . . – 40 to + 85°C
Commercial . . . . . 0 to + 70°C

DC ELECTRICAL CHARACTERISTICS – TTL INTERFACE
V_{DD} = 5.0 V ± 10 % - 55°C to 125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
V_{IL}	Low-Level Input Voltage				0.8	V	
V_{OL}	Low-Level Output Voltage	I_{OL} = 4.0 mA			0.4	V	
V_{OH}	High-Level Output Voltage	I_{OH} = - 2.0 mA	2.7			V	
I_{OL}	Low-Level Output Current	V_{OL} = 0.4 V, 70°C			4.0	mA	
		V_{OL} = 0.4 V, 85°C			4.0	mA	
		V_{OL} = 0.4 V, 125°C			4.0	mA	

DC ELECTRICAL CHARACTERISTICS – CMOS INTERFACE
V_{DD} = 5.0 V ± 10 % – 40°C to+ 85°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
V_{IL}	Low-level Input Voltage				30 % V_{DD}	V	
V_{IH}	High-Level Input Voltage		70 % V_{DD}			V	
V_{OL}	Low-Level Output Voltage	I_{OL} = 20 µA			0.1	V	
V_{OH}	High-Level Output Voltage	I_{OH} = - 20 µA	V_{DD} - 0.1			V	

V_{IH}	High-Level Input Voltage		2.0*		
			2.2		

* to θ = 0 to 70°C

DC ELECTRICAL CHARACTERISTICS – GENERAL

V_{DD} = 5.0 V ± 10 % Across Temperature Range Unless Otherwise Specified

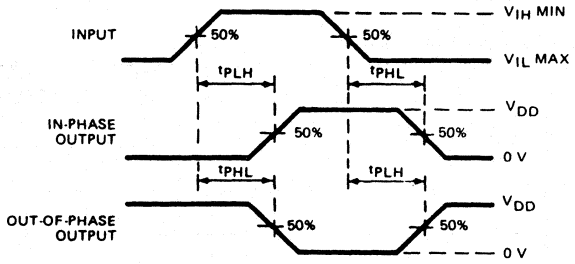
Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
I_{IL}/I_{IH}	Low-Level/High-Level input leakage current (without pull-up / pull-down)	$V_I = V_{SS}$ or $V_I = V_{DD}$			±1	µA	0/70°C
					±3	µA	–40/+85°C
					±5	µA	– 55/+125°C
I_{OZ}	3 state output leakage current	$V_O = 0$ or V_{DD}			±2.5	µA	0/70°C
					±5	µA	– 40/+85°C
					±10	µA	– 55/+125°C
I_{KLU}	Max DC I/O Current per Pin to Safeguard Latch-up	$V_O < V_{SS}$, $V_O > V_{DD}$	±100	±500		mA	
V_{ESD}	Electrostatic Discharge Protection	C = 100 pF R = 1500 Ohms Test Circuit per DOD-HD BK-263	±2000			V	
I_{DDSB}	Standby Current	$V_I = V_{DD}$ or V_{SS}		5		nA/gate	
I_{DDOP}	Operating Current	$V_I = V_{DD}$ or V_{SS}		5		µA/gate /MHz	

AC ELECTRICAL CHARACTERISTICS

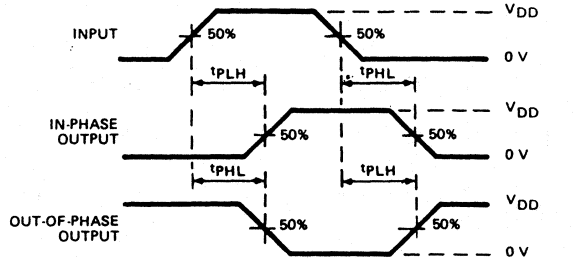
V_{DD} = 5.0 V ± 10 % Across Temperature Range
Standard Condition = 2 loads + 1 mm of metal interconnect
(See Fig. 9 titled "Switching Waveforms" for definitions).

Cell (Name)		Condition	Typ 25°C	Max 0/70°C	Max −40/85°C	Max −55/125°C	Units
Standard Inverter (IN01)	t_{PHL}	Std	1.1	2.6	2.8	3.1	ns
	t_{PLH}						ns
2-input NAND (NA02)	t_{PHL}	Std	1.5	3.5	3.7	4.2	ns
	t_{PLH}						ns
2-Input NOR (NO02)	t_{PHL}	Std	1.9	4.3	4.5	5.1	ns
	t_{PLH}						ns
4-Input NAND (NA04)	t_{PHL}	Std	2.3	5.4	5.7	6.4	ns
	t_{PLH}						ns
D-Type Flip-Flop (DF08)		Std					ns
Clk to Q	t_{PHL}		2.0	4.6	4.8	5.4	ns
	t_{PLH}						ns
Set-up Time	t_{SU}		1.2	2.8	2.9	3.3	ns
Hold Time	t_H		0.3	0.7	0.7	0.8	ns
TTL Non-Inverting Output Driver (OB01)	t_{PHL}	10 LSTTL, 50 pF	2.7	6.3	6.6	7.5	ns
	t_{PLH}						ns
	t_{PHL}	5 LSTTL, 25 pF	2.0	4.7	4.9	5.6	ns
	t_{PLH}						ns
	t_{PHL}	1 LSTTL, 15 pF	1.8	4.1	4.3	4.8	ns
	t_{PLH}						ns
CMOS Non-Inverting Output Driver (OB03)	t_{PHL}	10 LSTTL, 50 pF	2.9	6.6	6.9	7.8	ns
	t_{PLH}						ns
	t_{PHL}	5 LSTTL, 25 pF	2.3	5.2	5.4	6.2	ns
	t_{PLH}						ns
	t_{PHL}	1 LSTTL, 15 pF	2.0	4.5	4.7	5.3	ns
	t_{PLH}						ns
TTL Non-Inverting 3-State Output-Driver (IO01)	t_{PHL}	10 LSTTL, 50 pF	4.5	10.5	11.0	12.4	ns
	t_{PLH}						ns
	t_{PHL}	5 LSTTL, 25 pF	3.9	9.0	9.4	10.7	ns
	t_{PLH}						ns
	t_{PHL}	1 LSTTL, 15 pF	3.6	8.4	8.8	9.9	ns
	t_{PLH}						ns
	t_{PAZ}	Active to Z	5.0	11.6	12.1	13.7	ns
	t_{PZA}	Z to Active					ns
CMOS Non-Inverting 3-State Output Driver (IO03)	t_{PHL}	10 LSTTL, 50 pF	4.6	10.6	11.1	12.6	ns
	t_{PLH}						ns
	t_{PHL}	5 LSTTL, 25 pF	4.0	9.2	9.6	10.9	ns
	t_{PLH}						ns
	t_{PHL}	1 LSTTL, 15 pF	3.7	8.6	8.9	10.1	ns
	t_{PLH}						ns
	t_{PAZ}	Active to Z	5.4	12.6	13.1	14.9	ns
	t_{PZA}	Z to Active					ns
TTL Inverting Receiver (IB08)	t_{PHL}	Std	0.9	2.2	2.2	2.5	ns
	t_{PLH}						ns
CMOS Inverting Receiver (IB02)	t_{PHL}	Std	0.8	1.9	2.0	2.2	ns
	t_{PLH}						ns

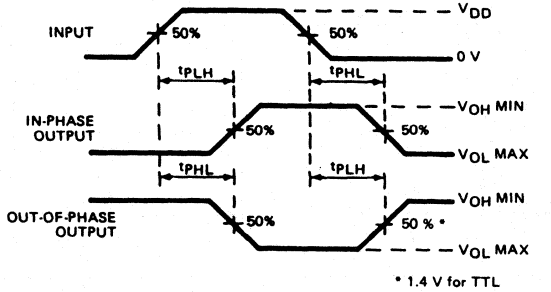
Typical Values are @ 5.0 V
Refer to Wave Forms in Figures 9 and 10
Refer to Figure 10 for test load



VIEW A. Input Buffer Propatation Delay

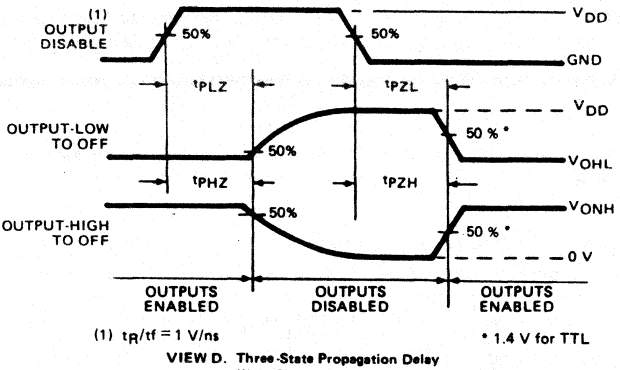


VIEW B. Internal Gate Propagation Delay



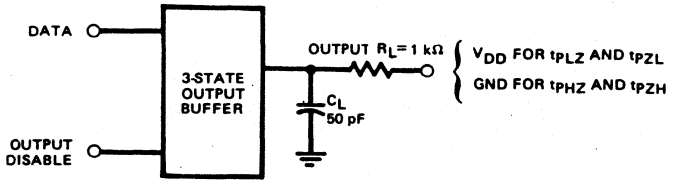
VIEW C. Output Buffer Propagation Delay

FIGURE 9 – SWITCHING WAVEFORMS



VIEW D. Three-State Propagation Delay Wave Shapes

FIGURE 9 – SWITCHING WAVEFORMS (Cont'd)



CHARACTERIZATION CIRCUIT

FIGURE 10 – TEST CIRCUIT

PACKAGING

Thomson Semiconducteurs has a wide variety of package options available to the user :

- Dual in line packages (DIP)
  - . Plastic
  - . Cerdip
  - . Side Braze
- Chip carriers
  - . Plastic Leaded Chip Carriers (PLCC)
  - . Ceramic Leadless Chip Carriers (CLCC)
- Pin Grid Arrays
  - . Plastic Pin Grid Arrays (PPGA)
  - . Ceramic Pin Grid Arrays (CPGA)

Where different packaging requirements are needed, contact Thomson Semiconducteurs Marketing. Thomson Semiconducteurs can also supply gate arrays products in dice form (chip tray or wafer form).

Additional package options will be available in the future.

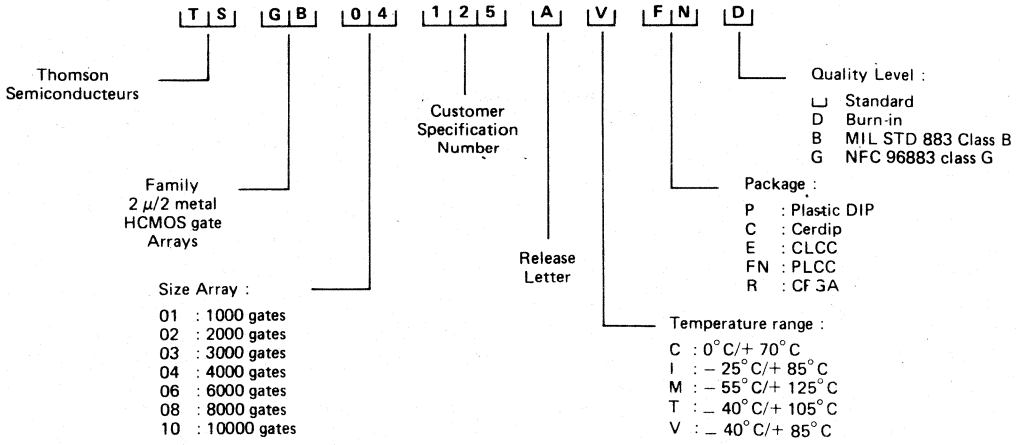
A table listing package availability for each size array is presented in Figure 11.

Part	DIP				PGA							LCC					
Number	24	28	40	48	68	84	100	120	144	180	208	44	52	68	84	100	124
TSGB 1000	P/C	P/C	P/C	P/C	P/C							P/C	P/C	P/C			
TSGB 2000	P/C	P/C	P/C	P/C	P/C	P/C						P/C	P/C	P/C	P/C		
TSGB 3000		P/C	P/C	P/C	P/C	P/C	P/C							P/C	P/C	C	
TSGB 4000			P/C	P/C	P/C	P/C	P/C	P/C						P/C	P/C	C	C
TSGB 6000					P/C	P/C	P/C	P/C	C					P/C	P/C	C	C
TSGB 8000						P/C	P/C	P/C	C	C					P/C	C	C
TSGB 10000						P/C	P/C	P/C	C	C	C			C	P/C	C	C

Notes : 1 - P = Plastic package
1 - C = Ceramic package

FIGURE 11 – GATE ARRAY PACKAGING OPTIONS (CERAMIC & PLASTIC)

ORDERING INFORMATION



THOMSON COMPONENTS SEMICONDUCTEURS

TSGB SERIES SOFTWARE MACROS
TTL LOGIC EQUIVALENTS
2 μ/2 METAL HCMOS GATE ARRAYS

TTL DEVICE	FUNCTIONAL DESCRIPTION	SOFT MACRO	GATE COUNT
74/5400	QUAD 2-INPUT POSITIVE NAND GATES	T00AA	4
74/5402	QUAD 2-INPUT POSITIVE NOR GATES	T02AA	4
74/5404	HEX INVERTERS	T04AA	6
74/5408	QUAD 2-INPUT POSITIVE AND GATES	T08AA	8
74/5410	TRIPLE 3-INPUT POSITIVE NAND GATES	T10AA	6
74/5411	TRIPLE 3-INPUT AND GATES	T11AA	6
74/5420	DUAL 4-INPUT POSITIVE NAND GATES	T20AA	4
74/5421	DUAL 4-INPUT POSITIVE AND GATES	T21AA	6
74/5423	EXPANDABLE DUAL 4-INPUT POSITIVE NOR GATES WITH STROBE	T23AA	9
74/5425	DUAL 4-INPUT POSITIVE NOR GATES WITH STROBE	T25AA	8
74/5427	TRIPLE 3-INPUT POSITIVE NOR GATES	T27AA	6
74/5430	8-INPUT POSITIVE NAND GATES	T30AA	6
74/5432	QUAD 2-INPUT POSITIVE OR GATES	T32AA	8
74/5442	4-TO-10 LINE DECODER (BCD TO DECIMAL)	T42AA	28
74/5443	4-TO-10 LINE DECODER (EXCESS-3 TO DECIMAL)	T43AA	28
74/5444	4-TO-10 LINE DECODER (EXCESS-3-GRAY TO DECIMAL)	T44AA	28
74/5445	BCD-TO-DECIMAL DECODER/DRIVER	T45AA	28
74/5450	DUAL 2-WIDE, 2-INPUT AND-OR-INVERT GATES, ONE GATE EXPANDABLE	T50AA	6
74/5451	DUAL 2-WIDE, 2-INPUT AND-OR-INVERT GATES	T51AA	4
74/5452	EXPANDABLE 4-WIDE AND-OR GATES	T52AA	8
74/5453	EXPANDABLE 4-WIDE AND-OR-INVERT GATES	T53AA	8
74/5454	4-WIDE AND-OR-INVERT GATES	T54AA T54BA	6 8

43 Avenue de l'Europe 78140 VELIZY VILLACOUBLAY FRANCE Tel. (1) 39 46 97 19 Telex TCSF 204780F Telecopie (1) 39 46 52 64

TTL DEVICE	FUNCTIONAL DESCRIPTION	SOFT MACRO	GATE COUNT
74/5455	2-WIDE 4-INPUT AND-OR-INVERT GATES	T55AA T55BA	6 7
74/5460	DUAL 4-INPUT EXPANDERS	T60AA	4
74/5461	TRIPLE 3-INPUT EXPANDERS	T61AA	6
74/5462	4-WIDE AND-OR EXPANDERS	T62AA	9
74/5470	AND-GATE J-K POSITIVE EDGE TRIGGERED FLIP-FLOP WITH PRESET AND CLEAR	T70AA	15
74/5471	AND-GATED R-S MASTER SLAVE FLIP-FLOP WITH PRESET AND CLEAR	T71AA T71BA	17 15
74/5472	AND-GATED J-K MASTER SLAVE FLIP-FLOP WITH PRESET AND CLEAR	T72AA	15
74/5473	DUAL J-K FLIP-FLOPS WITH CLEAR	T73AA	18
74/5474	DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND CLEAR	T74AA	14
74/5475	4-BIT BISTABLE LATCHES	T75AA	14
74/5476	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	T76AA	36
74/5477	4-BIT BISTABLE LATCHES	T77AA	14
74/5478	DUAL J-K FLIP-FLOP WITH PRESET, COMMON CLEAR, AND COMMON CLOCK	T78AA	21
74/5482	2-BIT BINARY FULL ADDER	T82AA	26
74/5483	4-BIT BINARY FULL ADDER WITH FAST CARRY	T83AA	65
74/5485	4-BIT MAGNITUDE COMPARATOR	T85AA	48
74/5486	QUAD 2-INPUT EXCLUSIVE-OR GATES	T86AA	12
74/5487	4-BIT TRUE/COMPLEMENT; ZERO/ONE ELEMENTS	T87AA	19
74/5490	DECADE COUNTER (BCD SEQUENCE) (BI-QUINARY)	 T90AA T90BA	 34 34
74/5491	8-BIT SHIFT REGISTER; SERIAL-IN, SERIAL-OUT, GATED INPUT	T91AA	42
74/5492	DIVIDE-BY-TWELVE COUNTER; DIVIDE-BY-TWO AND DIVIDE-BY-SIX	T92AA	35
74/5493	4-BIT BINARY COUNTER; DIVIDE-BY-TWO AND DIVIDE-BY-EIGHT	T93AA	28
74/5494	4-BIT SHIFT REGISTER; DUAL ASYNCHRONOUS PRESETS	T94AA	39
74/5495	4-BIT SHIFT REGISTER; PARALLEL IN, PARALLEL OUT, SHIFT RIGHT/LEFT, SERIAL INPUT	T95AA	37

TTL DEVICE	FUNCTIONAL DESCRIPTION	SOFT MACRO	GATE COUNT
74/5496	5-BIT SHIFT REGISTER; ASYNCHRONOUS PRESET	T96AA	42
74/5498	4-BIT DATA SELECTOR/STORAGE REGISTER; SELECTS 1 OF 2, 4-BIT WORDS	T98AA	31
74/5499	4-BIT BI-DIRECTIONAL UNIVERSAL SHIFT REGISTER	T99AA	54
74/54100	8-BIT BISTABLE LATCHES	T100AA	26
74/54101	AND-OR-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET	T101AA	16
74/54102	AND-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND CLEAR	T102AA	15
74/54103	DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR	T103AA	22
74/54106	DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND CLEAR	T106AA	22
74/54107	DUAL J-K FLIP-FLOPS WITH CLEAR	T107AA	18
74/54108	DUAL NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, COMMON CLK, AND COMMON CLEAR	T108AA	21
74/54109	DUAL J-/K POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND CLEAR	T109AA	22
74/54110	AND-GATED J-K MASTER-SLAVE FLIP-FLOP WITH DATA LOCK OUT	T110AA	17
74/54111	DUAL J-K MASTER SLAVE FLIP-FLOP WITH DATA LOCK OUT	T111AA	26
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74/54113	DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET	T113AA	20
74/54114	DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET, COMMON CLEAR, AND COMMON CLK	T114AA	21
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74/54125	QUAD BUS BUFFER GATES (3-STATE OUTPUTS; EN = 0)	T125AA	12
74/54126	QUAD BUS BUFFER GATES (3-STATE OUTPUTS; EN = 1)	T126AA	8
74/54133	13-INPUT POSITIVE NAND GATE	T133AA	11
74/54134	12-INPUT POSITIVE NAND GATE (3-STATE OUTPUTS)	T134AA	12
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TTL DEVICE	FUNCTIONAL DESCRIPTION	SOFT MACRO	GATE COUNT
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74/54139	DUAL 2-TO-4 LINE DECODER/MULTIPLEXER	T139AA	22
74/54142	DIVIDE-BY-10 COUNTER/4-BIT LATCH/DECODER/DRIVER	T142AA	84
74/54143	COUNTER/LATCH/DECODER/DRIVER	T143AA	122
74/54145	BCD-TO-DECIMAL DECODER/DRIVER	T145AA	28
74/54147	10 LINE DECIMAL TO 4 LINE BCD PRIORITY ENCODER	T147AA	34
74/54148	8-LINE TO 3-LINE OCTAL PRIORITY ENCODER	T148AA	33
74/54150	1-OF-16 DATA SELECTOR/MULTIPLEXER	T150AA	73
74/54151	1-OF-8 DATA SELECTORS/MULTIPLEXERS WITH STROBE TRUE AND COMPLEMENT OUTPUTS	T151AA	35
74/54152	1-OF-8 DATA SELECTORS/MULTIPLEXERS	T152AA	33
74/54153	DUAL 4-TO-1 LINE DATA SELECTORS/MULTIPLEXERS	T153AA	24
74/54154	4-TO-16 LINE DECODER/DEMULTIPLEXER	T154AA	57
74/54155	DUAL 1-OF-4 DECODER/DEMULTIPLEXER	T155AA	21
74/54157	QUAD 2-TO 1 DATA SELECTOR/MULTIPLEXER (NON-INVERTING OUTPUTS)	T157AA	13
74/54158	QUAD 2-TO-1 DATA SELECTOR MULTIPLEXER (INVERTING OUTPUTS)	T158AA	11
74/54160	SYNCHRONOUS 4-BIT DECADE COUNTER ASYNCHRONOUS CLEAR; SYNCHRONOUS LOAD	T160AA	65
74/54161	SYNCHRONOUS 4-BIT BINARY COUNTER ASYNCHRONOUS CLEAR; SYNCHRONOUS LOAD	T161AA	63
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74/54163	SYNCHRONOUS 4-BIT BINARY COUNTER SYNCHRONOUS CLEAR; SYNCHRONOUS LOAD	T163AA	61
74/54164	8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTER ASYNCHRONOUS CLEAR	T164AA	53
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TTL DEVICE	FUNCTIONAL DESCRIPTION	SOFT MACRO	GATE COUNT
74/54173	4-BIT D-TYPE REGISTER (3-STATE OUTPUTS)	T173AA	52
74/54174	HEX D-TYPE FLIP-FLOPS; COMMON CLEAR	T174AA	39
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74/54178	4-BIT UNIVERSAL SHIFT REGISTER	T178AA	47
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74/54193	SYNCHRONOUS UP/DOWN, DUAL CLOCK COUNTER; BINARY WITH CLEAR	T193AA	76
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TTL DEVICE	FUNCTIONAL DESCRIPTION	SOFT MACRO	GATE COUNT
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74/54259	8-BIT ADDRESSABLE LATCH	T259AA	56
74/54260	DUAL 5-INPUT NOR GATES	T260AA	8
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74/54266	QUAD 2-INPUT EXCLUSIVE-NOR GATES; OPEN COLLECTOR OUTPUTS	T266AA	12
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74/54276	QUAD J-/K FLIP-FLOP	T276AA	50
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74/54280	9-BIT ODD/EVEN PARITY GENERATOR/CHECKER	T280AA	42
74/54283	4-BIT BINARY FULL ADDER	T283AA	59
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74/54295	4-BIT BI-DIRECTIONAL UNIVERSAL SHIFT REGISTER	T295AA	43
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TTL DEVICE	FUNCTIONAL DESCRIPTION	SOFT MACRO	GATE COUNT
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74/54373	OCTAL D LATCHES 3-STATE OUTPUTS, COMMON OUTPUT COUNTER, COMMON ENABLE	T373AA	42
74/54374	OCTAL D TYPE FLIP-FLOPS; COMMON CLOCK 3-STATE OUTPUTS, COMMON OUTPUT CONTROL	T374AA	59
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74/54376	QUAD J-/K FLIP FLOPS COMMON CLK, COMMON CLEAR	T376AA	43
74/54377	OCTAL D FLIP-FLOP COMMON CLK, COMMON ENABLE	T377AA	44
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74/54381	ALU/FUNCTION GENERATORS; 8 BINARY FUNCTIONS	T381AA	194
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74/54390	DUAL DECADE COUNTERS	T390AA T390BA	58 56
74/54393	DUAL 4-BIT BINARY COUNTERS	T393AA	50
74/54395	4-BIT UNIVERSAL SHIFT REGISTER; 3-STATE OUTPUTS	T395AA	48
74/54398	QUAD 2-INPUT MULTIPLEXER WITH STORAGE	T398AA	30
74/54399	QUAD 2-INPUT MULTIPLEXER WITH STORAGE	T399AA	29
74/54425	QUAD GATES; 3-STATE OUTPUTS, EN = 1	T425AA	12
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